ToASt ASIC development status

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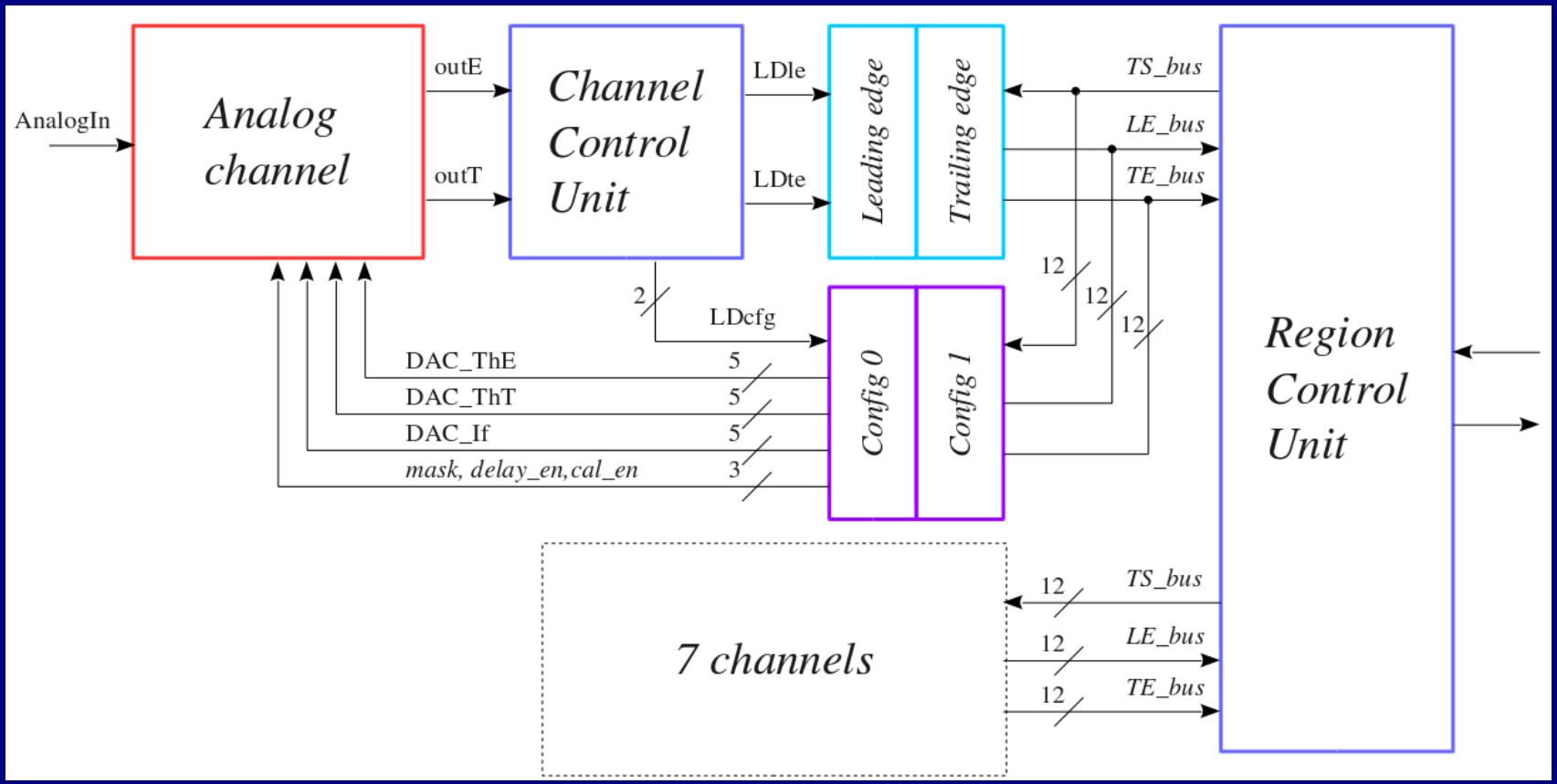
Specifications

Specification	Min	Max	Unit
Input capacitance	2	17	pF
Max rate per strip		40	kHz
Input charge	1	40	fC
Noise		1500	e^-
Preamp peaking time	50	$\geq$ 100	ns
Channels per chip	64		
Reference clock		160	MHz
Charge resolution	8		bits
Time resolution (pk-pk)		6.25	ns
Time resolution (r.m.s.)		1.8	ns
Power consumption		256	mW
Chip dimensions	4.5 $\times$ 3.5		mm^2
Pads position	On two sides only		

ToASt main characteristics

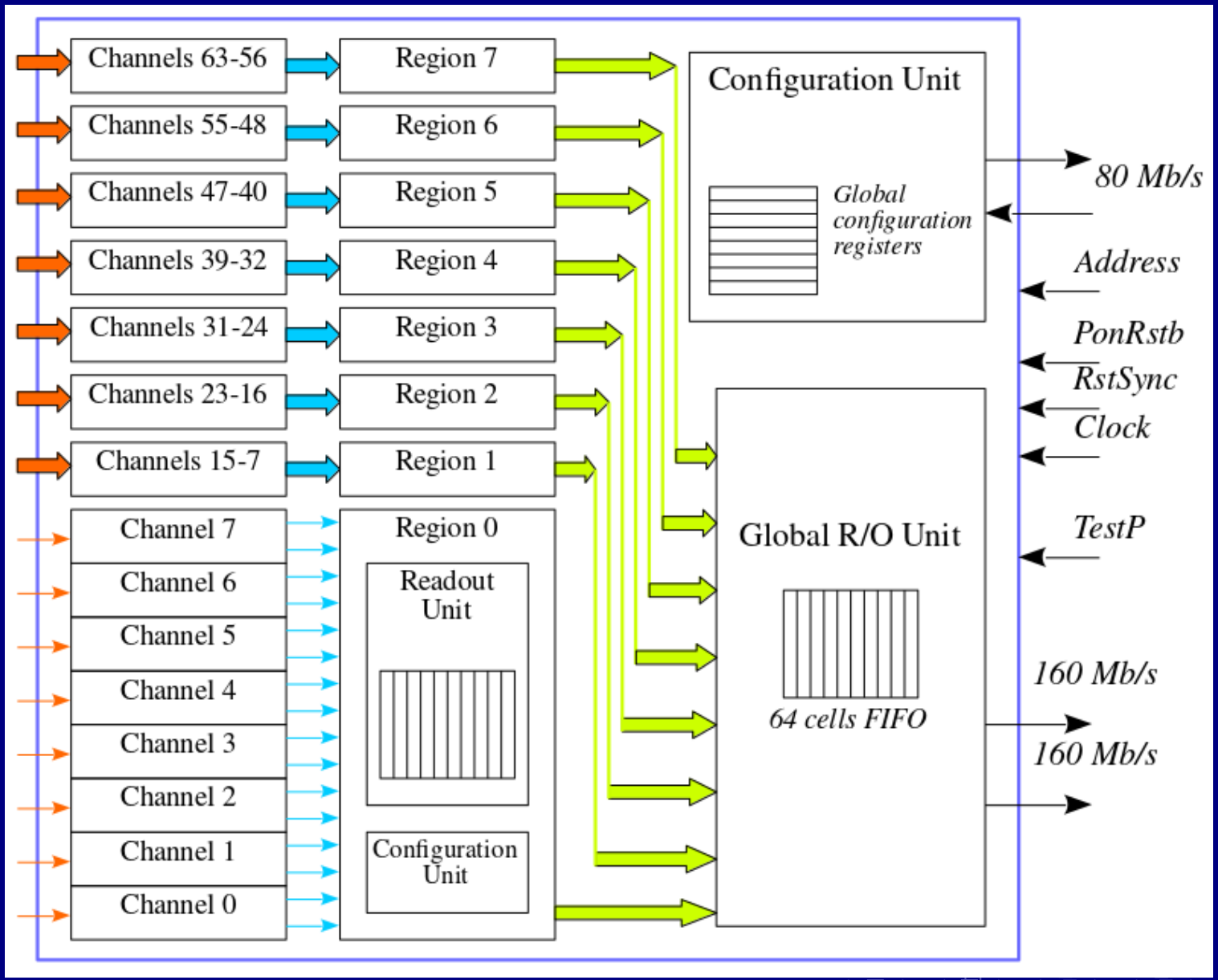
- 64 input channels
- Time of Arrival (ToA) and Time over Threshold (ToT) measurements
- Master clock frequency : 160 MHz
- Region : groups of 8 channels with local FIFO
- Second level FIFO buffering for the 8 regions
- Two output serial links at 160 Mb/s
- Serial configuration protocol at 80 Mb/s
- Full SEU protection via Triple Modular Redundancy
- CMOS 0.11 μm technology

ToASt channel schematic



- Common time reference : 12 bits time stamp distributed to all channels
- Time stamp can be Gray-encoded
- LE and TE registers latch time stamp at comparator rising/falling edges

ToASt architecture



Power analysis

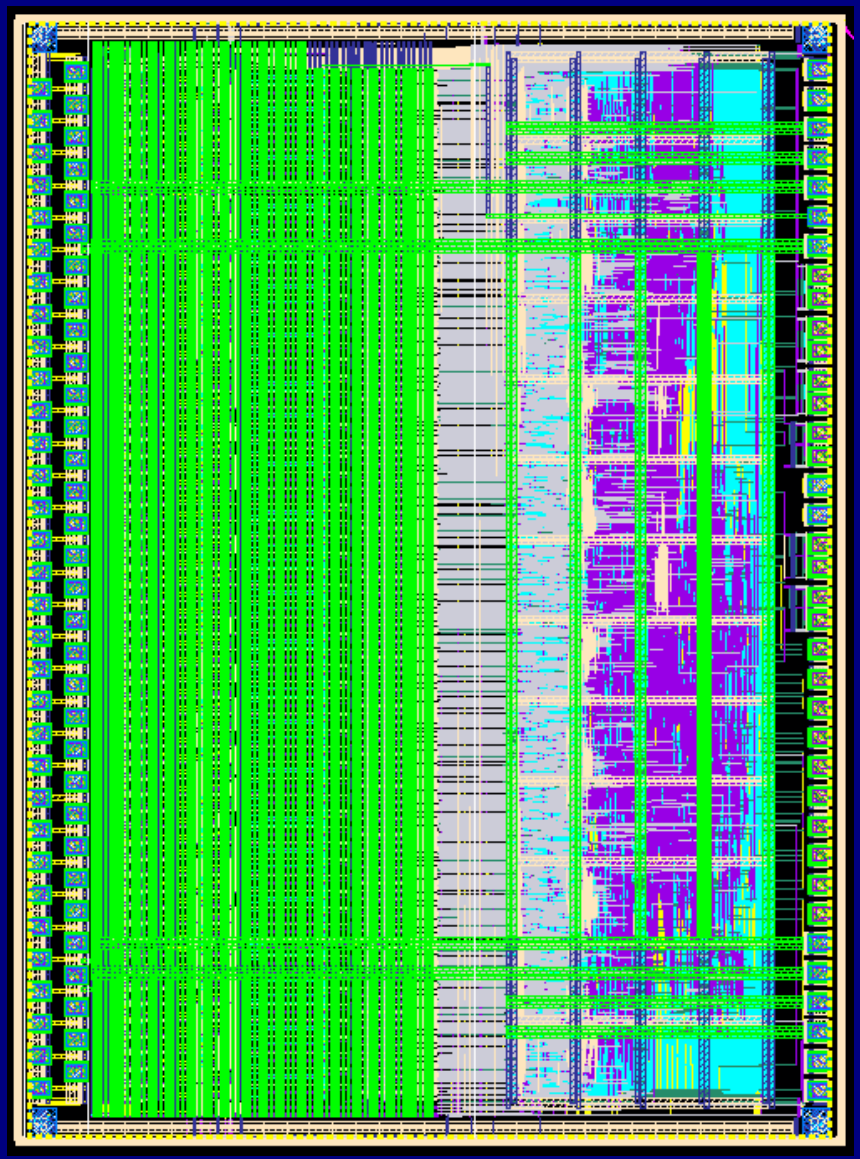
	fullTMR	noTMR	ToASt_v1
Total Analog Power	146.7	146.7	146.7
Total PADS Power	24.8	24.8	24.8
Total Digital Power	321.27	80.8	190.2
Total Power	492.78	256.08	361.7

- Power in mW, V_{DD}=1.2 V *(digital V_{DD} range 1.08÷1.32 V)*
- Simulated with realistic testbench, 160 MHz, all drivers active *(3×8.5 mW)*
- No significant difference between binary and Gray encoding
- ToASt_v1 :
  - Channel leading and trailing edge registers triplication removed
  - Region FIFO triplication removed

ToASt pinout

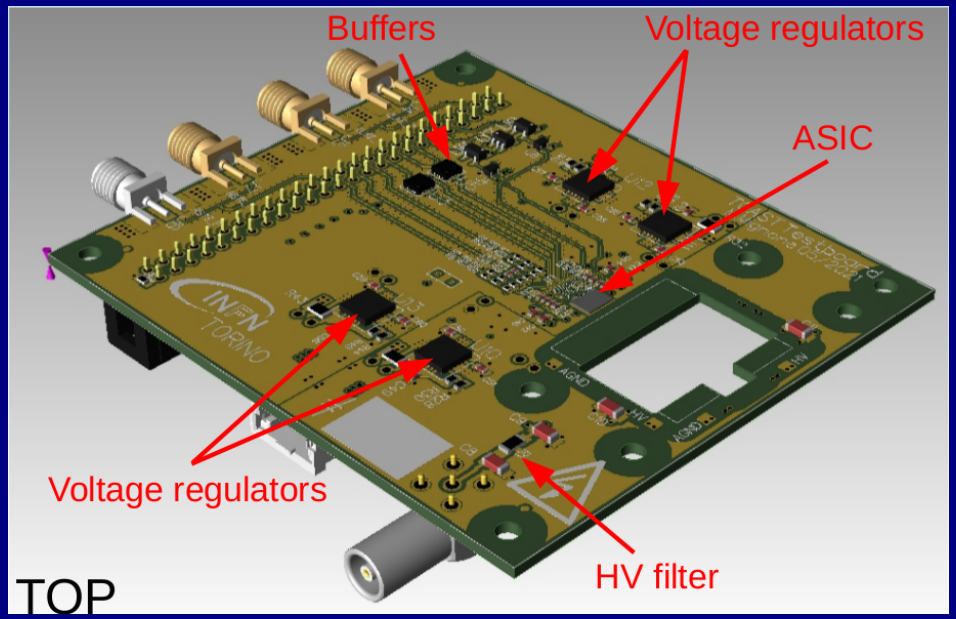
Pin name	Direction	Description
in[63:0]	In	Analog inputs
PonRstb	In	Power on asynchronous reset
RstSync	Rx	Synchronous reset
ChipAddr[6:0]	In	Chip address
TestPulse	In	Digital test pulse
CfgRx	Rx	Configuration receiver
CfgTx	Tx	Configuration transmitter
TxOut_0	Tx	Data serial output 0
TxOut_1	Tx	Data serial output 1
V_{BG}	In	Analog bandgap reference
V_{DDA},V_{SSA}	IO	Analog supply and ground
V_{DDD},V_{SSD}	IO	Digital supply and ground
V_{DDE},V_{SSE}	IO	Pads supply and ground

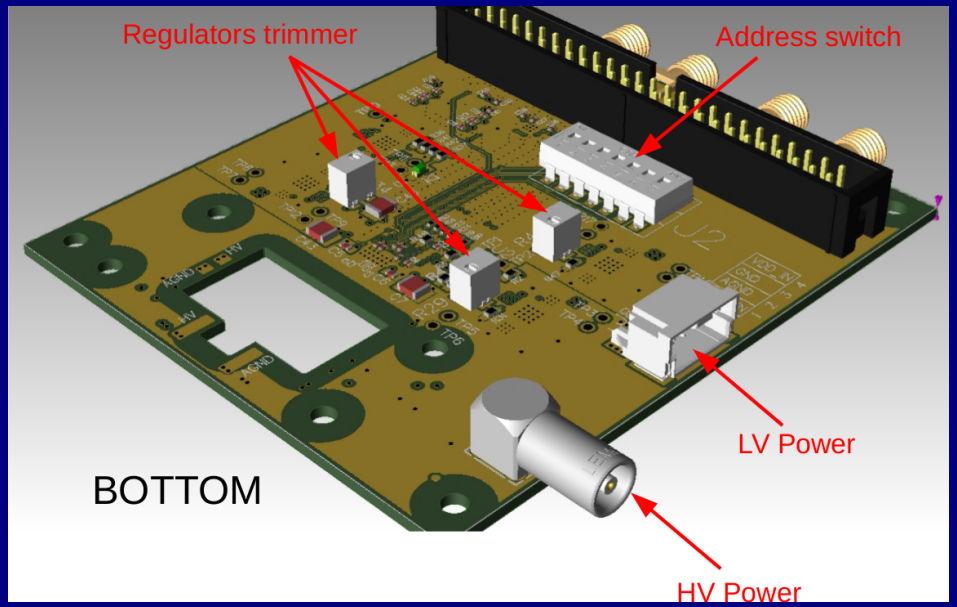
ToASt layout



- CMOS UMC 0.11 μm technology
- Digital-on-top design flow
- Die size : 3.24×4.41 mm^2
- Left pads pitch (on two rows) : 63 μm
- Right pads pitch : 90 μm
- Three power domains : analog, digital, digital pads *(all supply voltages at 1.2 V)*
- One external analog reference ($V_{BG} = 600$ mV)
- SLVS driver/receivers

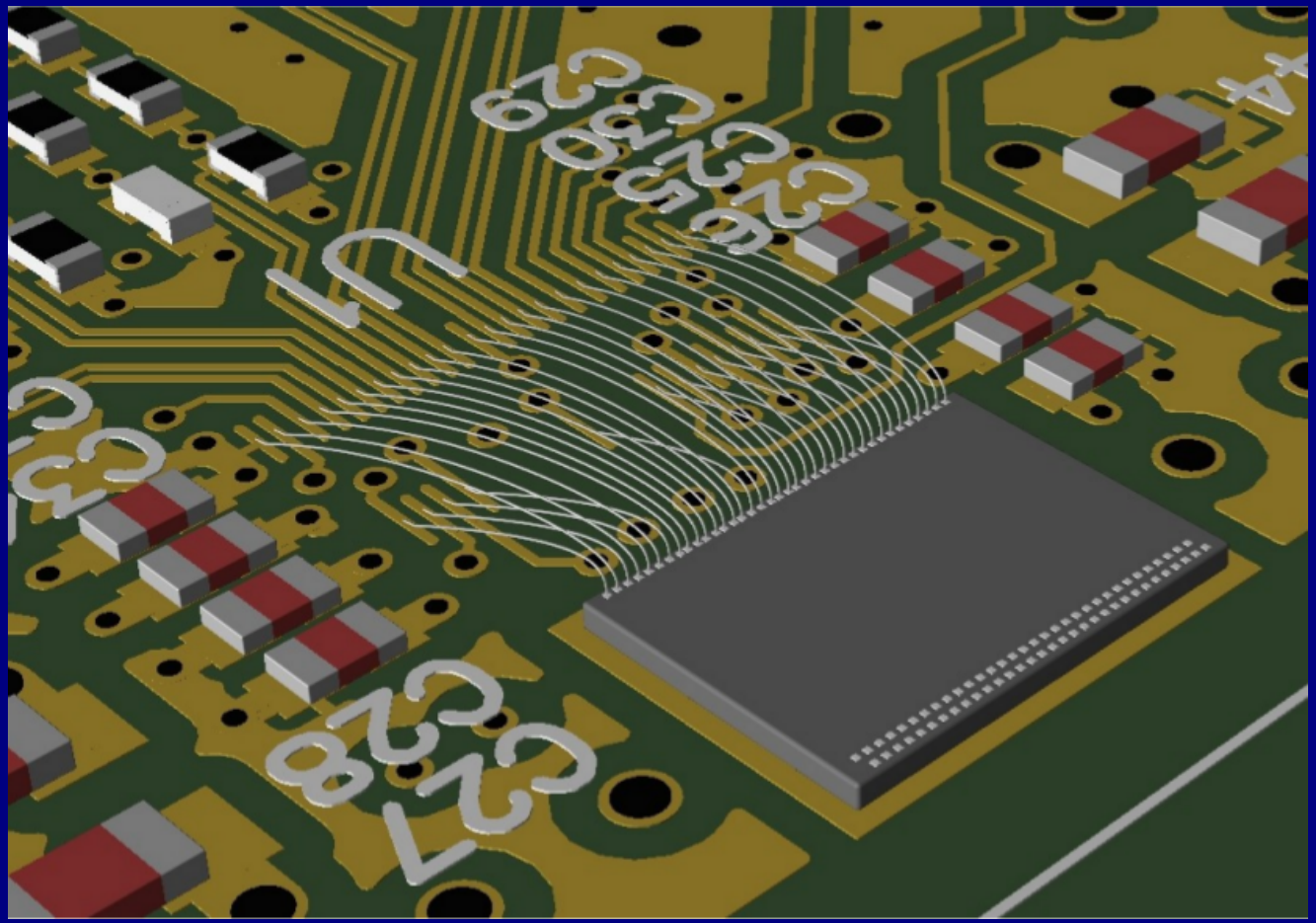
Test PCB





- External drivers for SLVS→LVDS conversion
- Adjustable power supplies

Test PCB - bonding wires



- Max wire lenght (incl. loop) : 4.5 mm
- Min wire lenght (incl. loop) : 2.6 mm
- Max wire angle : 8^o
- Shortest wires for power supply pads

Status

- Design completed
- Submitted on April 28^{th} 2021
- Due to the radiation tolerant design, declared as dual use design
  - Countries of use : Germany, Italy
- Trade-off between power consumption and SEU protection to be evaluated.
- Other possible power consumption mitigation strategy :
  - Analog bias tuning
  - Digital supply voltage reduction to 1.08 V (or maybe 1 V).
- Power consumption estimate to be verified by tests.
- PCB design ready *(M. Mignone)*.
- First version of acquisition system ready *(R. Wheadon)*.