Detektor Technologie und System Platform: Säule 1: Technologien für hochintegrierte Detektoren

WP 3.1: 3D ASICS

Ulrich Trunk

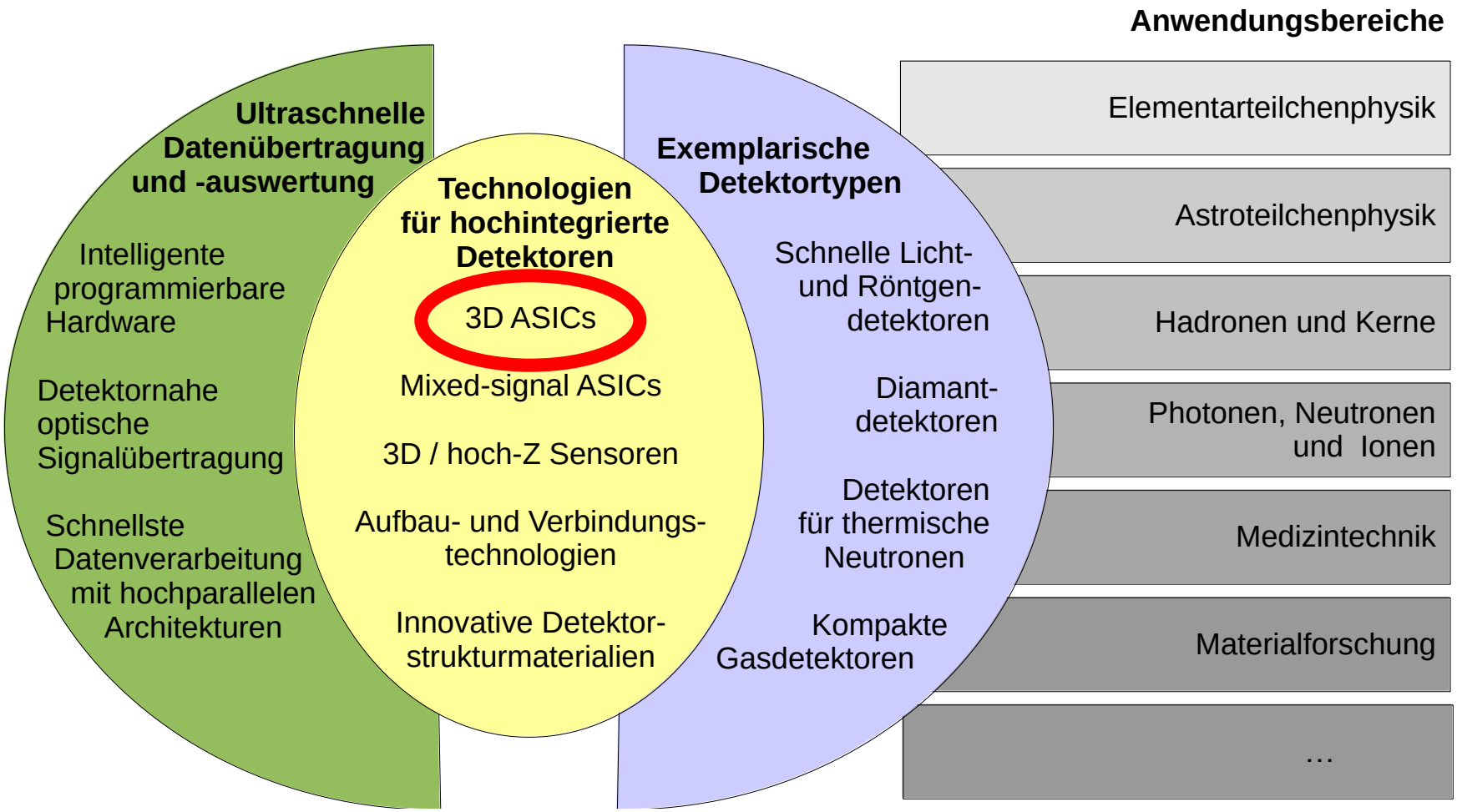
HGF Detector Portfolio Pillar 1 Meeting

DESY, 13-14 June 2012.

HELMHOLTZ GEMEINSCHAFT

DESY

Structure


Anwendungsbereiche
Ultraschnelle Datenübertragung und -auswertung
Intelligente programmierbare Hardware
Detektornahe optische Signalübertragung
Schnellste Datenverarbeitung mit hochparallelen Architekturen
Technologien für hochintegrierte Detektoren
3D ASICs
Mixed-signal ASICs
3D / hoch-Z Sensoren
Aufbau- und Verbindungs-technologien
Innovative Detektor-strukturmaterialien
Exemplarische Detektortypen
Schnelle Licht- und Röntgen-detektoren
Diamant-detektoren
Detektoren für thermische Neutronen
Kompakte Gasdetektoren
Elementarteilchenphysik
Astroteilchenphysik
Hadronen und Kerne
Photonen, Neutronen und Ionen
Medizintechnik
Materialforschung
…

Outline:
The „W(ish)“-List...

- Why 3D-ASICS?
- Where to start?
- What do we want to achieve?
- Who is part of the workpackage?
- Who else will (or could) participate?
- Which technologies and processes are available?
- Which one will we use?
- What is the context in „Pillar 1“ and the whole HGF Portfolio, and how can we gain from synergies?
- What is our goal, i.e. final Deliverable and how will we achieve it?

Why 3D-ASICS?

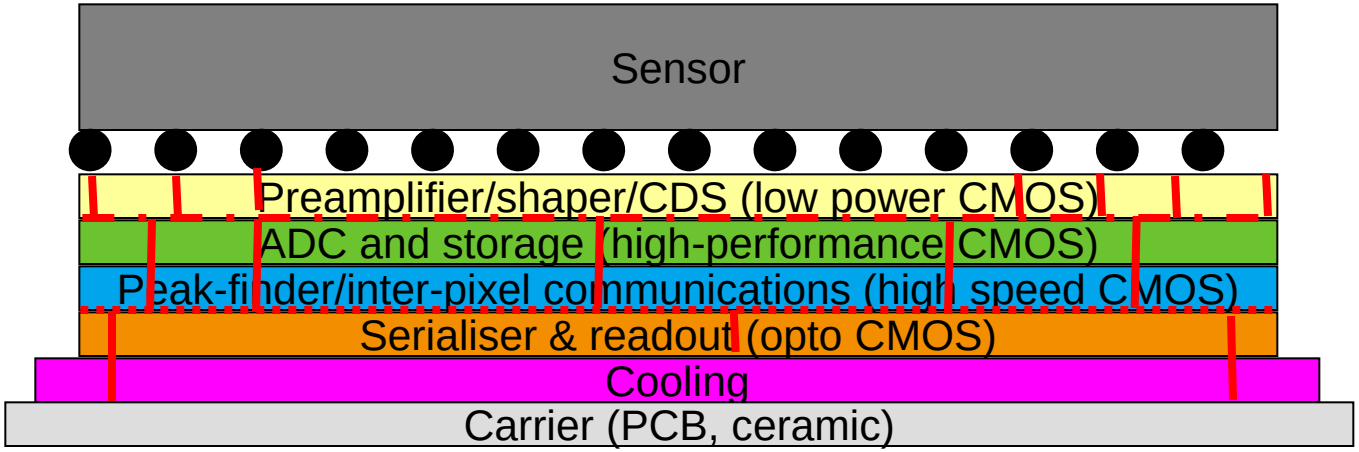
If you need to implement more circuit functionality in the same amount of chip area „real estate“* you can...

- use a smaller technology node
  - becomes very expensive
  - will have a negative impact on analogue circuits
- use 3D-integraton
  - TSVs
  - Wafer bonding
  - Limited availability

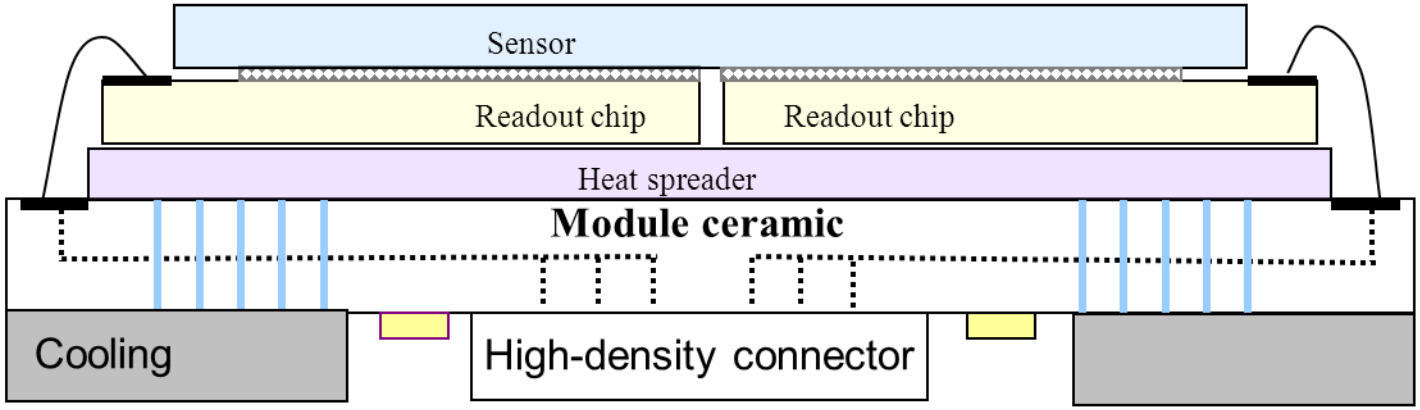
*this is the usual challenge for pixelated detectors –why not start here?

Why 3D-ASICS?

A hypothetical example....



Current State-of-the-art



Where to start?

Obviously with some existing pixel detector assembly...

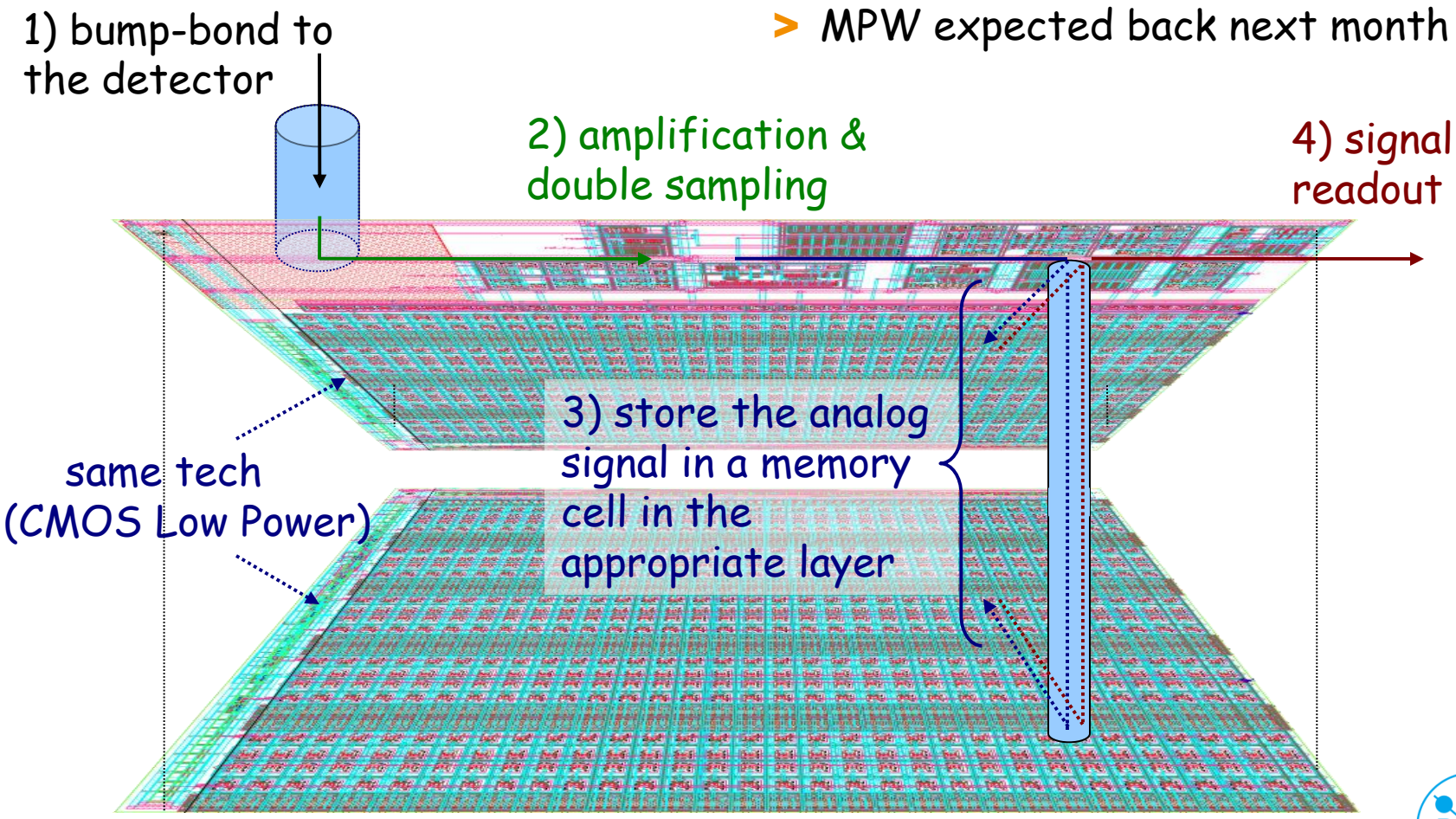
> AGIPD	Si, (Ge, GaAs)	PS	(DESY)
▪ AGIPD 3D evaluation			
> ATLAS Pixel	Si	HEP	(DESY)
> CBM Pixel	MAPS	HI	(GSI)
> Calice	Si, SiPMTs, MAPS	HEP	(DESY)
> CMS Pixel	Si	HEP	(DESY)
> LAMBDA/Medipix	Si, Ge, GaAs	PS	(DESY)
▪ Minapad (Single-Tier, Open-3D based assembly)			
> PANDA MVD/Topix	Si	HI	(GSI)
> .....many more....			

Choice should be based on our final goal.....

DESY

Disqualified as a goal due to an early start?

- Minapad
- AGIPD 3D evaluation



- MPW expected back next month

What do we want to achieve?

Enable any participating institution to produce 3D integrated circuits and detector assemblies by exploiting synergetic effects

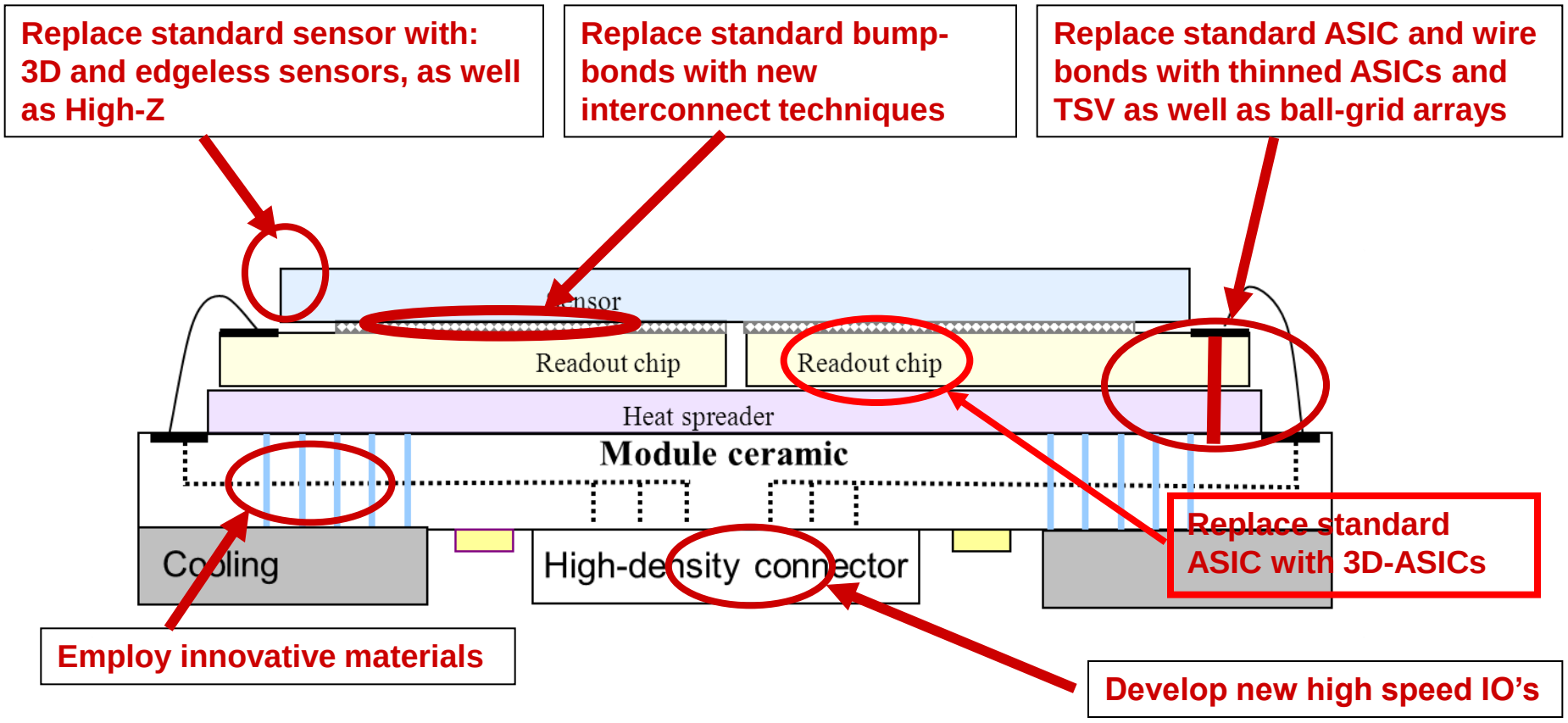
- among the participating Helmholtz-Centres and
- technologies coverd by the different workpackages:
  - WP1-3 mixed signal ASICs
  - WP1-4 high density interconnect
  - WP1-2 3D and high-Z sensors
  - WP1-5 novel materials

Stimulate spin-offs outside the pillar

- Tomographic dignostics of interconnects @ ANKA
- Integration of high-speed data transmission (Pillar 2)

Pillar 1 : The “Helmholtz-Cube”

Vertically Integrated Detector Technology



from Heinz Graafsma‘s presentation
at the kick-off meeting

Who is part of the workpackage?

Helmholtz-Centres:

- DESY
- FZJ
- KIT

Who else will (or could) participate?

External research centres:

- Fermi National Accelerator Laboratory (USA)
- IN2P3 Institut national de physique nucléaire et de physique des particules (France)
- Institut Pluridisciplinaire Hubert Curien, Strasbourg
- Laboratoire de l'Accélérateur Linéaire, Orsay
- Max-Planck-Institut für Physik, Munich
- Paul Scherrer Institut, Villigen (Switzerland)
- Science and Technology Facilities Council, STFC Technology, RAL, Harwell Oxford (UK)

University groups:

- AGH University of Science and Technology, Krakow,
- Albert-Ludwigs-Universität Freiburg,
- RWTH Aachen,
- Technische Universität Dresden,
- Universitätsklinkum Carl Gustav Carus, Dresden
- Universität Augsburg,
- Universität Bonn,
- INFN Florence,
- Universität Hamburg,
- Universität Heidelberg,
- Universität Wuppertal

Other possible technology partners?

External partners:

- Fraunhofer IZM
- CERN
- NIKHEF (NL)
- VTT (FI)

Which technologies and processes are available?

Full 3D integration:

- CEA-LETI Open-3D (TSVs, microbump bonding
  - CEA
- IMEC ?
- MIT Lincoln Lab
- Tezzaron FaStack (TSVs, wafer bonding)
  - MOSIS, CMP, FNAL

TSVs (Thru-Silicon Vias):

- Fraunhofer IZM / IST / EMFT / ENAS
- IBM (Micron/?)
- AMS (?)
- VTT (eniac/KET bridge)
- ST (eniac/KET bridge)

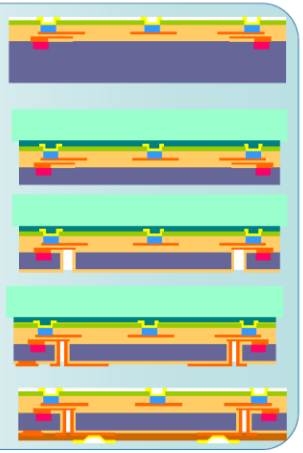
Bump-bonding:

- Fraunhofer IZM / IST / EMFT
- Ziptronix
- ....

Which one to use?

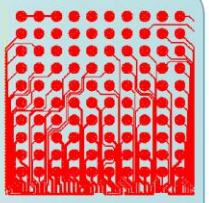
Process Flow description: TSV last technology

- Front Side Under Bump Metallization
- Temporary bonding and thinning
- Through Silicon Via patterning
- Redistribution Layer patterning
- Passivation and backside Under Bump Metallization
- Debonding

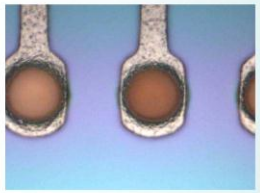


Back Side signal redistribution

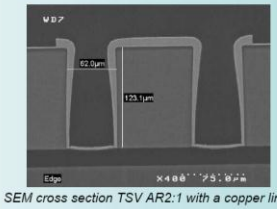
- Barrier and Seed layer deposition (PVD)
- RDL lithography step:
  - Negative dry film resist
  - Alignment on TSV level
- Cu electrodeposition step / Liner deposition into the TSV
- Seed layer etching



Design of RDL level



Optical view of the RDL lines below the TSV

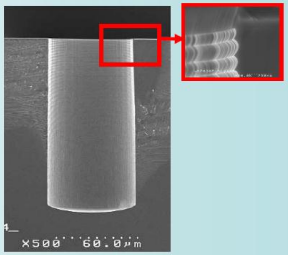


SEM cross section TSV AR2:1 with a copper liner

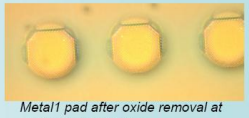
Main drawback: TSV size 60µm Ø

Through Silicon Via (TSV) process

- TSV lithography step:
  - Double side step (Font side / back side alignment)
  - Via Diameter=60µm
- DRIE Bosch 120µm Silicon etch:
  - Etch rate~ 7.5µm/min
  - Low undercut
  - Slope = 90°
- Passivation oxide deposition
  - Temperature limited to 200°C
  - Step coverage = 20%
- Etch back: removal of the oxide layer at the bottom of the cavity



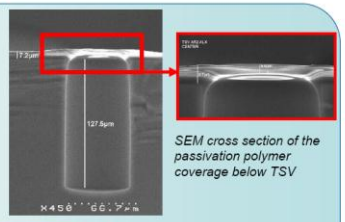
SEM cross section of 120µm TSV DRIE etched



Metal1 pad after oxide removal at the bottom of the via

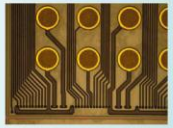
Passivation and Under Bump Metallization

- Passivation of copper lines:
  - Spin-on photosensitive polymer layer
  - Alignment on RDL level



SEM cross section of the passivation polymer coverage below TSV

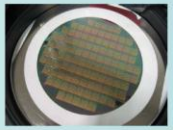
- Under Bump Metallization :
  - UBM deposition
  - Patterning



Optical view of the back side UBMc

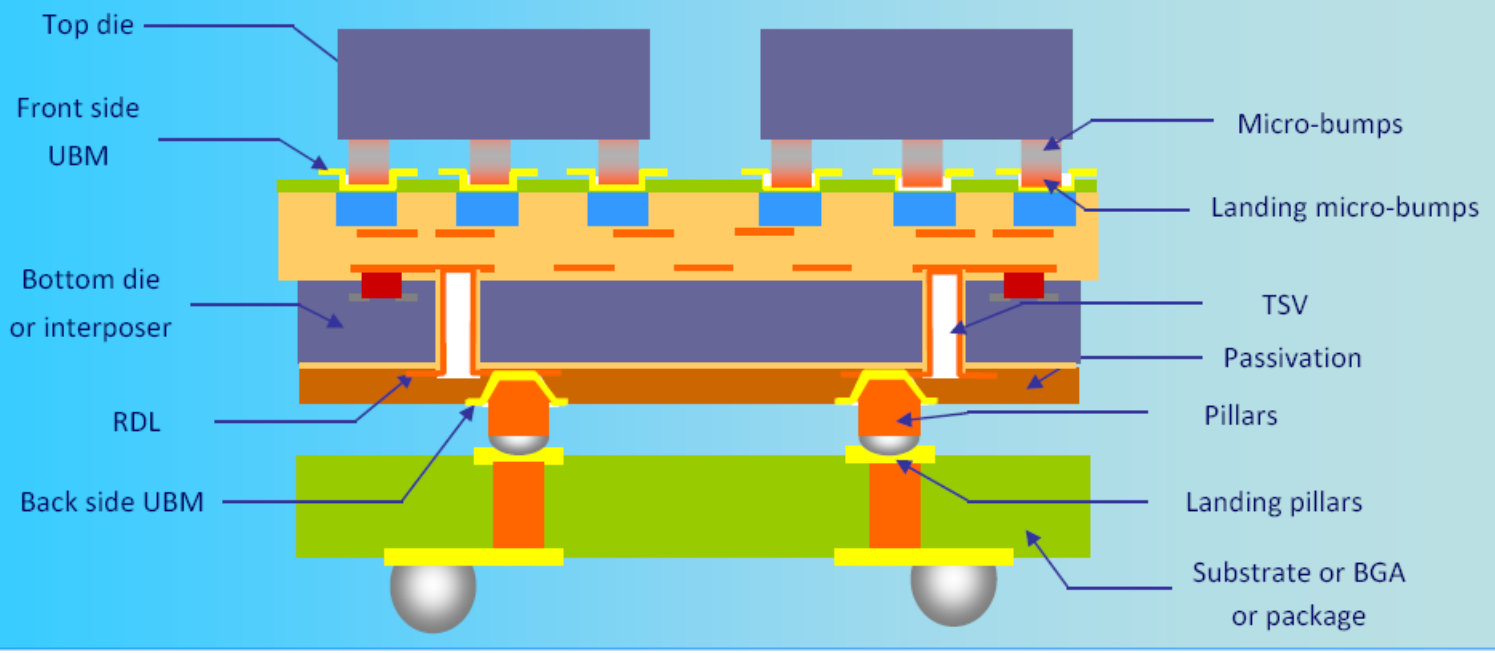
- Debonding from the glass carrier:
  - Slide-off technique

120µm thick debonded wafer



Open 3D™ technological offer

- **Technological modules définitions :**
  - TSV
  - RDL
  - UBM
  - Interconnections
  - Stacking
  - Packaging with partner collaboration

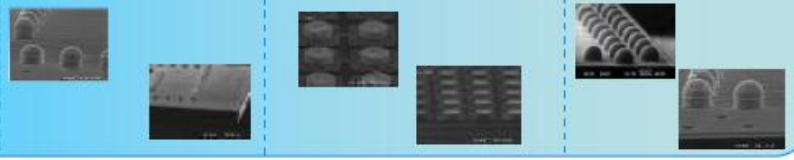


Open 3D™ technological offer

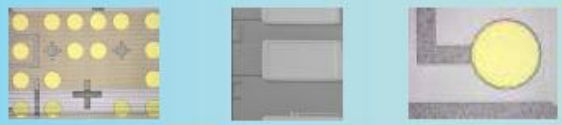
Technological modules

- **TSV Last**
  - AR 1:1
  - AR 2:1
  - AR 3:1

- **Interconnections**
  - Micro-bumps
  - Landing micro-bumps
  - Pillars



- **Under Bump Metallurgy (UBM)**

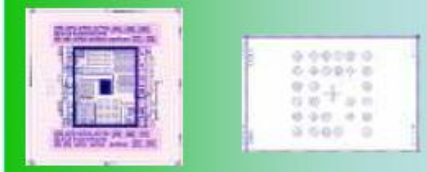


- **Redistribution layer (RDL)**

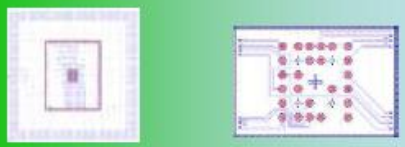
- **Stacking : D2W**

DRM / DK / layout / masks

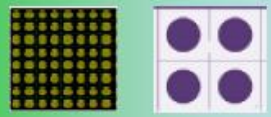
TSV



Interconnections

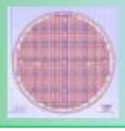


UBM



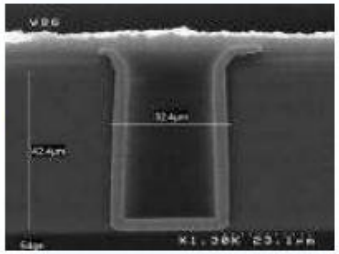
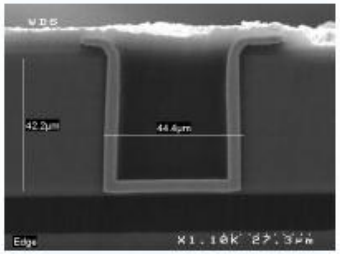
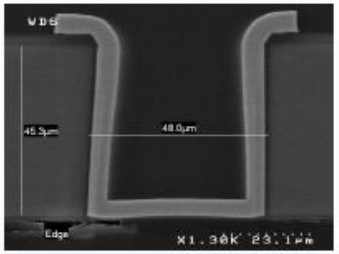
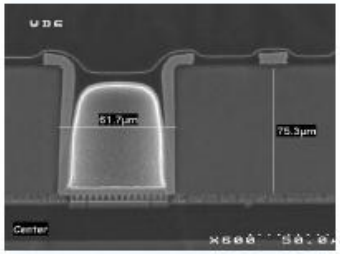
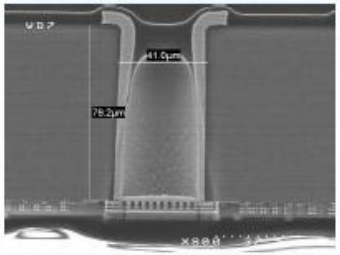
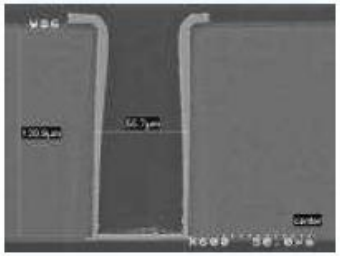
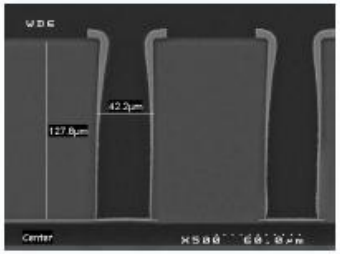
RDL

Stacking



Open 3D™ technological offer / TSV

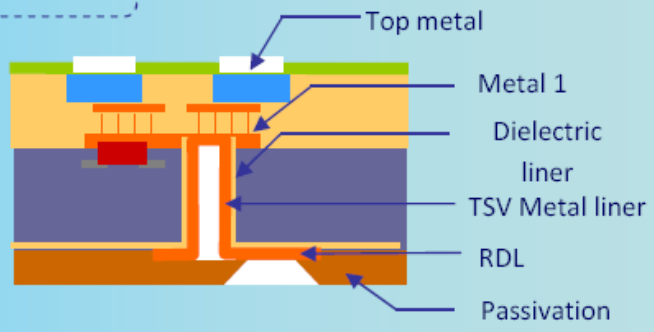
TSV Gallery

TSV diameter	30 µm	40 µm	50 µm	60 µm
AR 1:1 & 1.5:1				
AR 2:1	Not yet demonstrated		Available Not yet required	
AR 3:1	Not yet demonstrated		Available Not yet required	Not yet demonstrated

Open 3D™ technological offer / TSV

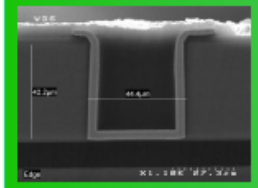
TSV DRM & schematic

- Wafer size : **200 & 300 mm**
- TSV type : **via last / Cu liner**
- Minimum pitch : **80 µm (for 40µm TSV)**
- TSV diameter : **30 to 100 µm**
- Aspect Ratio (AR) : **from 1:1 to 3:1**

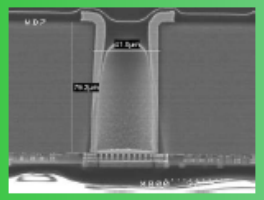


TSV morphological & electrical results

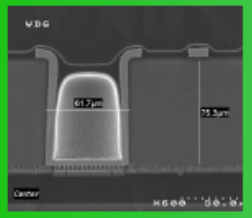
AR 1:1

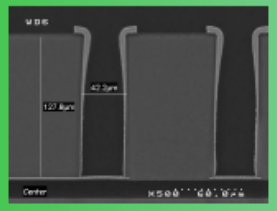


AR 2:1



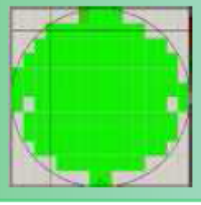
AR 3:1



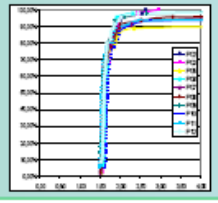


TSV characteristics

TSV geometry	R (mΩ)	C (pF)	Elec. Yield	Insul. (MΩ)	I_{leak} (A)
$TSV_{60/80}$	15.1	0.57	100 %	> 100	-
$TSV_{60/120}$	19.1	0.82	100 %	> 100	$1.3\ 10^{-9}$ @ 10V $3.1\ 10^{-9}$ @ 50V
$TSV_{40/80}$	20.1	0.46	> 99%	> 100	-
$TSV_{40/120}$	30.4	0.63	> 99%	> 100	$7.4\ 10^{-9}$



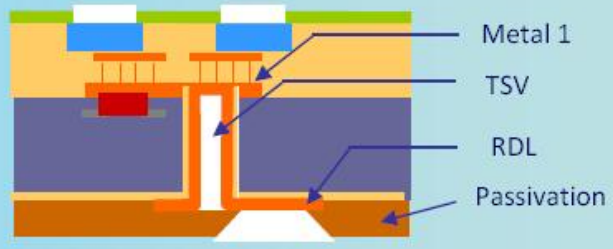
Electrical tests results



Open 3D™ technological offer / RDL

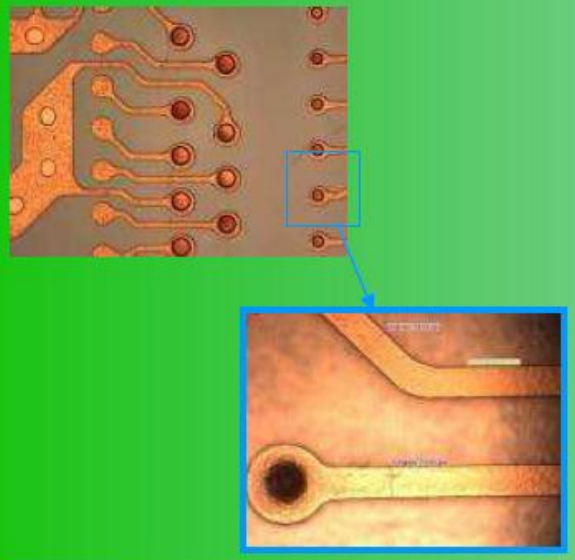
RDL DRM & schematic

- Wafer size : **200 & 300 mm**
- RDL material : **Cu / protective layer possible**
- RDL thickness : **1-10 µm**
- RDL minimun width : **20 µm**
- RDL minimun space : **20 µm**



RDL Morphological & electrical results

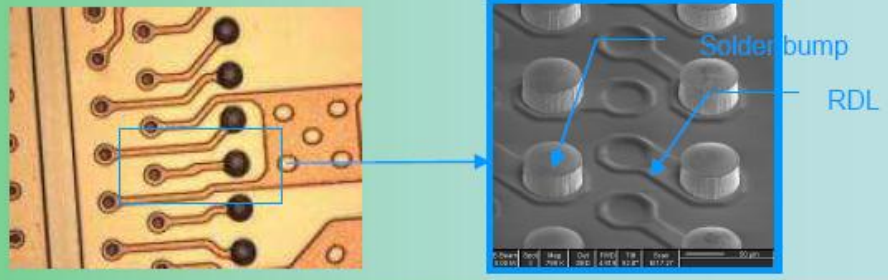
Backside Cu RDL



RDL characteristics

	Insolation between lines	I_{leak} @ 10V (A)	Elec. Yield
RDL	> 6.0 GΩ	$1.6\ 10^{-9}$	100 %

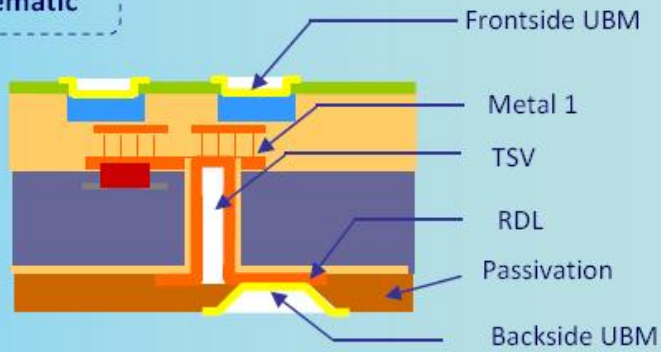
Cu RDL integration : Solder bumps on RDL + passivation



Open 3D™ technological offer / UBM

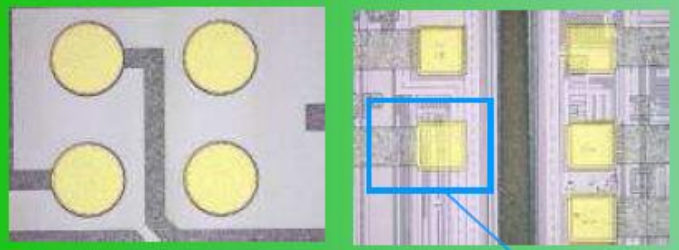
UBM DRM & schematic

- Wafer size : **200 & 300 mm**
- UBM material : **TiNiAu**
- UBM thickness : **0.5 – 10 µm**
- UBM width : **20 – 800 µm**
- UBM minimun pitch : **40 µm – 1.6 mm**



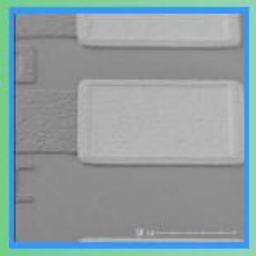
UBM Morphological & electrical results

Backside and frontside UBM possible



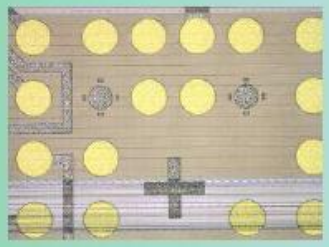
Different shape possible :

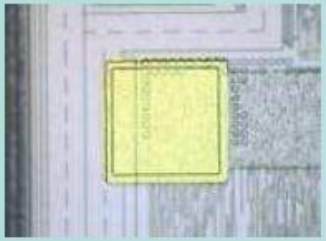
- Square
- Polygons
- Circle



Two possible technologies :

- Metal sputtering / thickness range : 0.5 – 1 µm
- ECD / thickness range : 1 – 10 µm

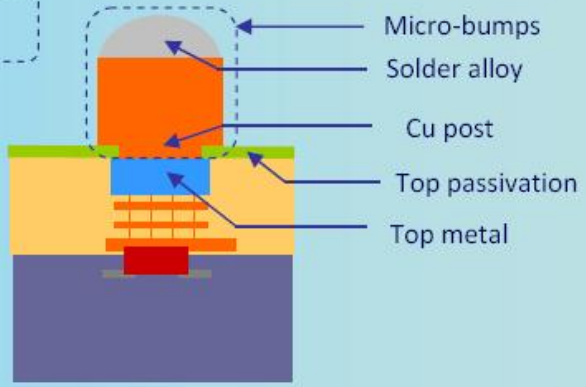




Open 3D™ technological offer / Micro-bumps

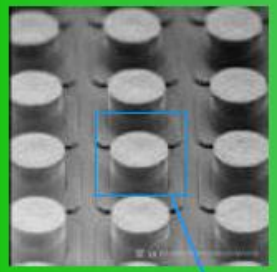
Micro-bumps DRM & schematic

- Wafer size : **200 & 300 mm**
- Micro-bumps material : **Cu post / SnAg solder**
- Minimum pitch : **50 µm**
- Micro-bumps diameter : **25 µm**
- Micro-bumps thickness : **25 – 35 µm**

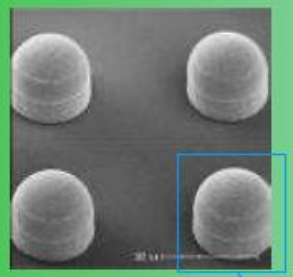


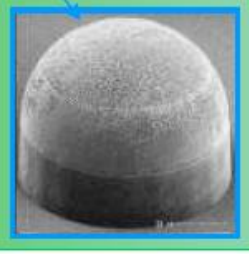
Micro-bumps Morphological & electrical results

Micro-bumps before reflow

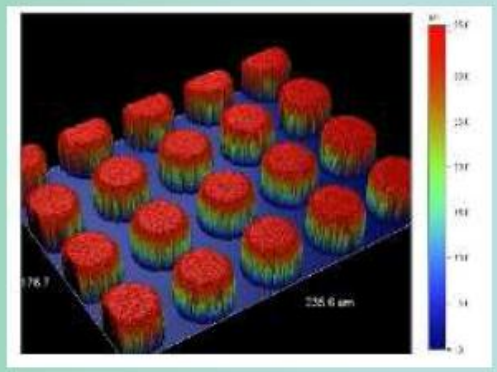


Micro-bumps after reflow





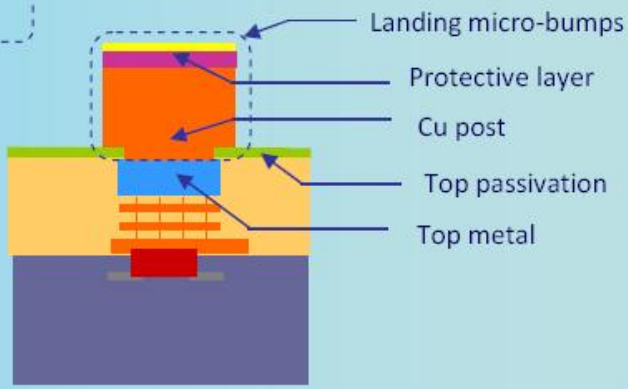
Micro-bumps characterization



Open 3D™ technological offer / Landing micro-bumps

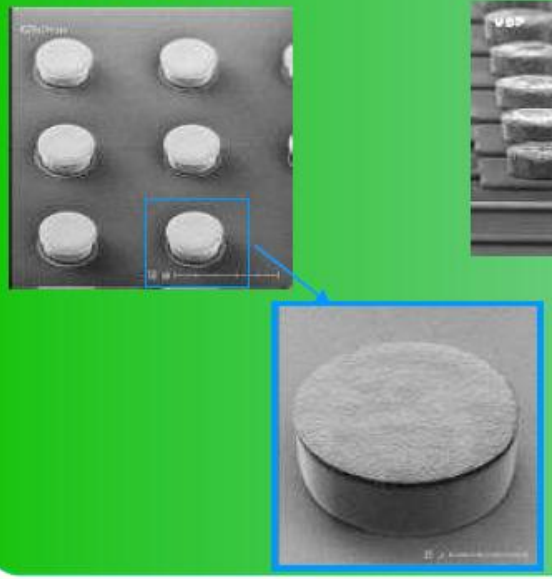
Landing micro-bumps DRM & schematic

- Wafer size : **200 & 300 mm**
- Landing micro-bumps material : **Cu post / NiAu protection possible**
- Minimum pitch : **50 µm**
- Landing micro-bumps diameter : **25 µm**
- Landing micro-bumps thickness : **8 – 12 µm**

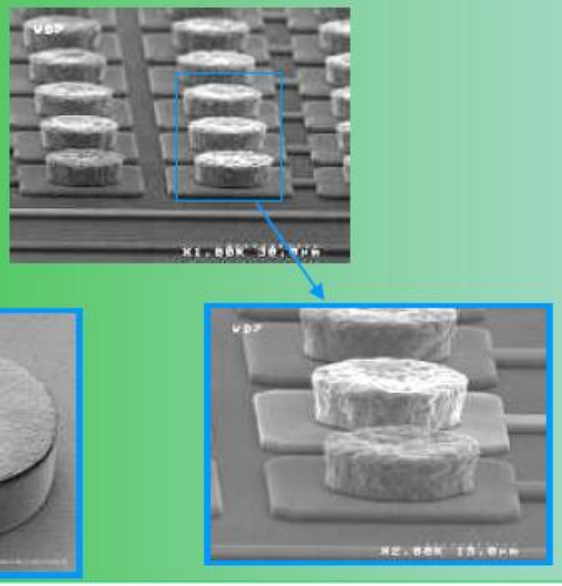


Landing micro-bumps Morphological & electrical results

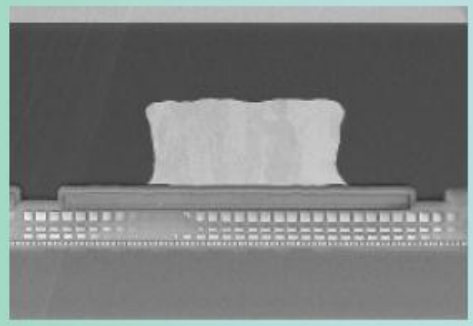
Landing micro-bumps with protective layer



Landing micro-bumps w/o protective layer



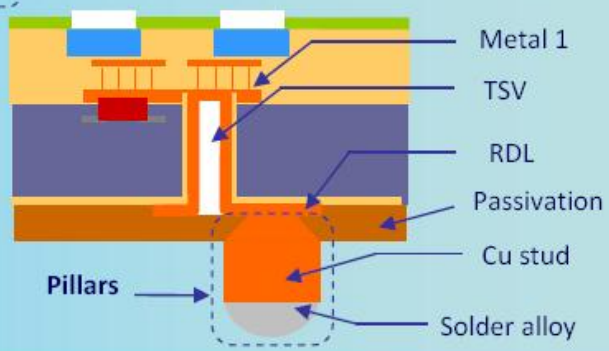
Landing micro-bumps on top metal



Open 3D™ technological offer / Pillars

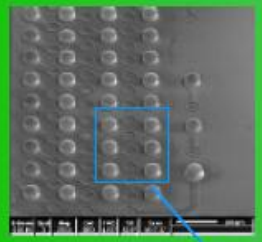
Pillars DRM & schematic

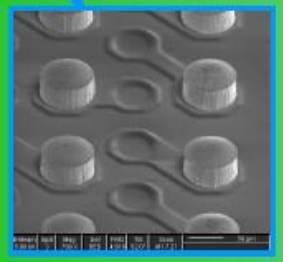
- Wafer size : **200 & 300 mm**
- Pillars material : **Cu stud / SnAg solder**
- Minimum pitch : **120 µm**
- Pillars diameter : **60 – 80 µm**
- Pillars thickness : **60 – 80 µm**



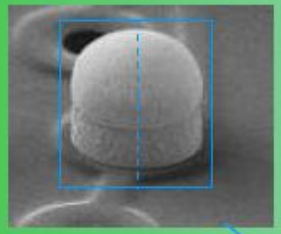
Pillars Morphological & electrical results

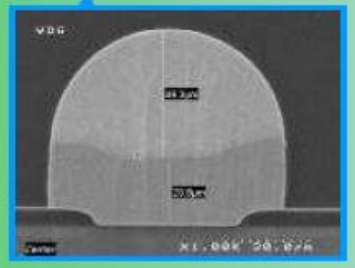
Pillars





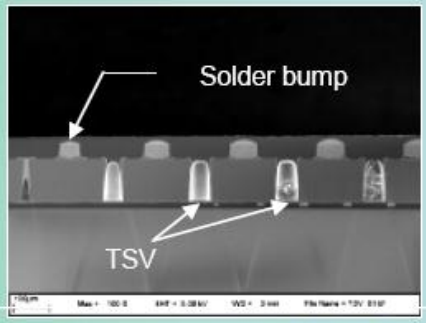
Pillars cross section





Pillars characteristics

	R (mΩ)	Elec. Yield
Pillars	50	100 %



Pillars integration with TSV

Tezzaron FaStack

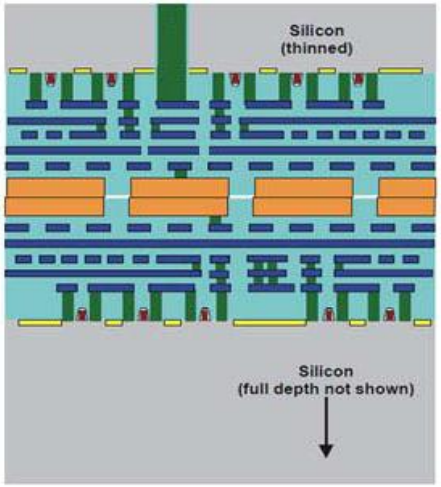
Products :: IC's Manufacturing :: **CMOS 130nm FaStack(R)**

TECHNOLOGY:	
CMOS 130nm FaStack (3D-IC Integration)	
Met. layer(s):	6 per Tier (Metal 6 is used as bond interface) + TSV (Through Silicon Via)
Poly layer(s):	1
Maximum die size:	2cm x 2cm
Usable cells:	535 digital cells in both Low Power Low VT and Low Power Std VT
Available I/O:	I/O cell library with digital pads is available for 1.2V/1.5V core 3.3V I/O, 5.0V Tolerant
Temp. range:	-40° C. / +125° C.
Supply voltage:	1.2V/1.5V core 3.3V I/O, 5.0V Tolerant
SPECIAL FEATURES:	High performance mixed analog/digital process. Two Tiers bonded face-to-face
APPLICATION AREA:	Mixed Signals analog/digital, Pixels Arrays, Large Digital Designs, System on Chip
LIBRARIES:	Digital cells: All the standard digital cells plus composed cells (complex gates, arithmetic cells, register files,...).
Megacells:	Single Port RAM, Double Port RAM, ROM.
RAM/DP-RAM/ROM:	Memory Compilers.
DESIGN KITS:	
Unix based:	CADENCE, SYNOPSYS, MENTOR, MicroMagic
Windows based:	none
PACKAGING:	All standard packages (DIL, LCC, PGA,...).
TEST:	Contact CMP
INTERFACE FORMAT:	GDSII, CADENCE
SPICE parameters:	SPECTRE, HSPICE, ELDO
DRC, ERC rule set:	Calibre DRC/LVS/3DLVS/PEX, Assura LVS/QRC, Hercules
DESIGN SUPPORT:	DRC checking (free for submitted designs)
PRICES:	
Cell libraries:	Distributed under NDA
Design kits:	Distributed under NDA
Prototyping:	See the general CMP price list for prototyping
Low volume production:	Depends on each specific case; contact CMP
TURNAROUND TIME:	Typical: TBD

Main drawback:

Turn-around delays of

0.5a ... 2a



Tezzaron FaStack

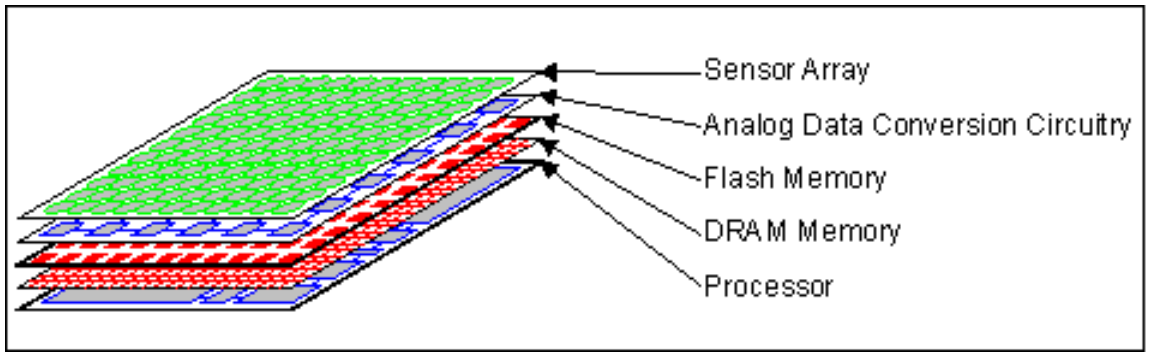
Commercial from Tezzarons web site....

FaStack® Creates 3D Integrated Circuits (3D-ICs)

Tezzaron's groundbreaking FaStack technology creates fast, dense, highly integrated 3D chips. The heart of the process is wafer-level stacking. Device circuitry is divided into sections that are built on separate wafers using standard processing. Hundreds of thousands of vertical "Super-Contact™" connectors are built into the wafers. Finished wafers are metallized with a proprietary bonding pattern. They are then aligned with a precision of 0.5 micron, bonded, and thinned. Additional wafers may be bonded and thinned in turn. The finished stack is diced into individual 3D-IC devices.

Wafer Stacking

Wafer Stacked SoC (proposed)

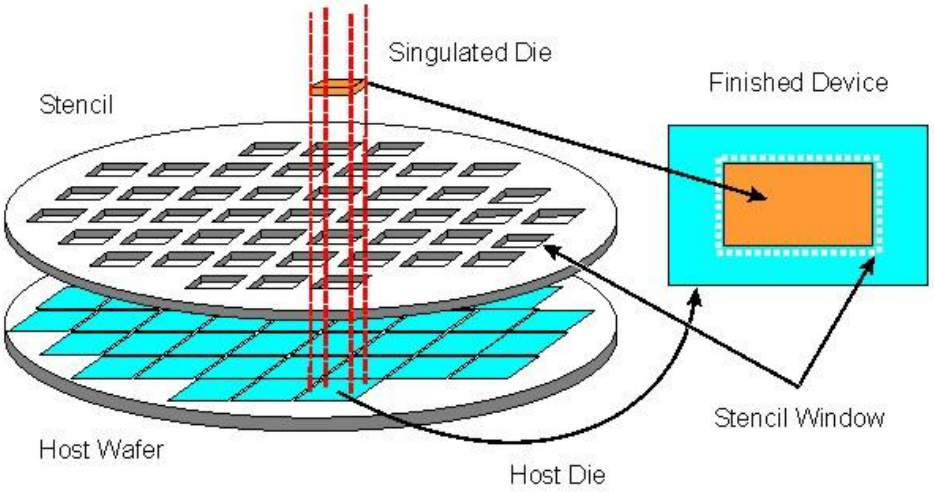


Tezzaron FaStack

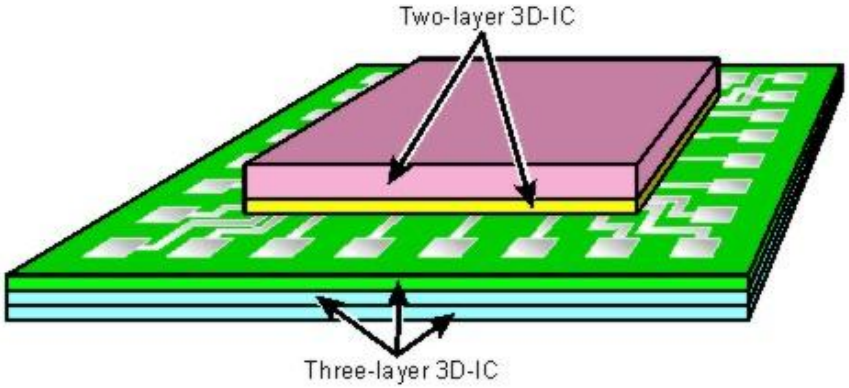
Commercial from Tezzarons web site....

A variation on the FaStack process stacks individual dies onto an uncut wafer that is then diced into 3D-ICs. The dies may themselves be FaStack 3D-ICs, and the uncut wafer may be a FaStack wafer stack; this "stack of stacks" scenario allows for extremely flexible integration projects.

Die-on-Wafer Stacking



Hyper-Integrated Stack of Stacks (in progress)



A Superior Technology

FaStack devices have many advantages over their single-layer counterparts. They are much more dense and their short vertical interconnects allow them to operate at higher speeds with a lower power budget. In addition, FaStack allows disparate elements to be processed on separate wafers for simpler production and greater optimization.

Unlike the separate chips in a "System-in-Package" (SiP) component, FaStack layers are fully integrated into a single IC by a dense system of through-silicon interconnects. FaStack devices match the tight integration of SoC devices while out-doing SiPs for high speed, low power budget, and tiny footprint.

Although other 3D-IC technologies exist, FaStack offers several important benefits:

> No exotic process requirements
> Extremely high interconnect density
> High-precision alignment
> Low-stress tungsten TSV for reduced thermal mismatch
> No thin-wafer handling requirements
> Extreme thinning allows 3D-ICs to fit in standard packaging
> Real working devices since 2004 - with **no** failures to date!

Tezzaron FaStack

More commercials....

Applications for FaStack®
FaStack's wafer stacking offers benefits to a variety of applications. Sensor arrays, for example, achieve unprecedented density by moving the support circuitry to a different layer than the sensors themselves. "System-on-Chip" (SoC) devices built with FaStack reduce power consumption, footprint, and interconnect delays. Microprocessors built with FaStack incorporate a huge, fast memory cache on a separate layer. FaStack also enables enormous improvements in **memory technology** **and allows seamless integration of differing process technologies. As 3D-ICs move into the mainstream, entirely new products will emerge to capitalize on this technology.**

Getting the FaStack® Advantage
Tezzaron is currently exploiting the benefits of FaStack in three ways:

1) joint development projects with technology partners and systems designers,

2) licensing the production technology to manufacturers, and

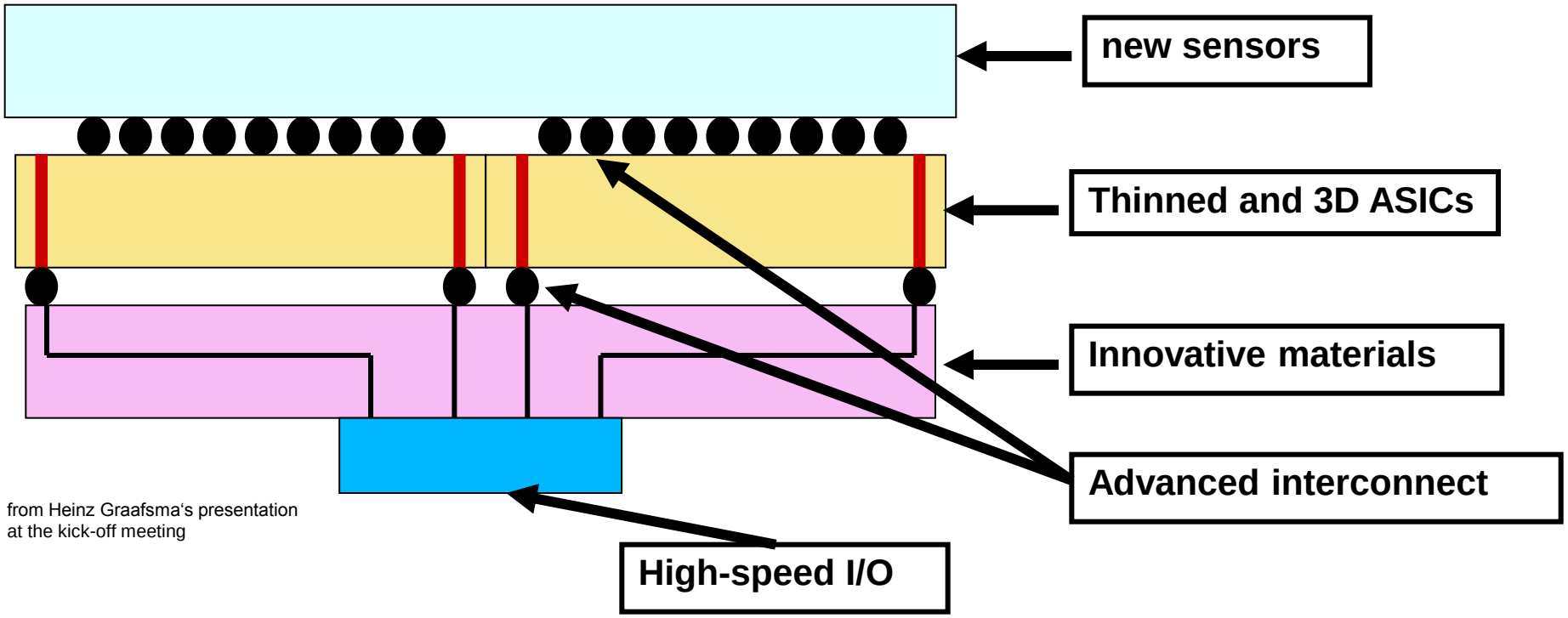
3) producing our own FaStack-based products.

Gaining from synergies?

In the context of WP1 we could (and should) make use of:

- Mixed-signal ASICS (P1 WP2)
- „Aufbau und Verbindungstechnologien“ (P1 WP4)
- „Innovative Detektorstruskturmaterialien“ (P1 WP5)
- „Detektornahe optische Signalübertragung“ (P2 WP3)
- 3D- und „high-Z“ sensors (P1 WP3)

Pillar 1: The “Helmholtz-Cube”



from Heinz Graafsma‘s presentation
at the kick-off meeting

What is our final goal, and how will we achieve it?

Proposal:

A 3D-integrated pixel readout ASIC which should be usable as a...

- Calorimeter readout in HEP
  - trigger capability
- Tracker Readout in HEP and HI
  - low radiation length
  - trigger capability
  - analogue information
- Imager Readout in PS
  - photon counting
  - charge integrating analogue information

Outlook (i.e. my personal perspective of it)

If you want to grow fruits in different fields,

plant a strong tree now!