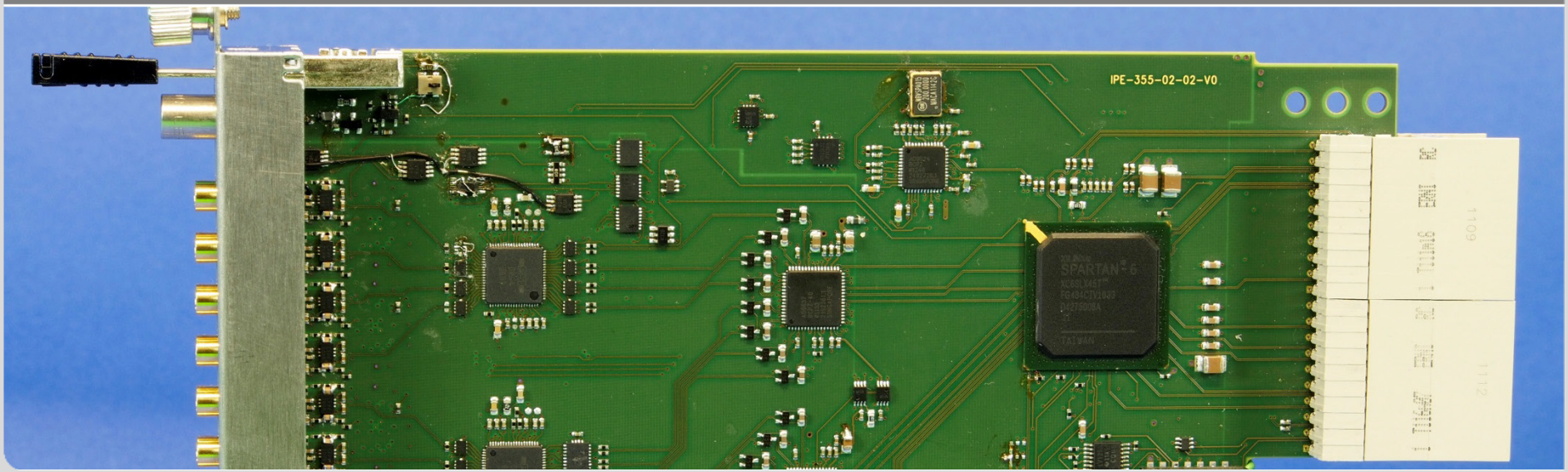
Karlsruhe Institute of Technology

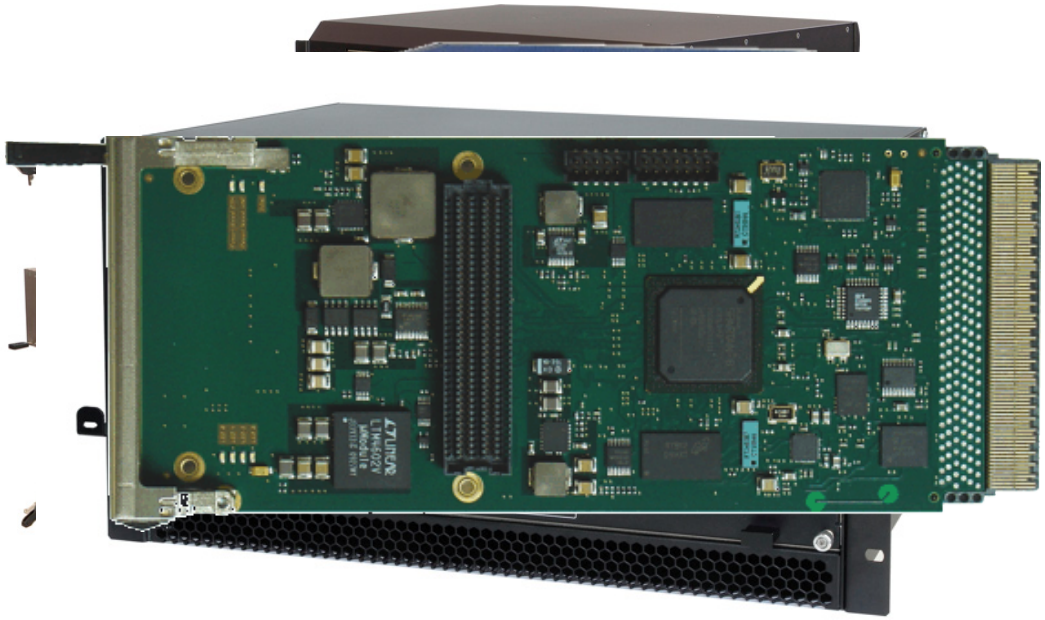
MTCA.4 a New Standard for Data Acquisition Systems

Institute for Data Processing and Electronics (IPE)



Telecommunication Computing Architecture (TCA)

- History of MTCA.4
  - ATCA Advanced Telecommunication Computing Architecture
  - AMC Advanced Mezzanine Card
  - MicroTCA
  - MTCA.4 (PICMG Standard)



MTCA.4 System

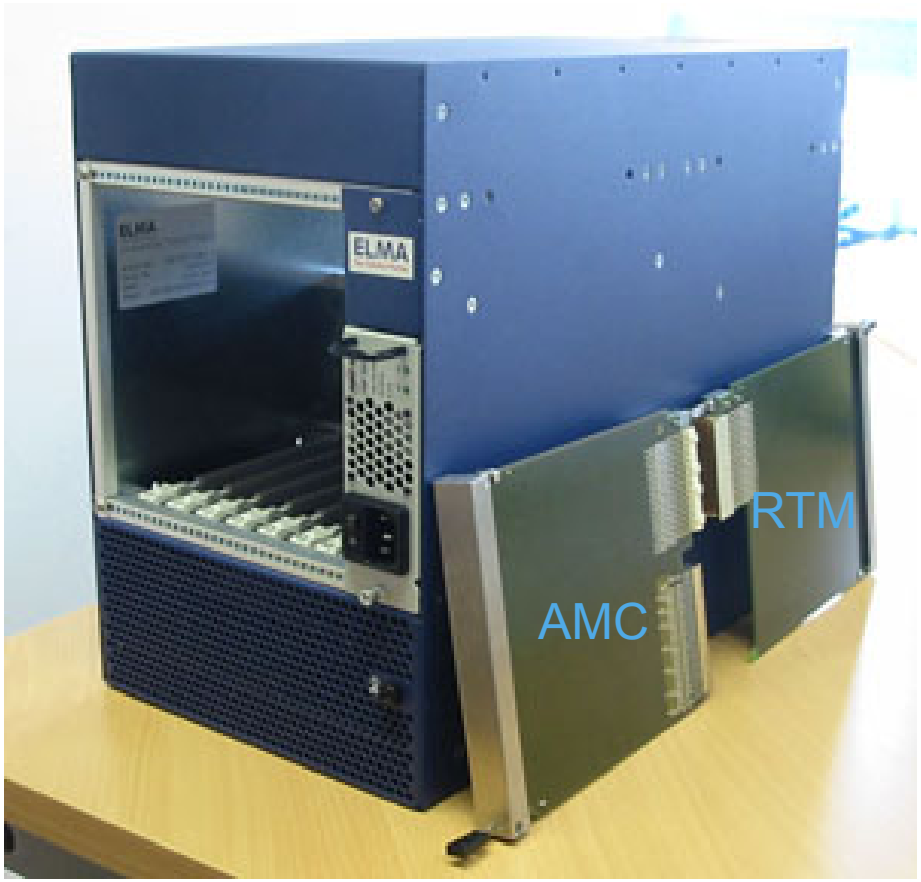
- Crate
- Power Modules

- MicroTCA Carrier Hub (MCH)

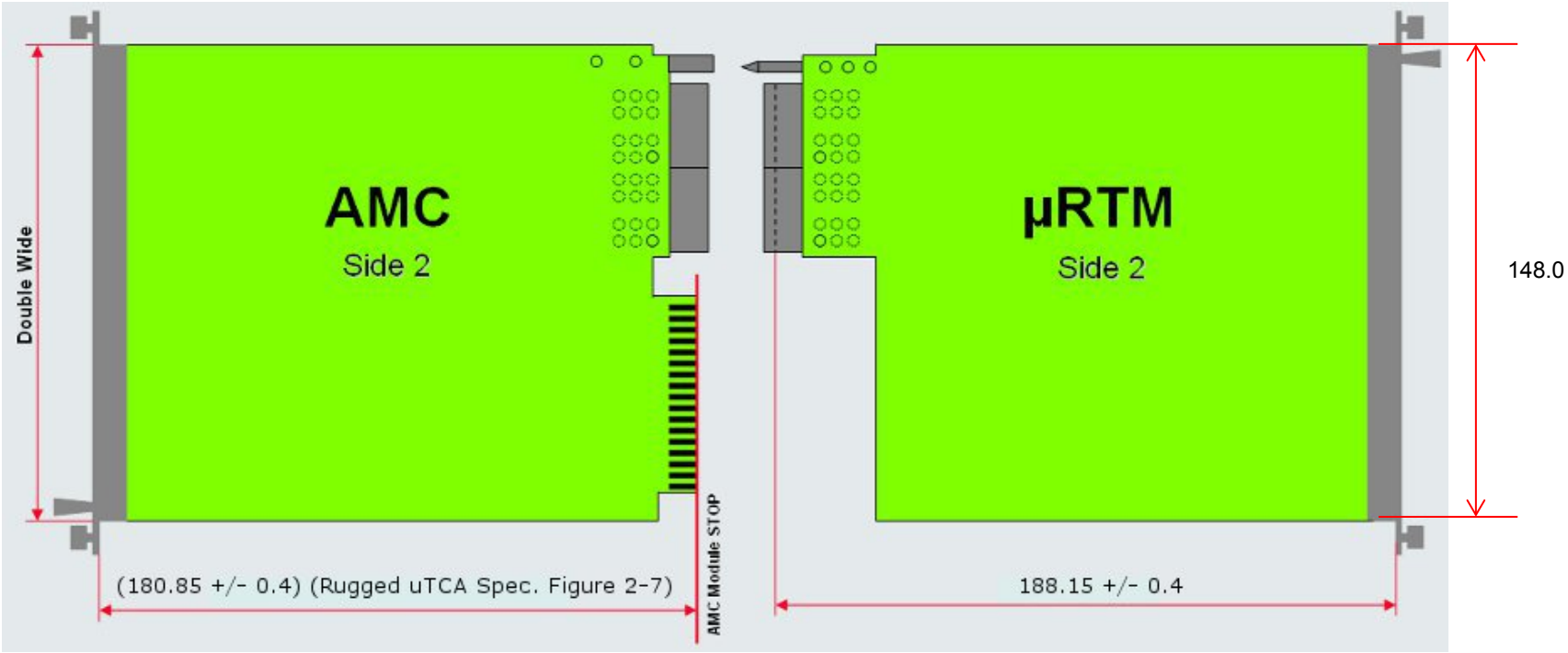
- AMC Board
  General Purpose Board
  Processor, DSP, FPGA

- Rear Transition Module (RTM)
  Rear I/Os
  Signal Conditioning
  Custuom Adaption

- Crate Control (IPMI Protocol)



MTCA.4 Board Dimensions

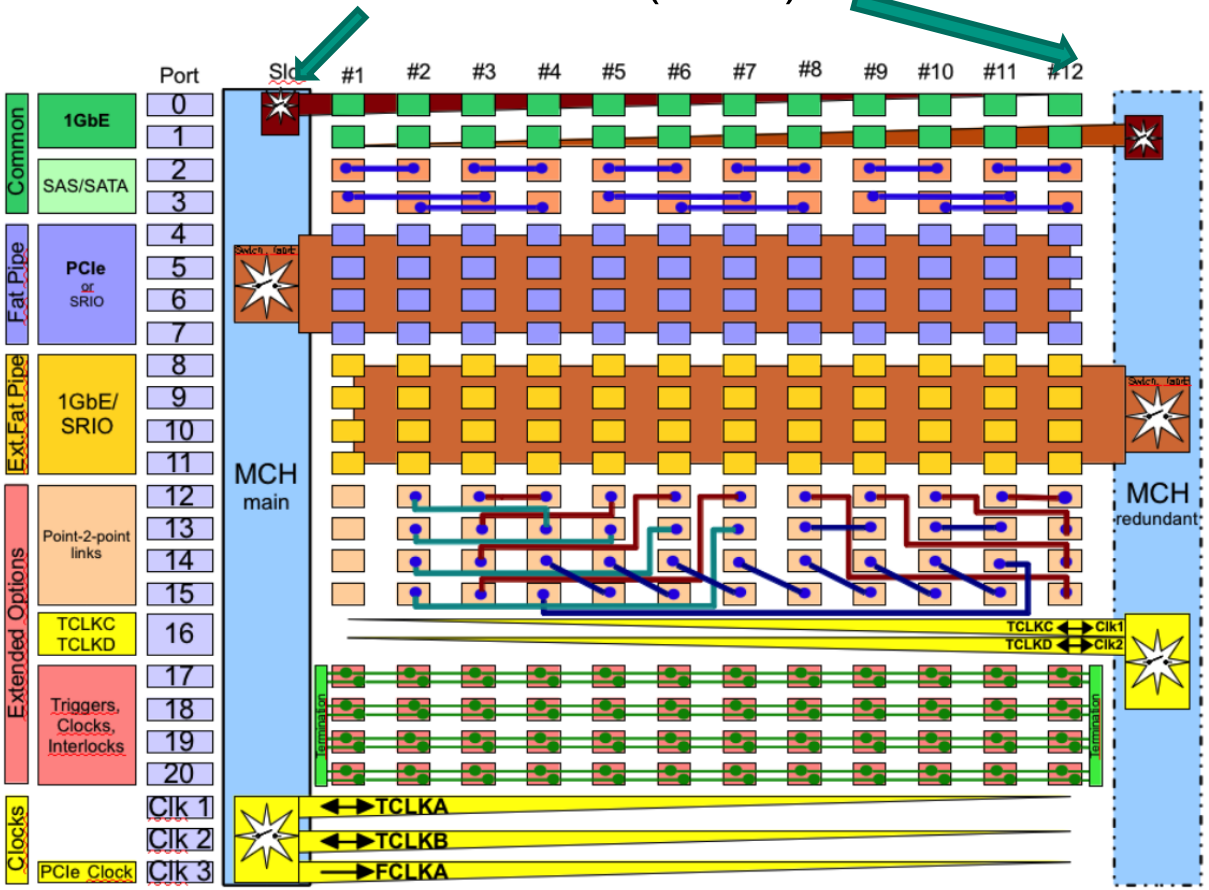


Picture by Schroff

MTCA.4 Backplane

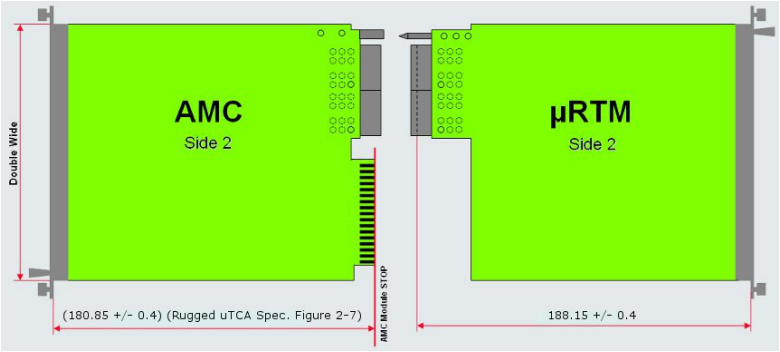
- 12 Slots
- 1 GbE
- PCIe Gen2(3) x4
- P2P Connections
- Trigger Lines
- CLKs

Redundant MicroTCA Carrier Hub (MCH)



RTM Specification

- Power 30W
- Zone 3 Connector
- Different definition available depending on application (analog and digital)
  - Class A1.1
  - Class A2.1
  - **Class D1.0 42 LVDS, 2 HS links**
  - …
  - Class D1.4 8 LVDS, 16 HS links

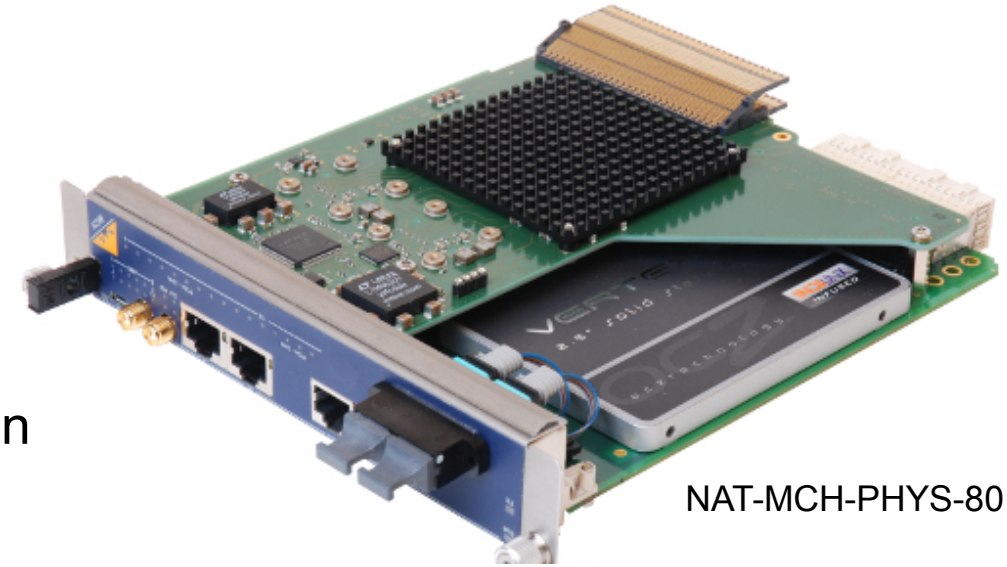


		A	B	C	D	E	F
J30	1	RTM_PWR	RTM_PWR	RTM_PS#	RTM_SDA	RTM_TCK	RTM_TDO
	2	RTM_PWR	RTM_PWR	RTM_MP	RTM_SCL	RTM_TDI	RTM_TMS
	3	CLK0_A2R+	CLK0_A2R-	CLK0_R2A+	CLK0_R2A-		
	4					B2	B2
	5	B2_cc	B2_cc	B2_cc	B2_cc	B2_cc	B2_cc
	6	B2	B2	B2	B2	B2	B2
	7	BR	B2	B2	B2	B2	B2
	8	BR	B2	B2	B2	B2	B2
	9	B2	B2	B2	B2	B2	B2
	10	B2	B2	B2	B2	B2_cc	B2_cc
J31	1	B1	B1	B1	B1	B1_cc	B1_cc
	2	B1	B1	B1	B1	B1_cc	B1_cc
	3	B1	B1	B1	B1	B1	B1
	4	B1	B1	B1	B1	B1	B1
	5	B1	B1	B1	B1	B1	B1
	6	B1	B1	B1	B1	B1	B1
	7						
	8						
	9	RCLK2_R2A+	RCLK2_R2A-	GL2_R2A+	GL2_R2A-	GL2_A2R+	GL2_A2R-
	10	RCLK1_R2A+	RCLK1_R2A-	GL1_R2A+	GL1_R2A-	GL1_A2R+	GL1_A2R-

LVDS or LVCMOS2V5 input/output
LVDS input or LVCMOS input/output
LVCMOS2V5 input/output

MicroTCA Carrier Hub (MCH)

- Hub Functionality
  - PCIe Gen3 x4
  - 1Gbit Ethernet
- Optical PCIe
  Uplink or Crate Interconnection
- Optinal SSD Storage
- RTM-RF-COMex-i7Q



NAT-MCH-PHYS-80

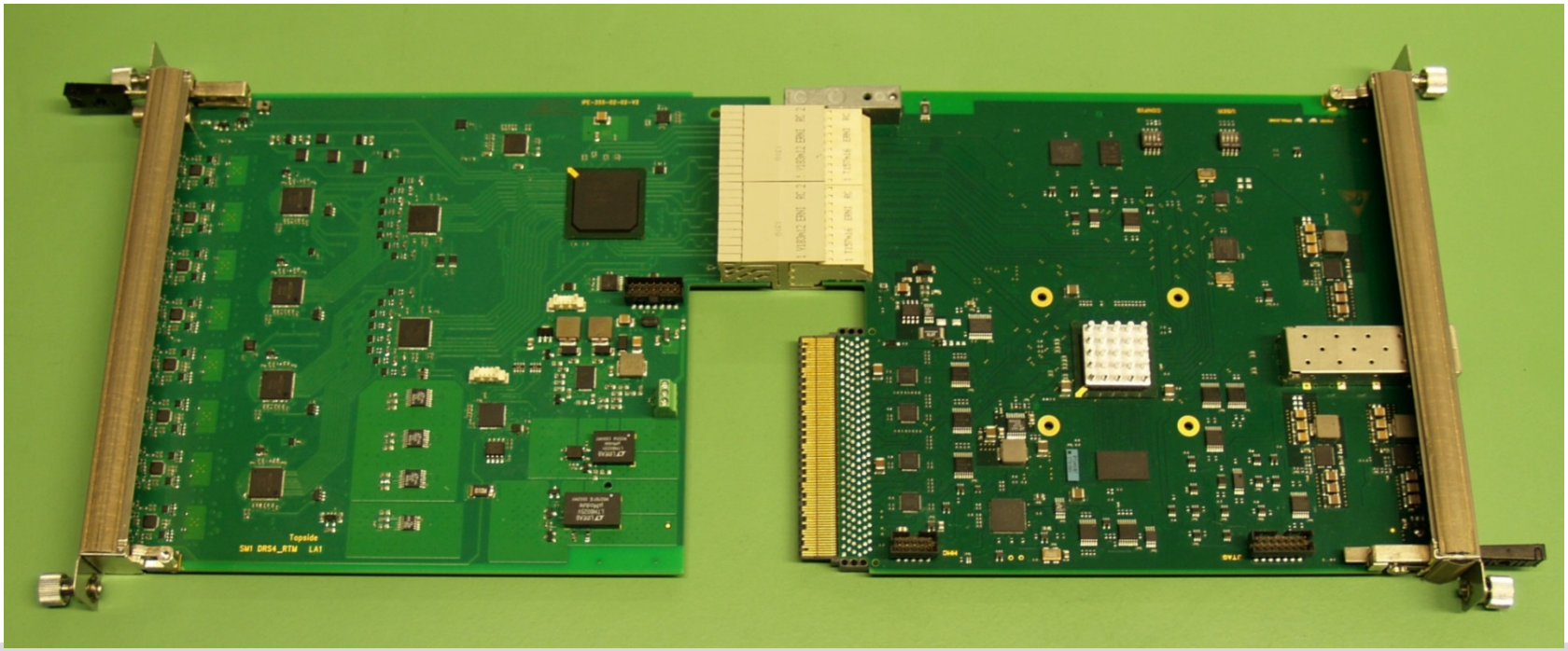
NAT-MCH-RTM-RF

MTCA.4 Activities at KIT

- Evaluation and Development of Hardware and Firmware
- Hardware Development RTM-DRS4 and RTM-32ADC
- Common Development of HGF-AMC Board with DESY
- EURECA: Muon Veto
- Ultrasound Computer Tomograph (USCT)
- FLUTE (LinAc): LLRF and Data Acquisition
- Gamma-CT: Collaboration with Helmholtz Center Dresden

MTCA.4 for Eureca

- RTM-DRS4
  - 16 Channel Transient Recorder
    4 x DRS4 (up tp 5 GSps)
    Low Power Digitization
  - Channel Specific Threshold Trigger
  - FPGA Spartan6
- AMC TAMC651 (TEWS)
  - FPGA Spartan6
  - PCIe Gen1 x1
  - SFP Front Side

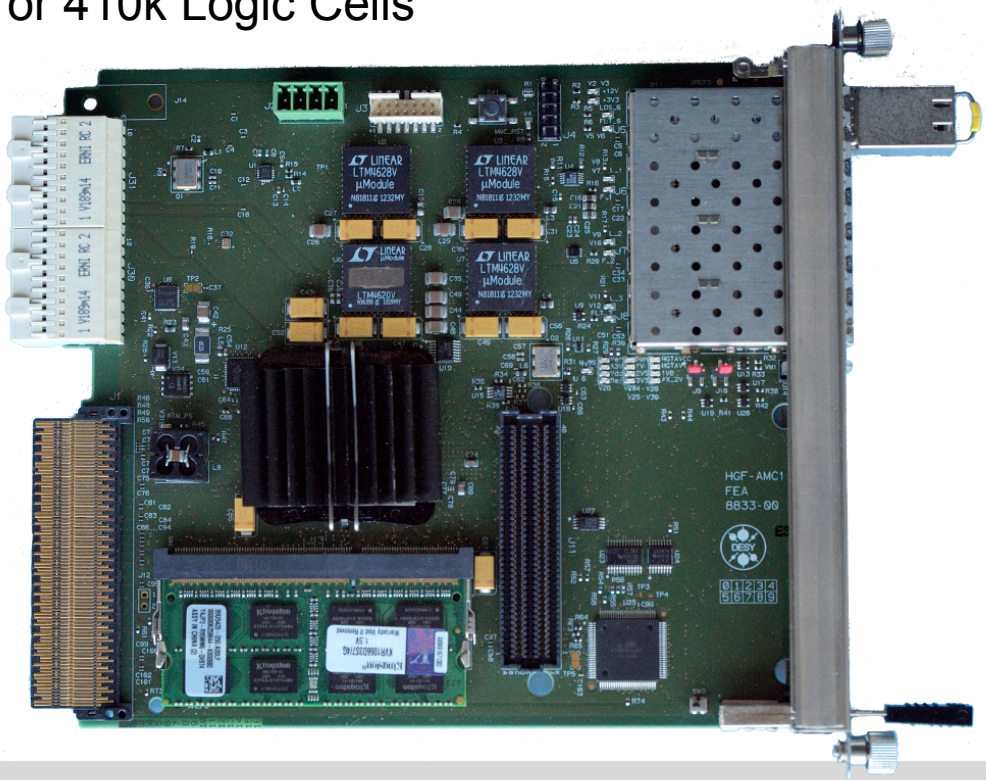


HGF-AMC Cooperation with DESY

- Supported by HGF-Program DTS

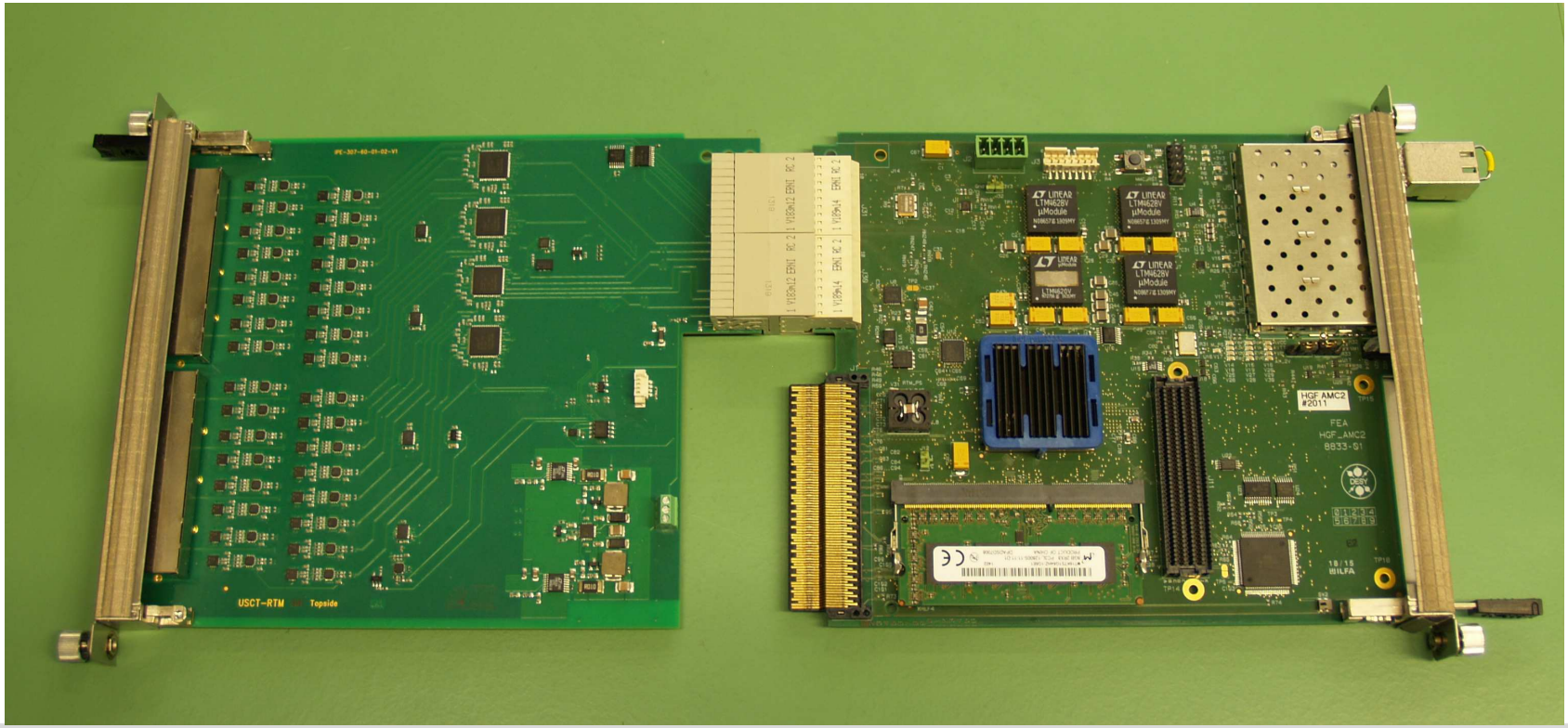
- Multipurpose Readout Board
- New Generation of FPGAs
  - Xilinx Kintex7 28nm with 325k or 410k Logic Cells
- PCIe Gen2 x4
- P2P 10 Gb/s
- SODIMM DDR3 Memory up to 8 GByte
- High Speed Serial Links (4 x 10G Ethernet)
- FPGA Mezzanine Card Connector (FMC)

- Peripheral IP Framework



MTCA.4 for USCT

- RTM-32ADC
  - 32 channels
  - 12b @ 10 to 40 MHz
  - VGA 0 to 40 dB
- HGF-AMC
  - FPGA Kintex7 410k Logic Cells
  - 8 GByte SODIMM



MTCA.4 Community

- Research
  - CERN, ELETTRA, FNAL, IHEP, IN2P3, IPFN, ITER, KEK, LBNL, SLAC
  - DESY, FZJ, GSI, HZDR
- Industry
  - Pentair, ELMA, Kontron, N.A.T., TEWS, Vadatech, Struck, Wiener
- HGF supported Programm „MTCA.4 for Industry and Research“
  - Dissemination of MTCA.4
    Link: MTCA.DESY.DE

Conclusion about MTCA.4

- MTCA.4 PICMG Standard
- Powerful Processing and High Bandwidth Capabilties
- Flexible and Scalable System

- Increasing Use in Scientific Applications

- Collaboration and Know-How Transfer between Scientific Facilities

- Commercial Components Available

- **Next Generation of Data Acquisition Systems**

Questions ?

Fully equipped 12 slot system
384 analog input channels

Some Digitizer Boards for MTCA.4 Systems

- FMC 16 x 16 bit @125 kHz **DESY**
- MTCA.4 10 x 16 bit @125MHz **Struck / Vadatech**
- MTCA.4 32 x 12 bit @20 MHz **TEWS**
- RTM 32 x 14 bit @40 MHz **KIT**
- RTM 16 x 12 bit @1.0 GHz **KIT**
- FMC 4 x 10 bit @1.25 GHz **4DSP**
- FMC 4 x 12 bit @ 1.0 GHz **KIT** (planned)