KIT ASIC Development for EUSO-like devices

Some specifications: (for improved Citriroc chip)

- Large number of channels: 64, 128, or more for simple board design
- BGA package instead of QFP
- 5 ns timing resolution and pulse shaping
- Low(er) power consumption (2mW/ch or less)
- Internal biasing for flat fielding/temperature control
- pulse counting & current integration over entire timing bin
  length selectable from 250ns-5us
- Multiplexed output (of analog signal)

Citriroc diagram

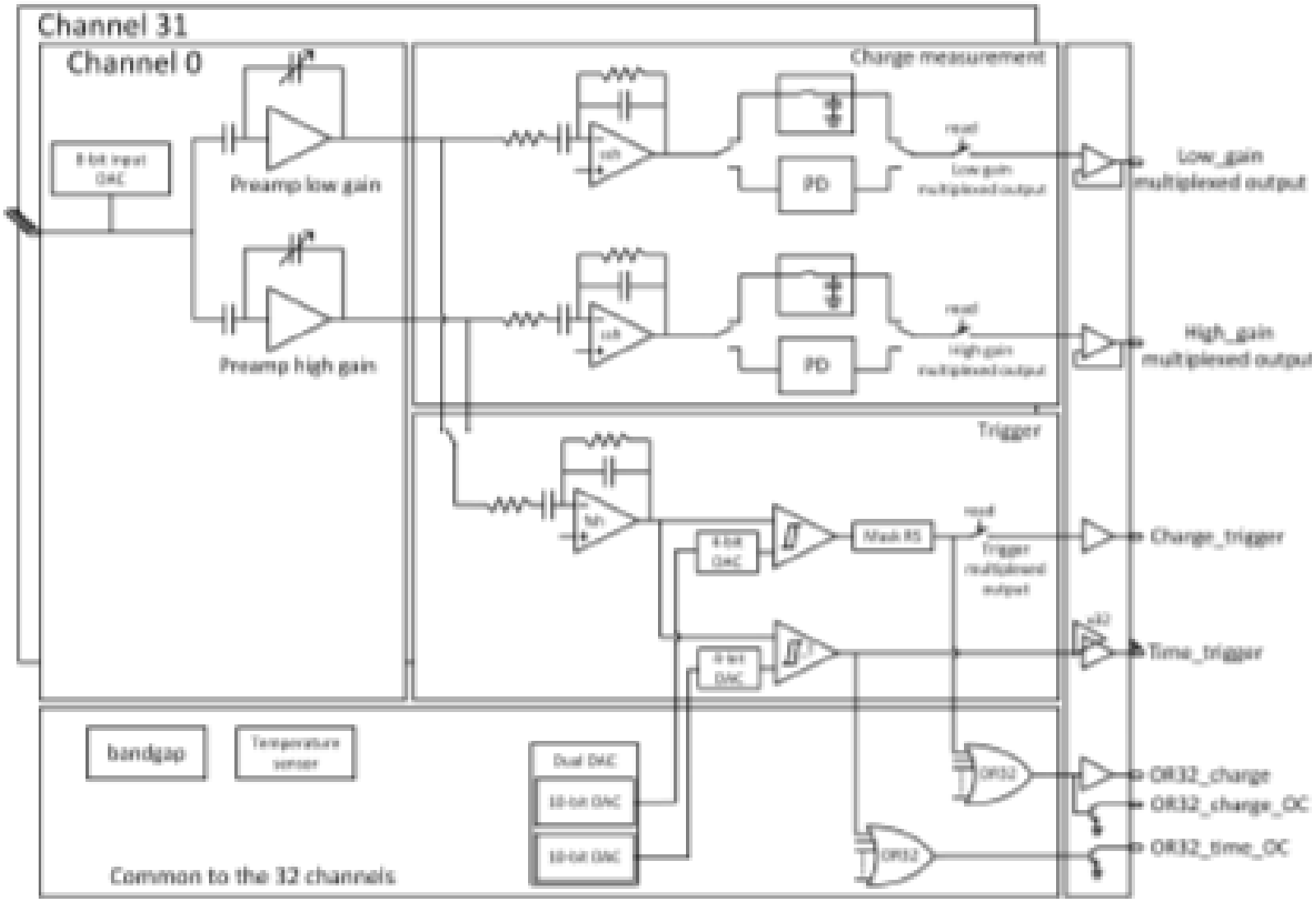


Figure 2 - General ASIC block scheme

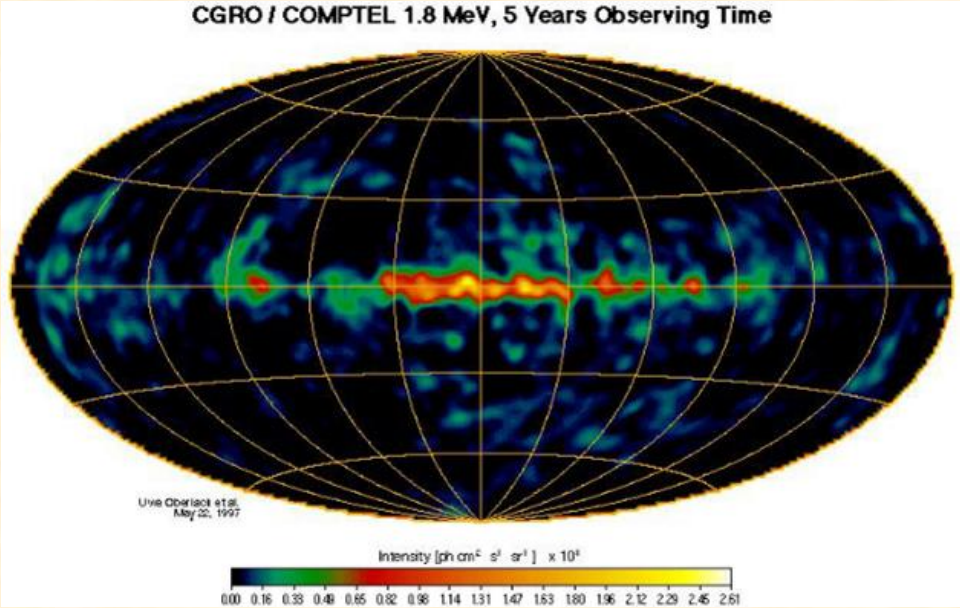
ASIC for large SiPM array

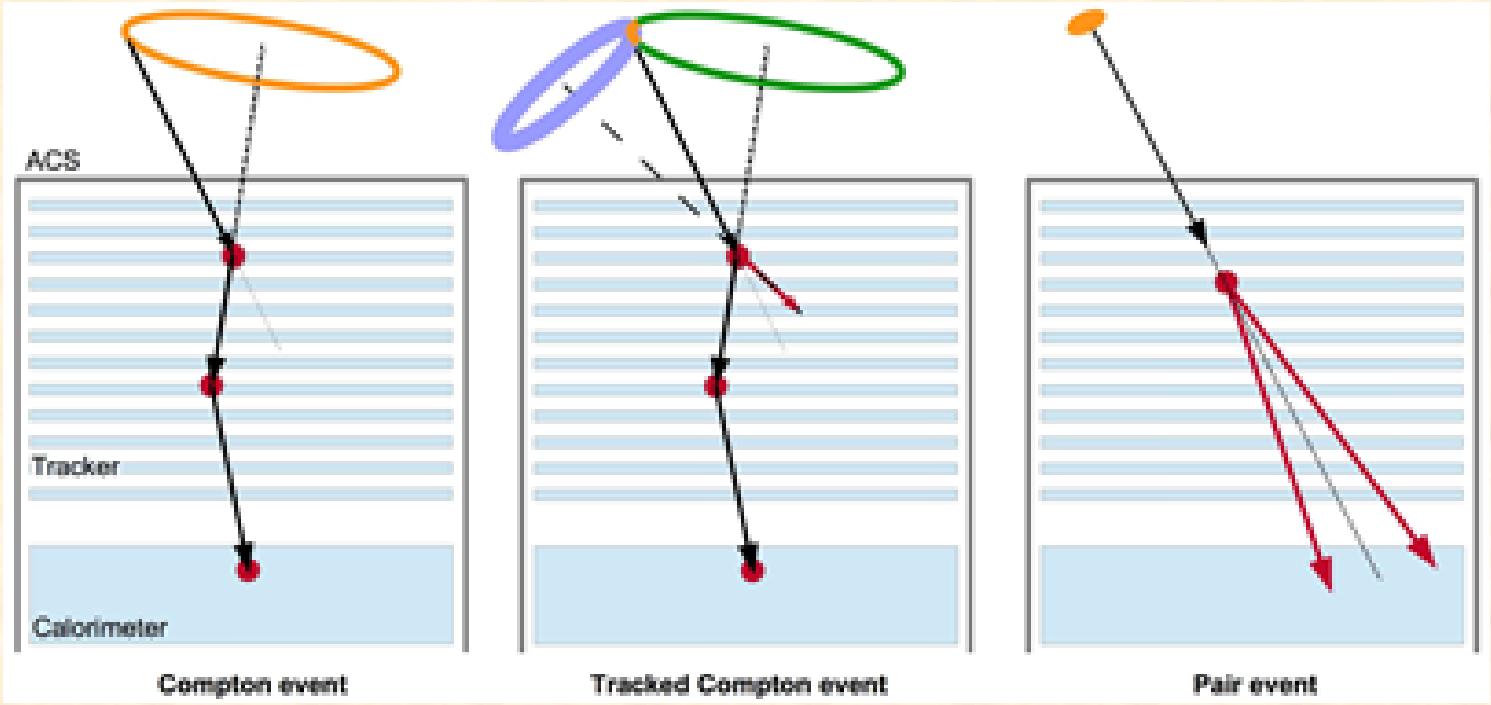
- Sum up the signal from 10÷100 cm² SiPM without adding up the capacity. (“amplifier” with ~100 inputs and 1 output channel)
- drive 50 Ω line (analog signal preferred)
- Should work at LN temperature
- available in ‘die’ (radiopurity requirement)
- ~mW power consumption, single rail power line (derived from SiPM bias)
- integrated bias circuit for ~100 SiPMs: equalise gain between SiPMs, current limit, shut down broken SiPM

We don’t need !

- signal rise time better than 10 ns
- dynamic range > 1000 / channel

γ-ray Astronomy: Compton & pair-production Telescopes





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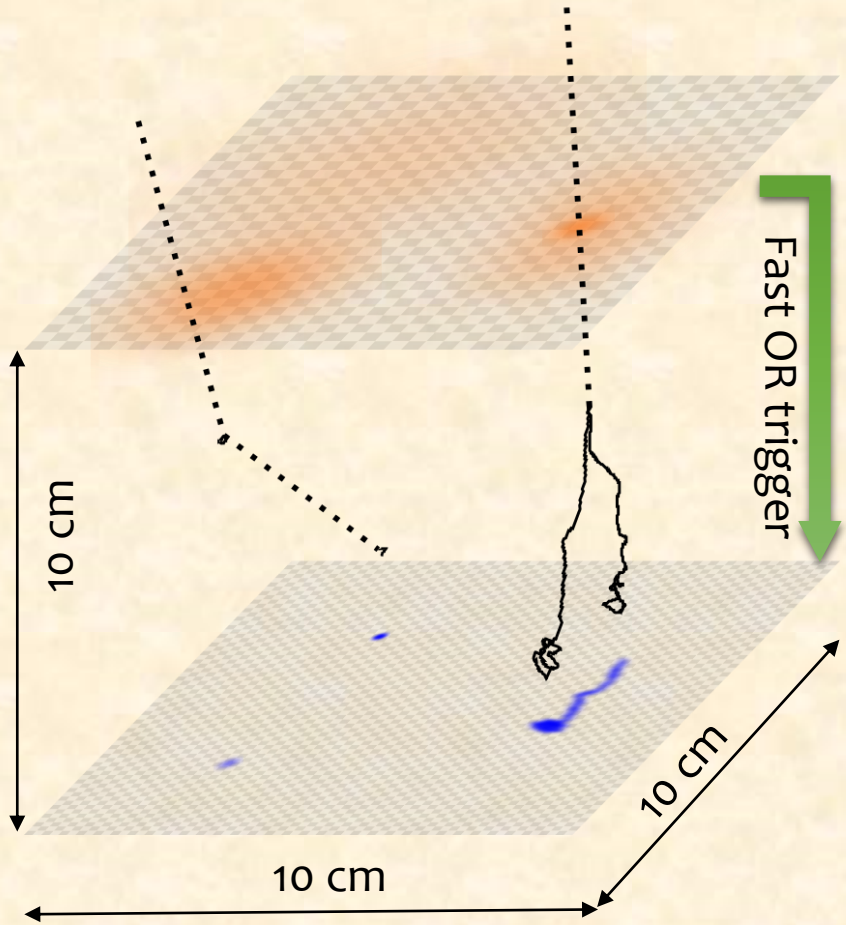
A liquid xenon TPC telescope

- 10x10x10 cm^3 module prototype



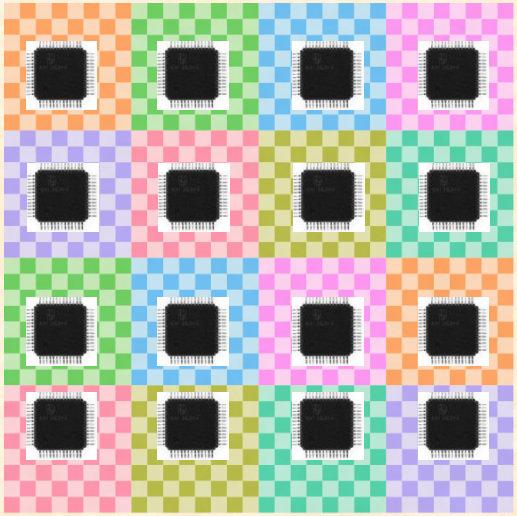
Scintillation light on SiPM

- Total light with high resolution
  - but also distribution
- Fast OR (~ ns resolution)
  - trigger for charge readout
  - In final instrument, Time-Of-Flight

Ionization drifts and is collected

- Charge with high resolution
  - ~100 e- ÷ ~500k e- (few keV ÷ some MeV)
- X-Y with <0.5 mm resolution
- Z from time delay (~200µm resolution)
- *How to sample charge from tracks? Still under discussion*

Some (tentative) numbers



SiPM readout plane

- VUV-sensitive sensors on the market probably 3x3 cm^2
  - o(1k) for prototype, o(200k) final instrument
  - If 64 channel ASIC, 16 chip for prototype, o(3k) later
- Dynamic range: *12 bits? 10bits and two gain 1xA, 4xA?*
  - *Some gain fine tuning / calibration possibilities?*

Ionization readout

- Low noise electronics, ENC ~100 e-
  - 12 bit dynamic range
- High channel density with 1.5x1.5 mm2 pixels
  - *e.g. 256 channel ASIC (16 chips for prototype, o(3k) at the end)*
- Slow e- mobility, 500 ns to integrate 1mm of charge cloud
  - *Can we have some form of 100ns sampling for tracks?*

Other challenges (under discussion)

- Data transmissions (ASIC to FPGA and further):
  - 12 bits / ch. >160 Mbs / ch. – OR – >2.5Gps / group of 16 ch.
- Heat load from electronics to liquid xenon