FPGAs in Research

Firmware Development for the ATLAS IBL BOC card

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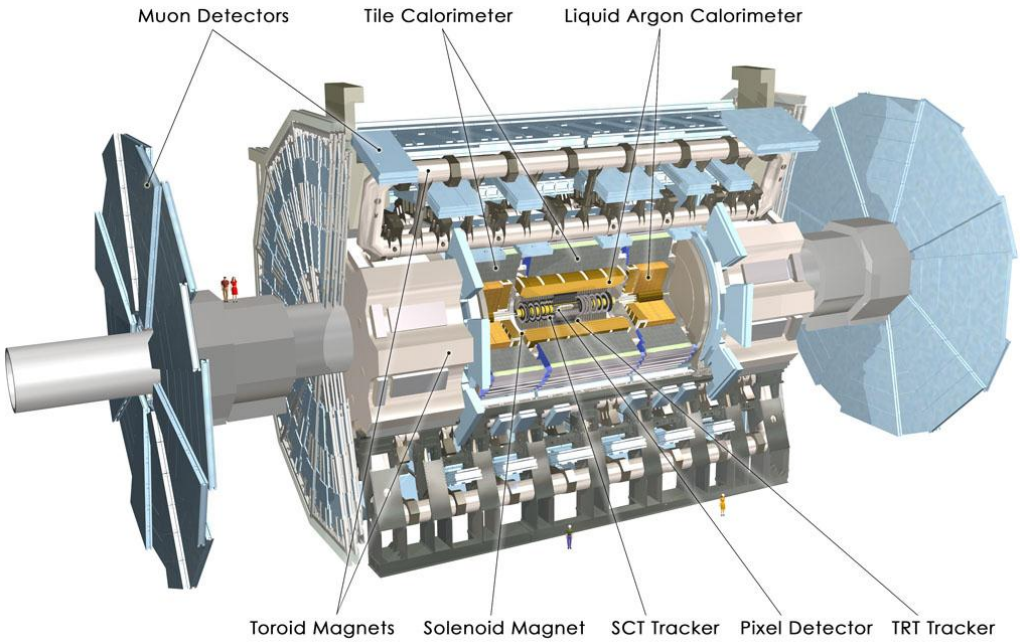
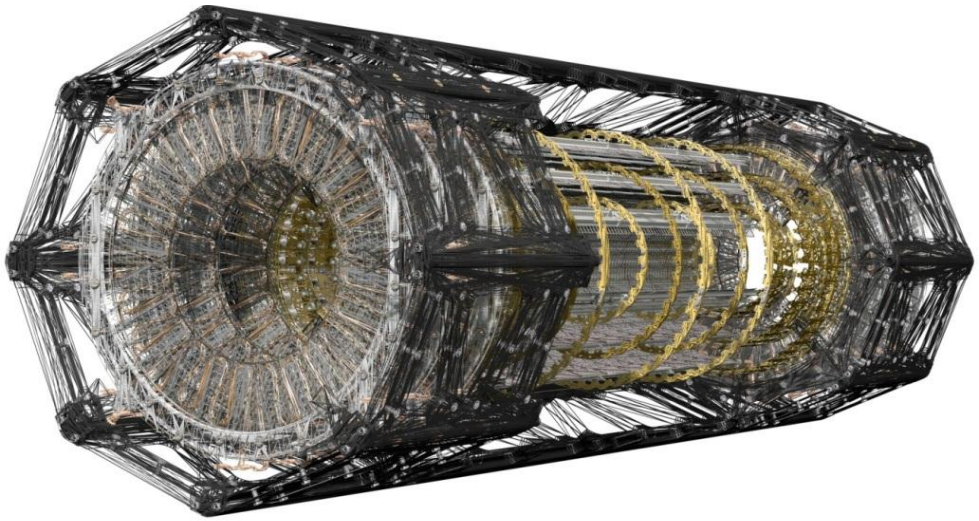
ATLAS Detector

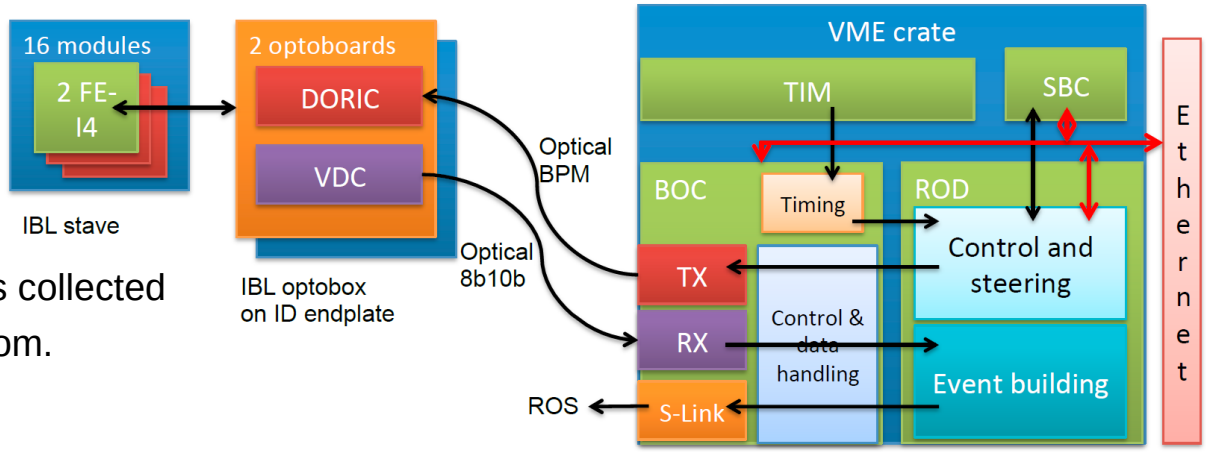
- ATLAS is the largest experiment at the LHC
- Length: 45 Meter
  Diameter: 22 Meter
  Weight: 7000 Tonnen
- Main task of the detector is the search for new particles.
- The pixel detector is the innermost part of ATLAS and is used for track recognition and reconstruction.
- Insertable b-Layer (IBL):
  - Installation during shutdown 2013/14
  - New innermost layer with additional 448 front-end-chips serving ~12 million channels
  - Increases the resolution of the current pixel detector and compensates irradiation damage





ATLAS IBL Readout

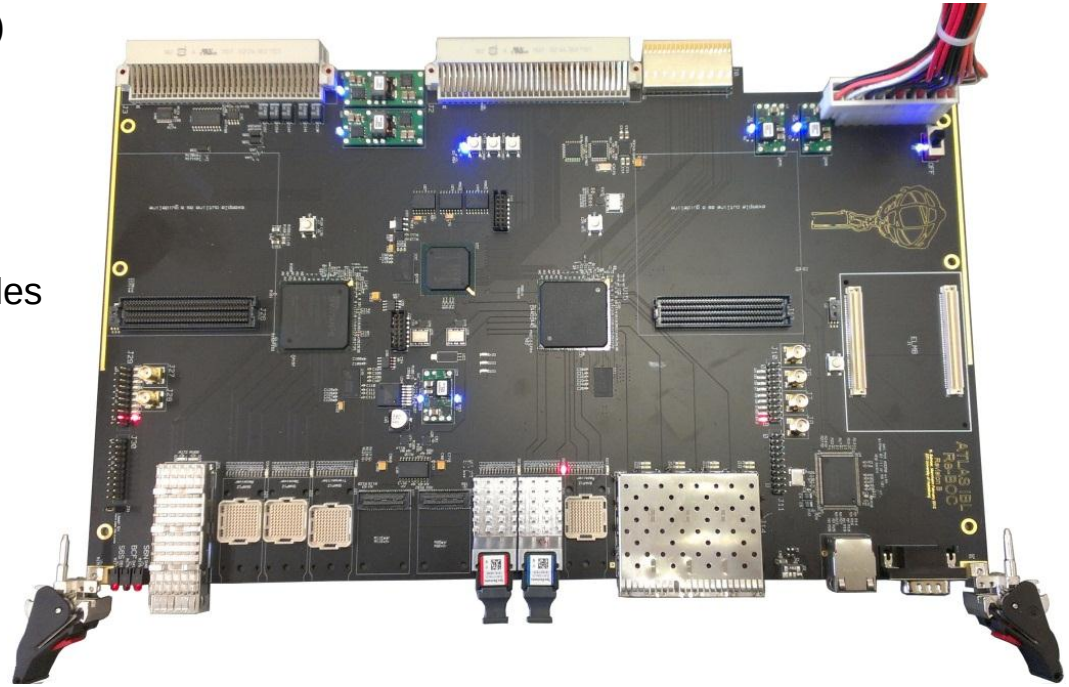
- On-Detector Readout:
  - Front-End-Chips reads hits from pixel sensor
  - Data of 32 front-end-chips is collected and send to the counting room.



- Off-Detector Readout:
  - Back-of-Crate card (BOC) is the converter between optical and electrical interfaces.
  - Read-Out-Driver (ROD) controls the readout of one stave and is responsible for histogramming and formatting the data as well as doing calibration scans.
  - TTC-Interface-Modul (TIM): controls timing and trigger of the modules
  - Read-Out-Subsystem (ROS): collects the data as first stage of the higher-level readout

ATLAS IBL BOC card

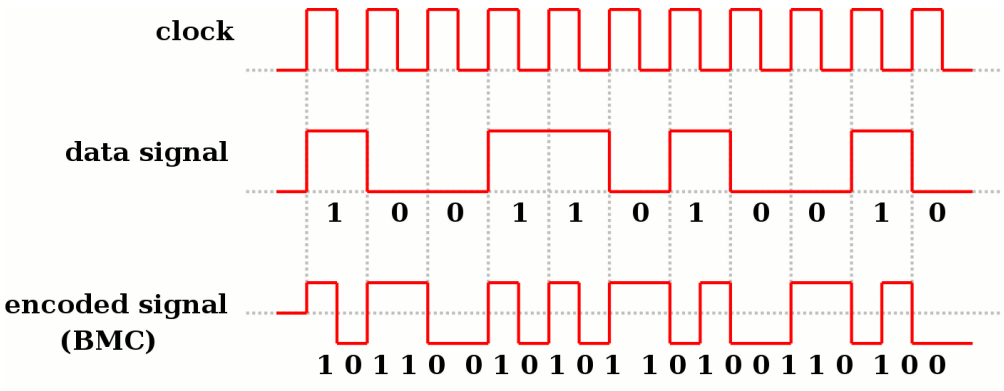
- FPGA-based redesign based on the current pixel readout system
- Xilinx Spartan 6 FPGAs:
  - 1x BOC Control FPGA (BCF, LX75T)
  - 2x BOC Main FPGA (BMF, LX150T)
- Optical modules:
  - To/from the detector:
    commercial SNAP12 RX/TX modules
    custom-made TX plugins
  - To the higher-level readout:
    commercial (Q)SFP modules
- „outer world“:
  - Gigabit Ethernet
  - VME



- Connection to the detector control system (DCS) with measurement module (ELMB): temperature, humidity

Requirements

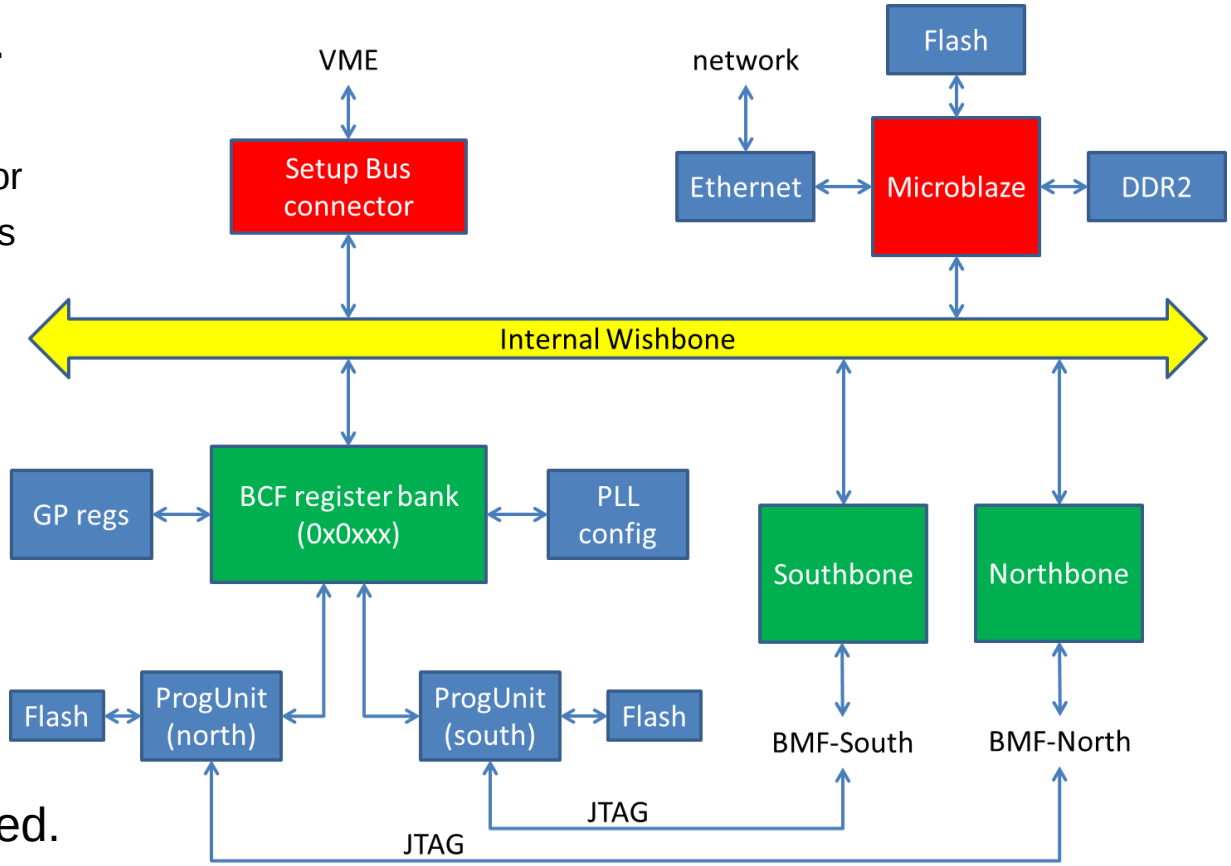
- 32 front-end-chips per card need to be read out
- The transmitters encode clock and data into a single BPM signal with 40 MBit/s data rate. This signal has to be delayed in steps of 100 ps to adjust the timing with respect to the bunchcrossing.



- Data from the detector has an 8b10b encoding and runs with 160 MBit/s.

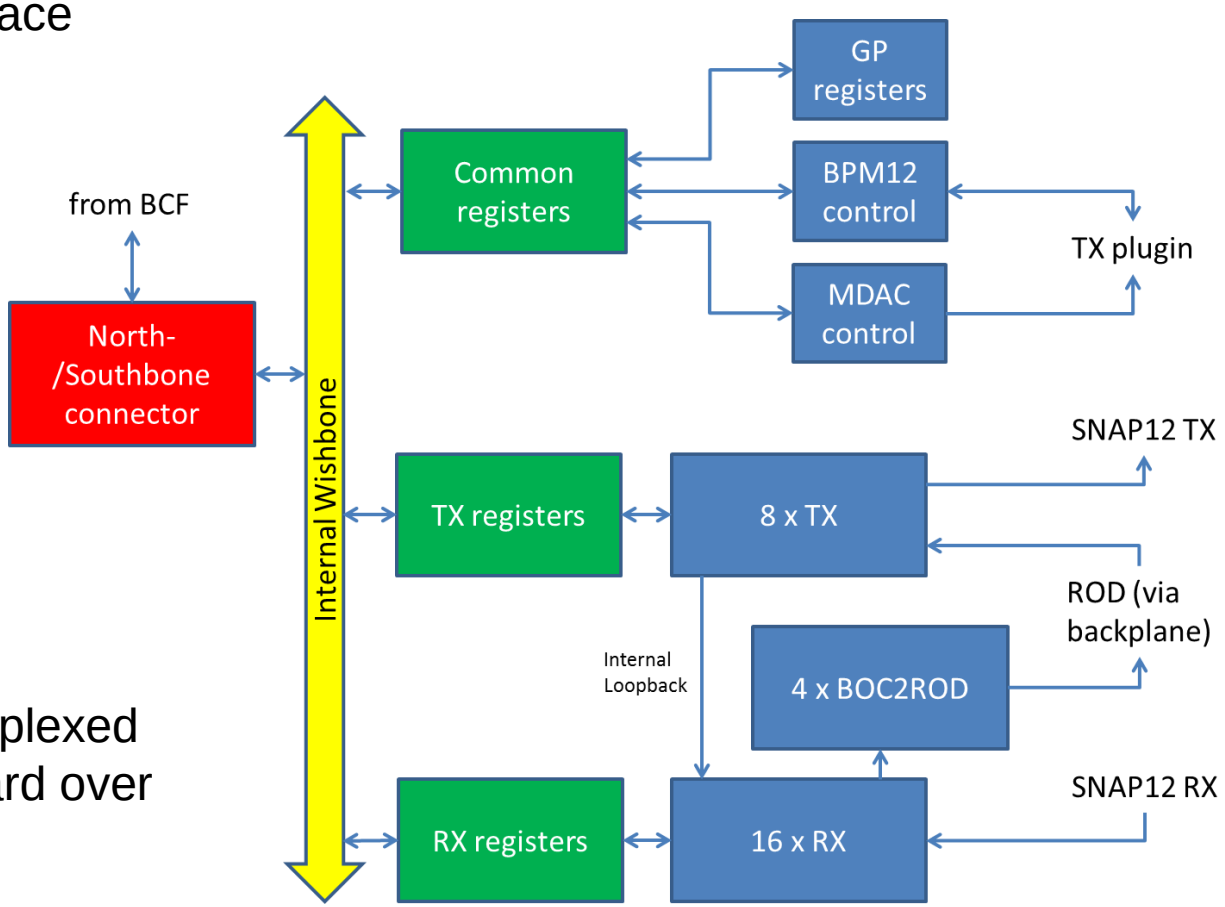
BCF Firmware

- BCF is responsible for control of the whole card.
- Important modules:
  - Wishbone bus with arbiter for up to 4 masters and 4 slaves
  - Microblaze-CPU is used for Ethernet communication and will be used for self-testing of the card (POST).
  - „ProgUnit“: controls the programming of the BMF and allows remote firmware upgrade.
- BMF FPGAs can be accessed memory-mapped.



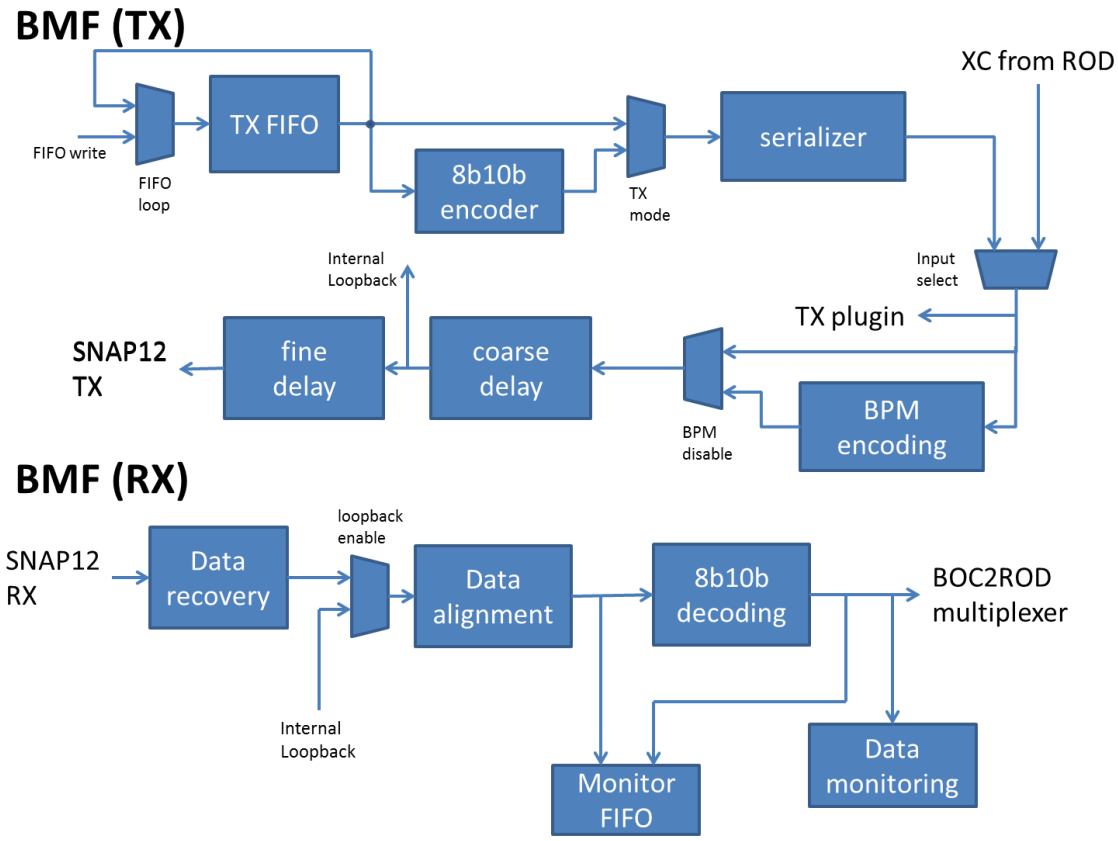
BMF Firmware

- Internal Wishbone interface
- 3 register banks:
  - Common registers (firmware version etc.)
  - RX registers
  - TX registers
- RX / TX schematic next slide
- 4 RX channels are multiplexed and send to the ROD card over a parallel bus.



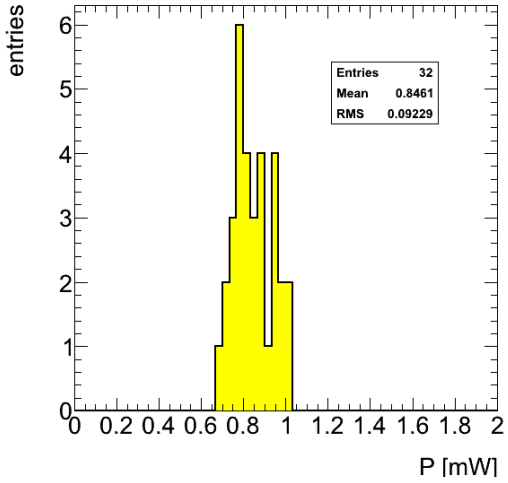
BMF transmitters/receivers

- TX:
  - Responsible for BPM-encoding of the trigger/control signals
  - Internal FIFO to inject data
  - Internal 8b10b encoding for testing purpose
- RX:
  - Data Recovery with 4x over-sampling and automatic phase adjustment
  - Word alignment using the 8b10b k-words (SOF, EOF)
  - Local buffer for received data (standalone setup)
  - Monitoring of incoming data to detect errors.

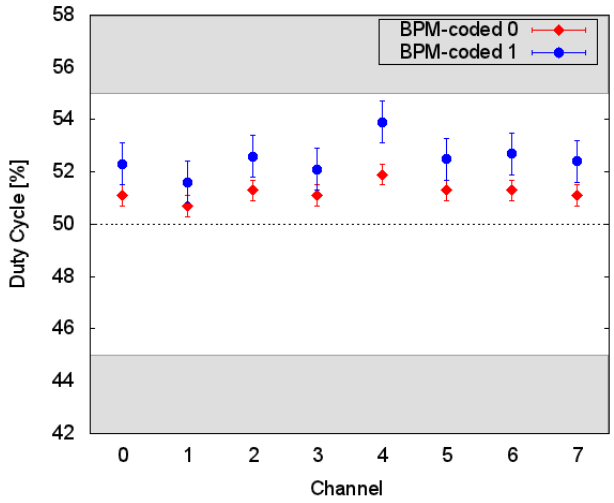


Transmitter tests

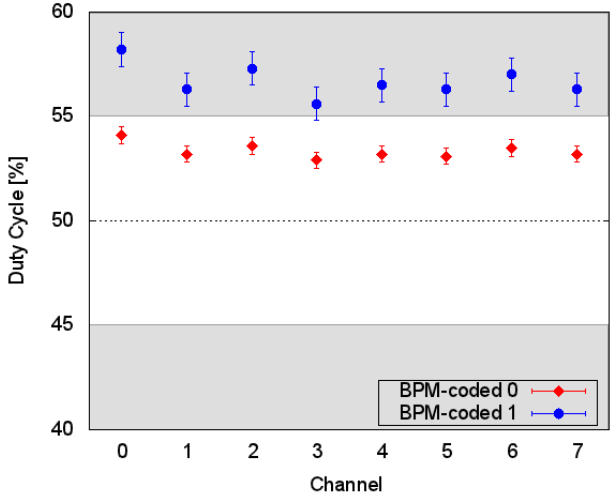
- We need to meet the requirements of the Optoboard with respect to the signal shape:
  - Duty-cycle between 45 and 55%
  - Input power at least -6 dBm
- SNAP12 output power around -1.9 dBm
  - A maximum attenuation of 3.1 dB in the fibers is acceptable.
    Fibers have estimated attenuation of less than 1 dB.
- Duty-cycle is distorted by the current implementation of the fine delay blocks:



Multiplexer-Chain

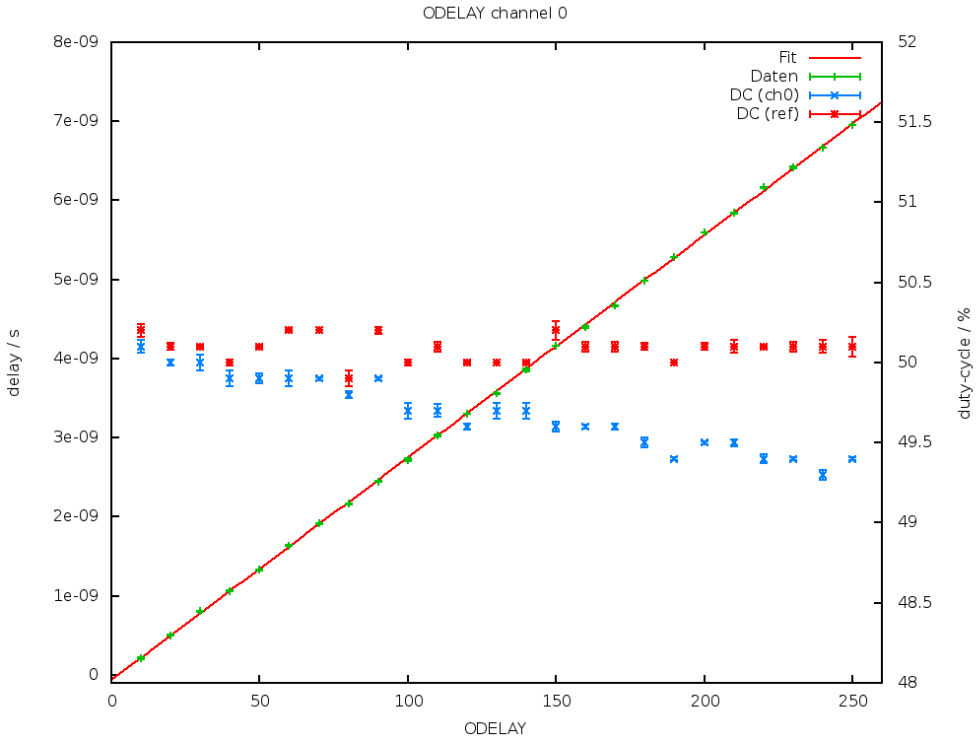


IODELAY



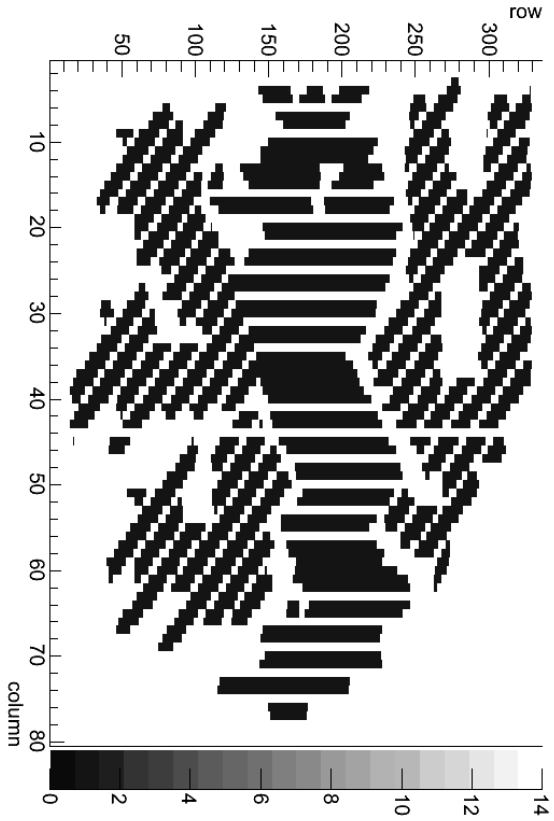
Fine-Delay-Implementation using ODELAY blocks

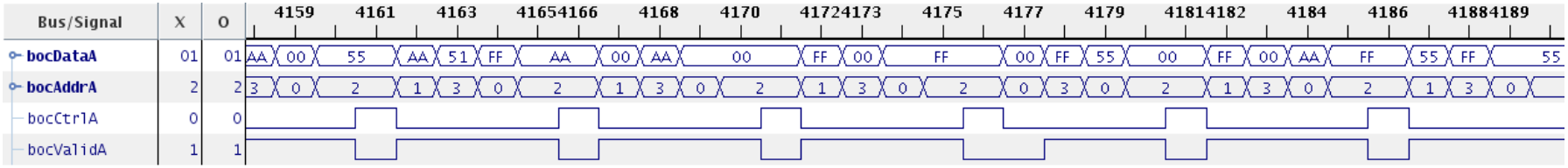
- Spartan-6 provides IODELAY blocks in the IOB.
- ODELAY-setting needs to be known at synthesis time (no variable ODELAY is available).
- We got very good results for the delay using ODELAYs.
- Idea: Changing the ODELAY value using partial reconfiguration
  - The P&R-netlist is modified with the FPGA editor.
  - Generation of a partial differential bitstream.
  - The bitstream is send to the ICAP port.
  - First test on the SP605 evaluation board were successful we will continue to work on this idea.



Test and verification of the receivers

- The receivers have been tested using internal and external loopback.
- Communication with the front-end-chips has also been tested extensivly.
- The whole receiver parts including the BOC-to-ROD interface have been tested by transferring over 2 terabytes of data. This results in a bit error rate smaller than 5×10^{-14}.





Conclusion

- The firmware for the ATLAS IBL BOC card has made good progress and is under test in Wuppertal, Bologna, Bern and at CERN.

- The fine delay implementation using ODELAY blocks and partial configuration shows very good results and will most likely be used in the final version of the firmware.