Karlsruher Institut für Technologie

Ultra-Fast Data Acquisition System of CSR *(Coherent Synchrotron Radiation)*

Workshop "HAP Topic 4 Advanced technology, 24 and 25 January 2013

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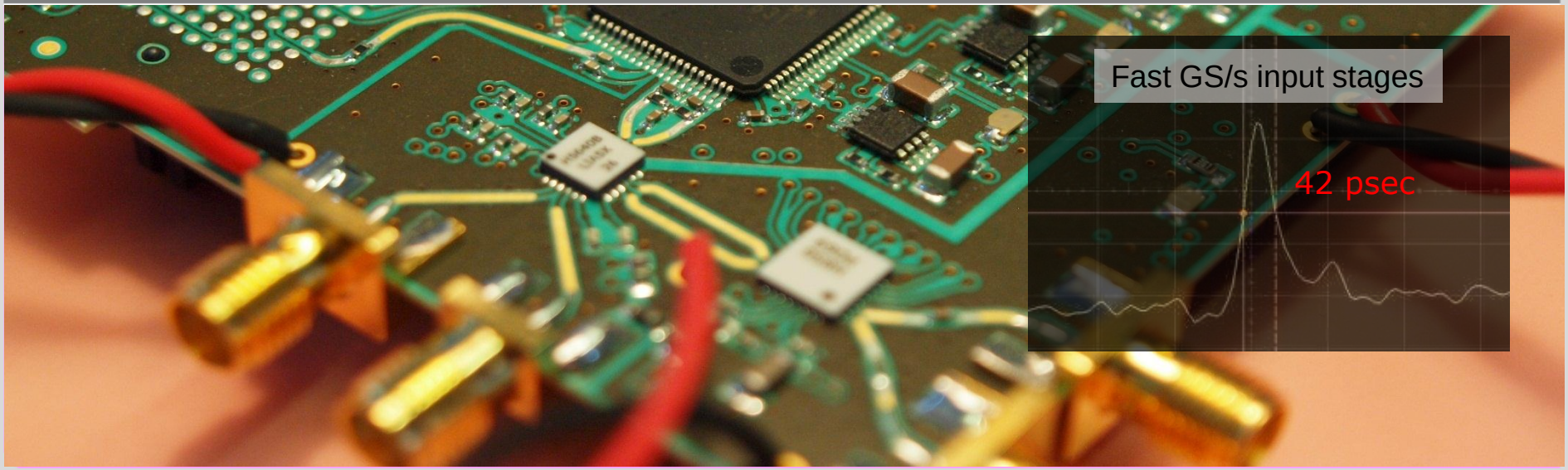
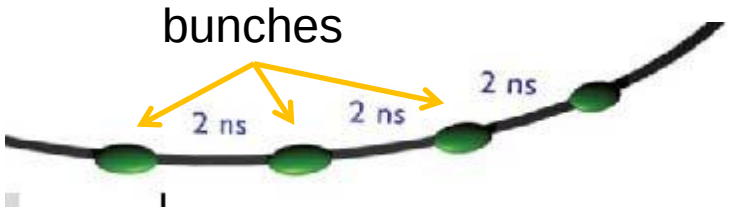
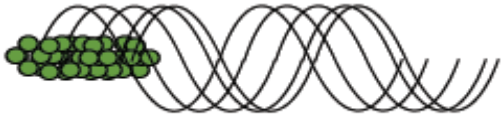
KIT, Institut für Prozessdatenverarbeitung und Elektronik
M. Caselle



THz radiation at ANKA



Normal mode



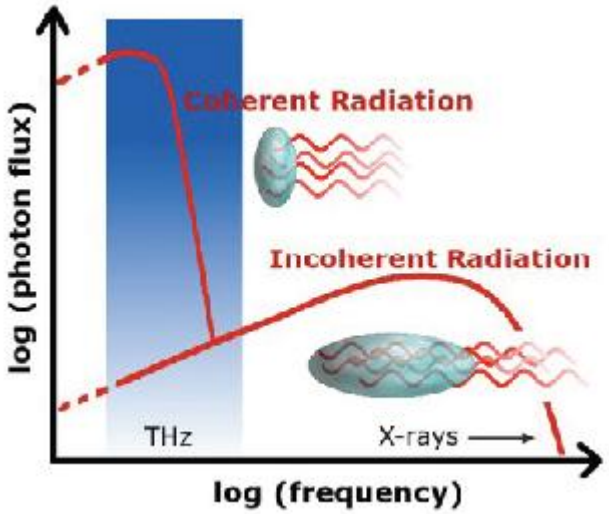
X-ray
incoherent radiation

Low alpha mode

THz
coherent radiation

ANKA parameters:

- Circumference: **110.4 m**
- RF-system: **500 MHz**
- Revolution time: **368 ns**
- Harmonic number: **184**
- Revolution frequency: **2.71MHz**
- Beam energy: **2.5 GeV**
  - low alpha mode: **1.3GeV**
- Bunch length (low alpha mode): few **ps**
- Bunch space: **2ns**

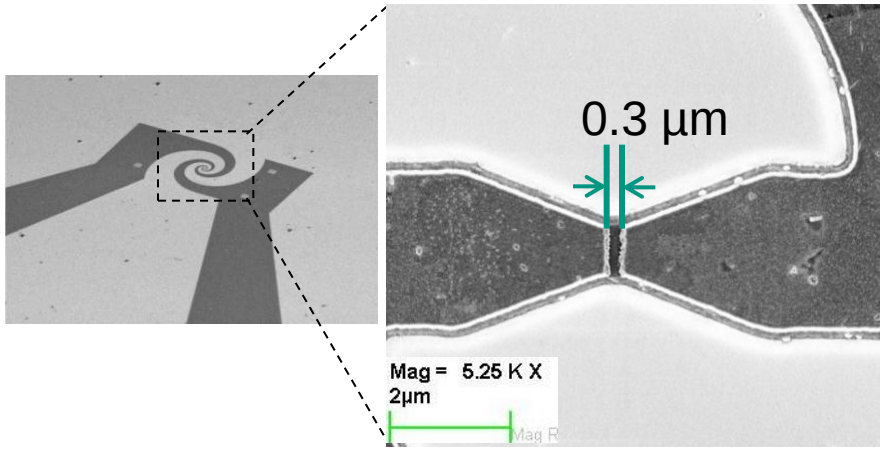


Procedure of bunch compression:

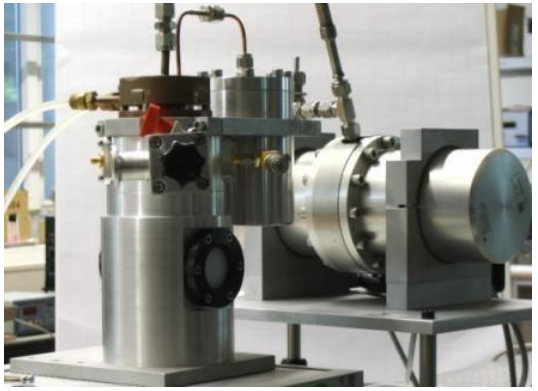
- ➡ injection
- ➡ ramping to 1.3 GeV
  - ➡ "squeeze"

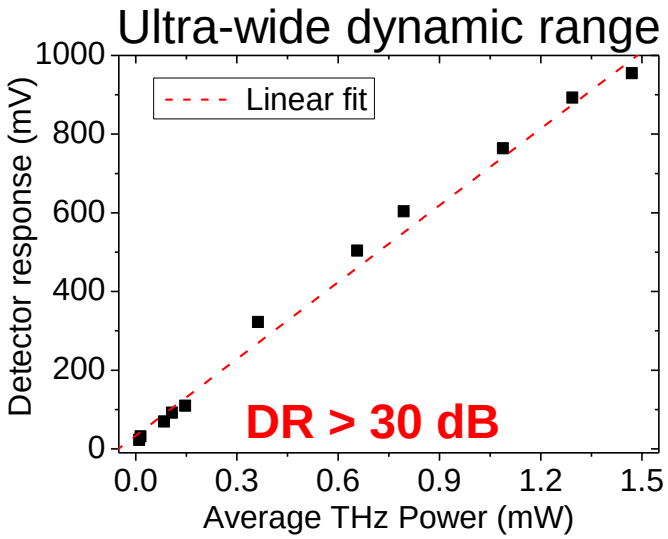
Reference:
OBSERVATION OF COHERENT THZ RADIATION FROM THE ANKA AND MLS STORAGE RINGS WITH A HOT ELECTRON BOLOMETER.
Proceedings of PAC09, Vancouver, BC, Canada, (A.-S. Müller)

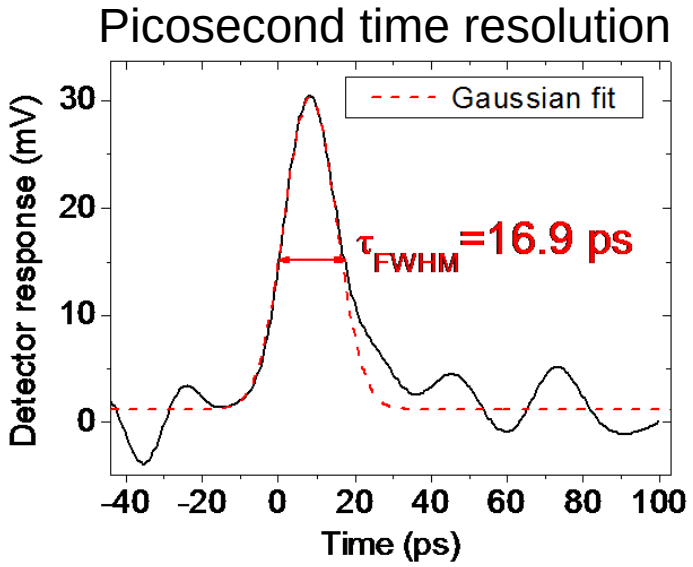
Ultra-fast YBCO THz detectors for picosecond synchrotron pulses



Nanometer-sized YBCO detectors in a high-speed readout system **operated > 77 K**







P. Thoma et al., *Applied Physics Letters*, 101, 142601, 2012
P. Probst et al., *Physical Review B*, 85, 174511, 2012

TeraHz detector & analog front-end

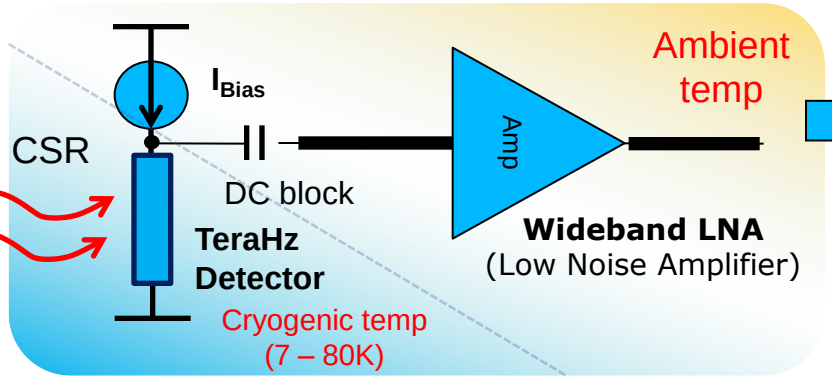
Detector system based on a superconducting NbN/YBCO ultra-fast bolometer with an bandwidth up to 1THz.

P. Probst. APPLIED PHYSICS LETTERS 98, 043504 (2011)

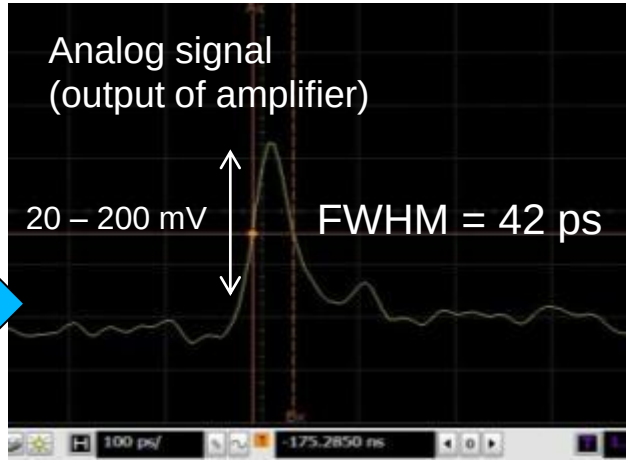
The analog circuit contains a low noise MMIC amplifier InP-HEMT based with a Bandwidth of 60GHz.

S. Wünsch. Superconductor science and technology – 20 (2007) S356-S361

ANKA – IR1



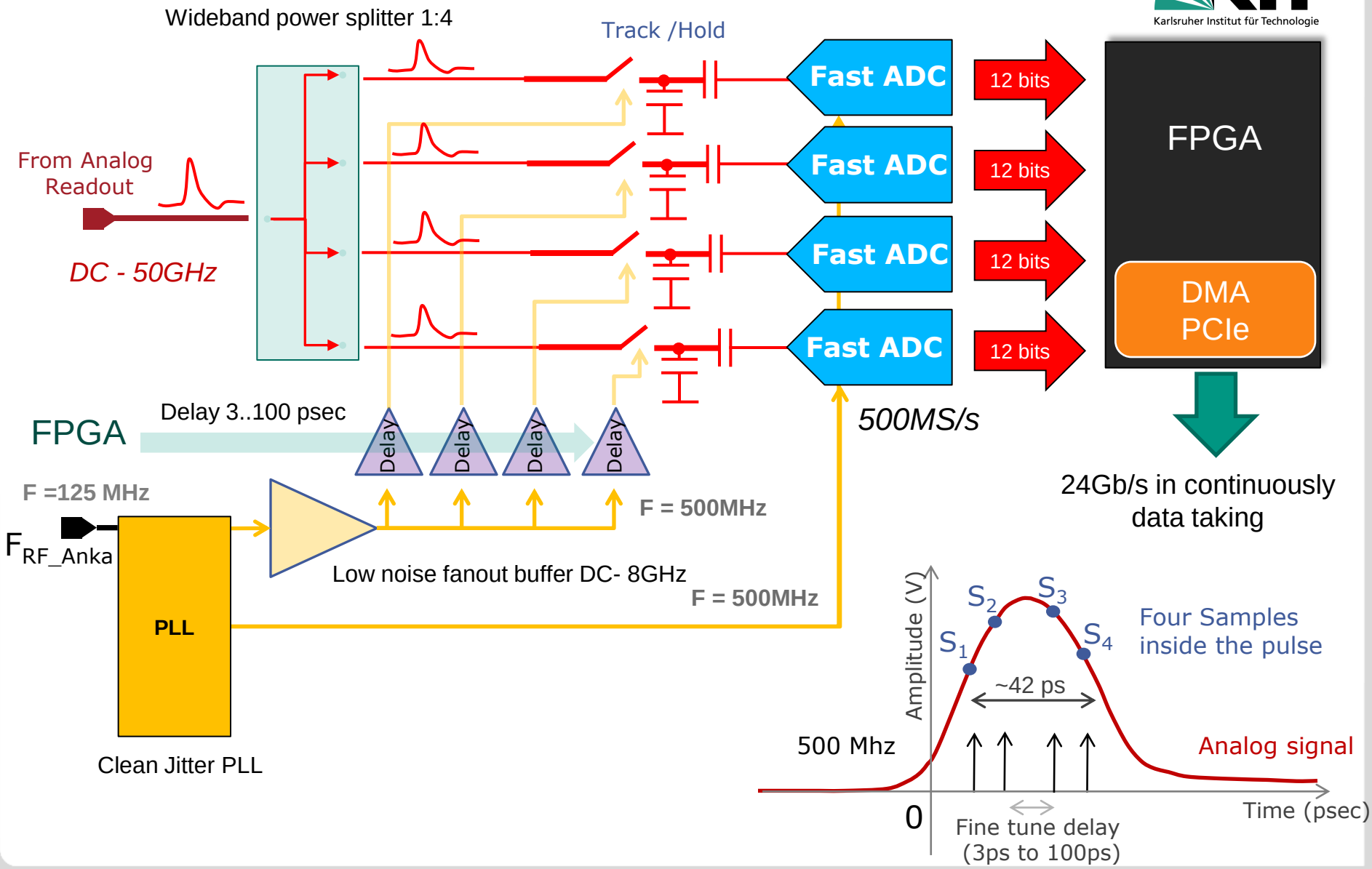
Pulse rate of 500MHz (ANKA RF-system)



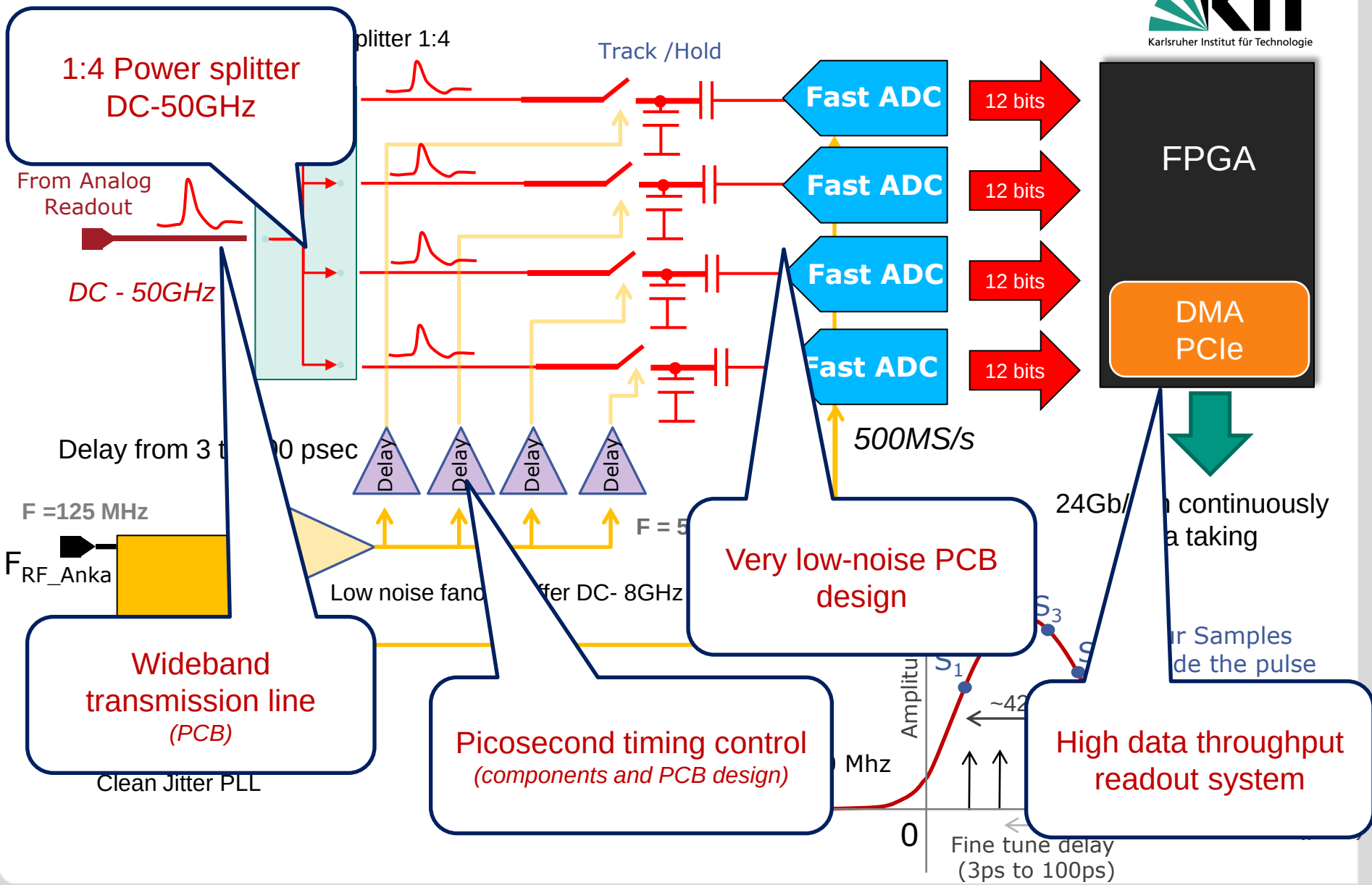
- Measure of the *peak amplitude* of each bunch *(range of few -600mV, resolution few mV)*
- Measure of the *pulse shape width of* each bunch *(range of 20 – 100 psec, resolution few psec)*
- Measure of the relative *time jitter* between bunches *(range 3- 100 psec, resolution few psec)*

Strategy: Digitize each pulse with 4 samples, perform the pulse shape reconstruction & Constant Fraction Discriminator (CFD) for precise pulse timestamp.

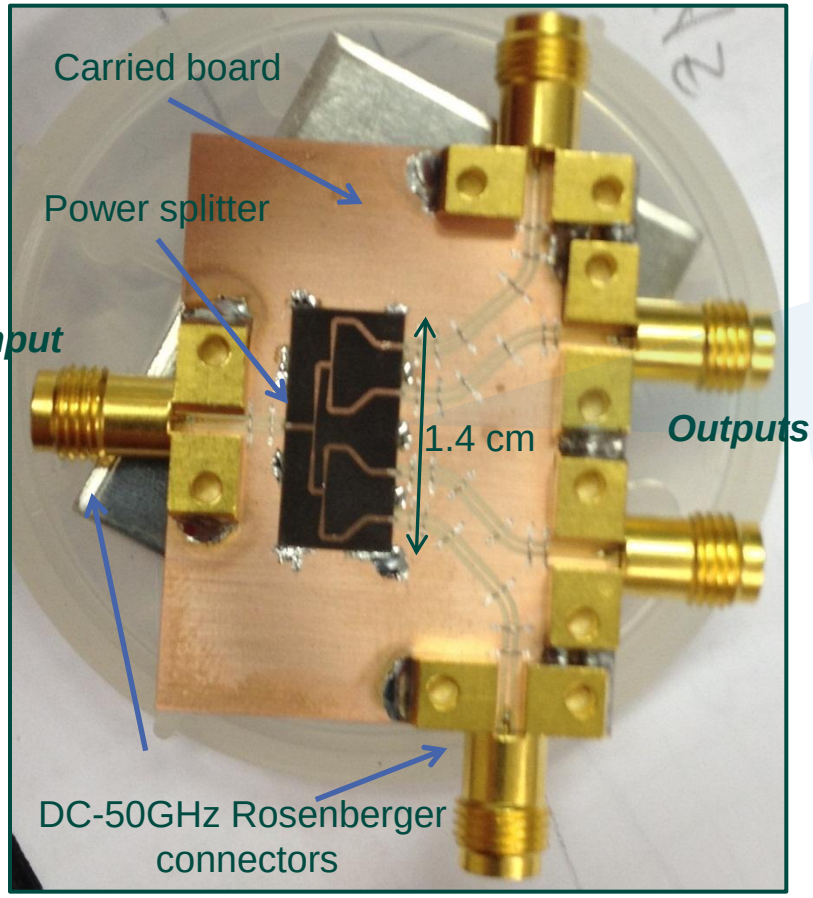
Fast pulse sampling board *(basic concept)*



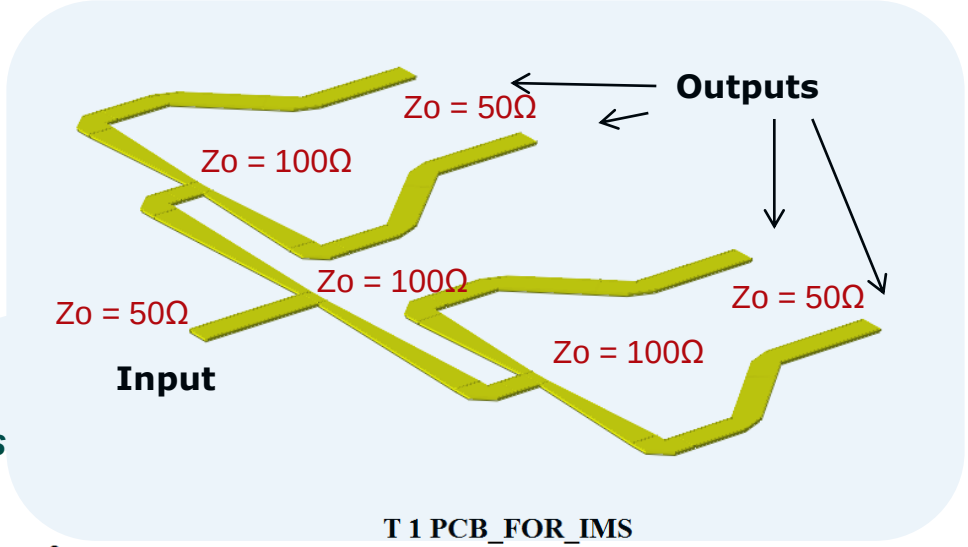
Fast pulse sampling board *(basic concept)*

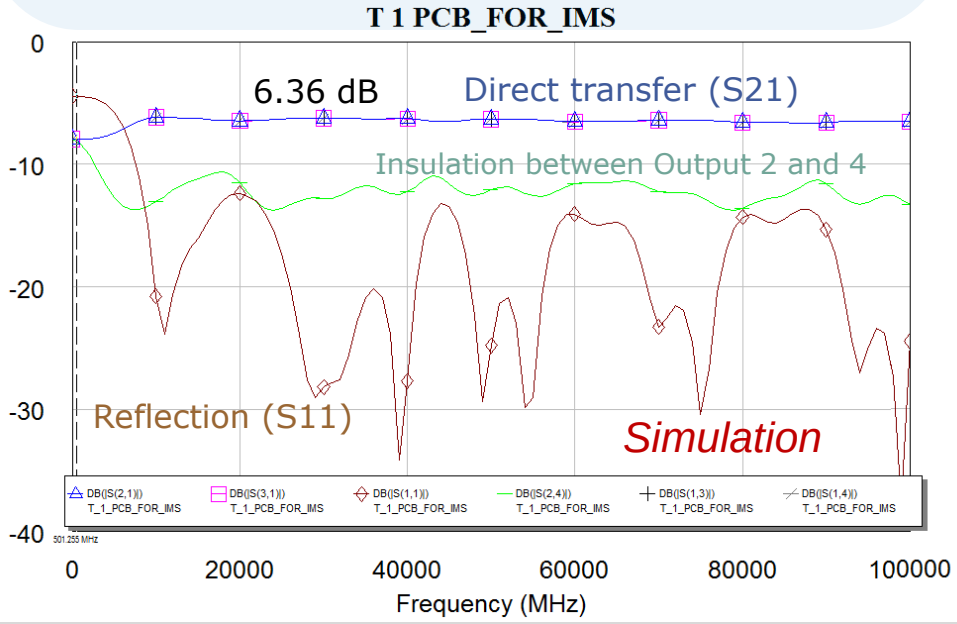


Power splitter DC - 50 GHz, PCB layout

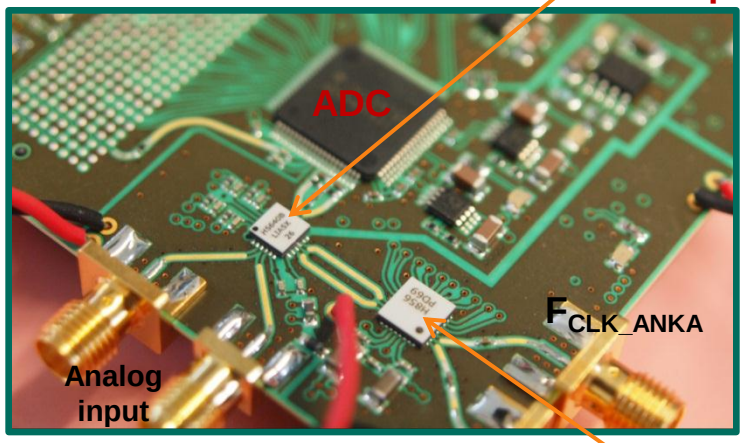


Substrate: Duroid5880

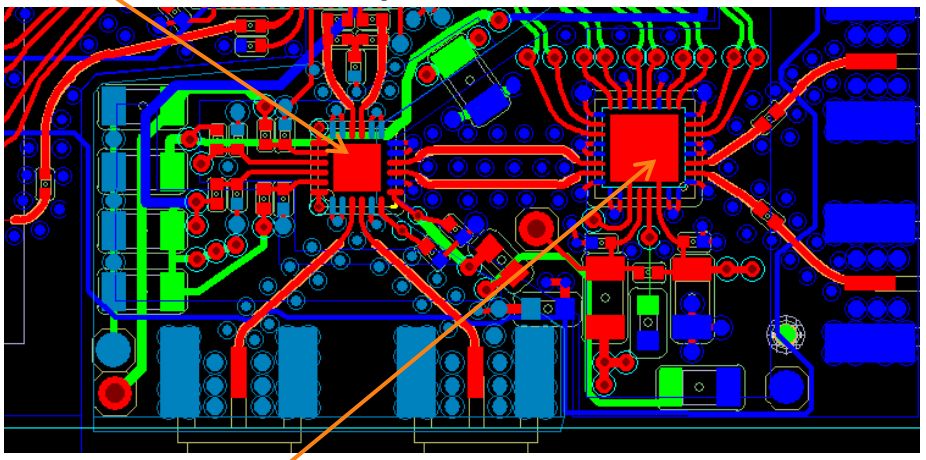




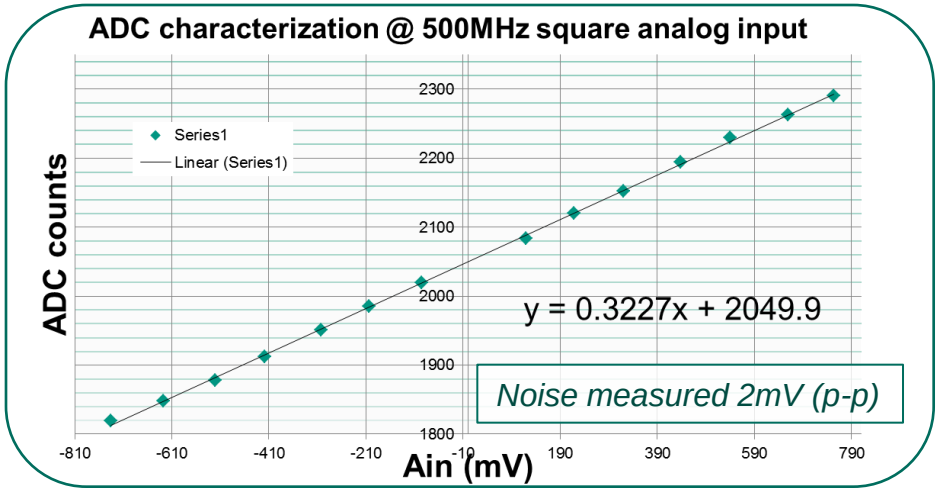
Pre-production board



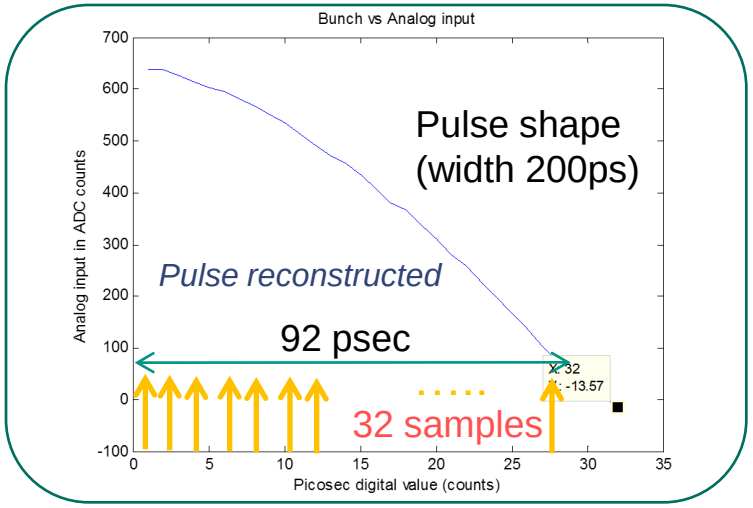
PCB layout - details



ADC linearity & noise measurement

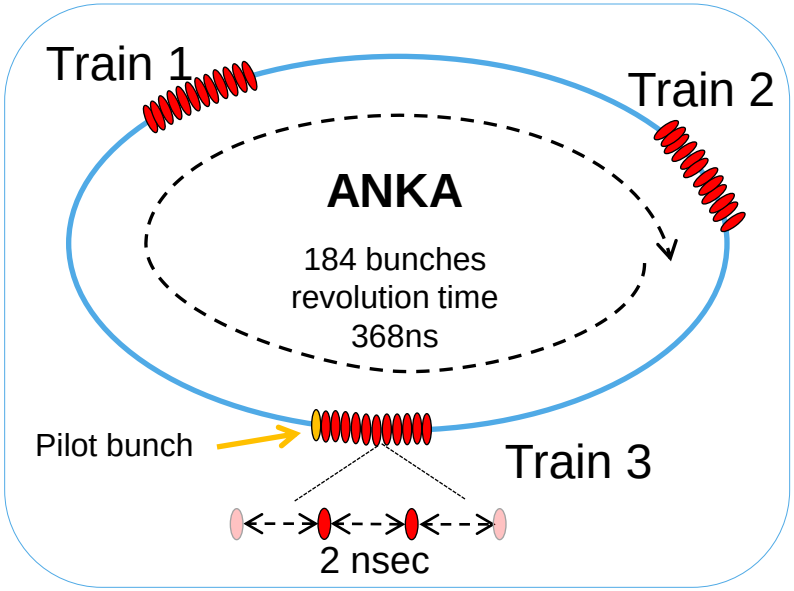


Sampling time characterization

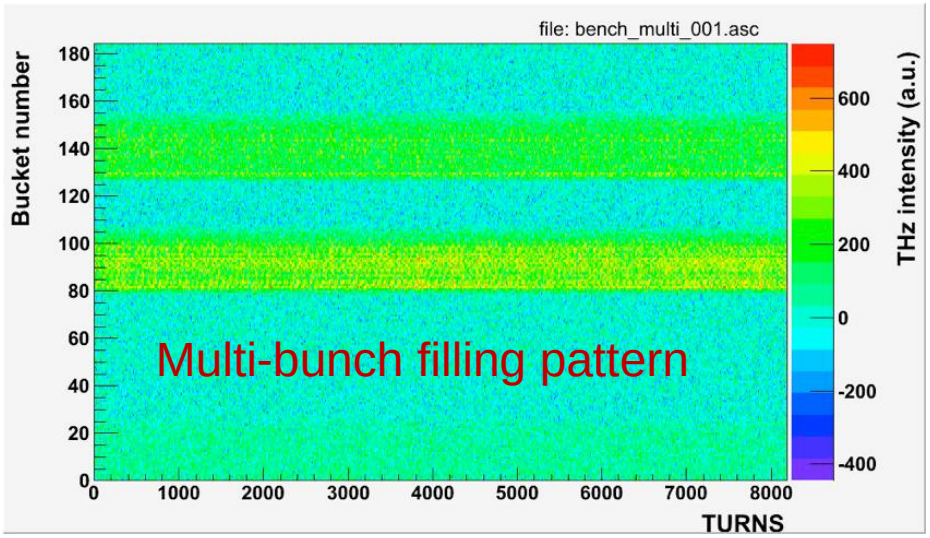


Sample time resolution < than 3psec

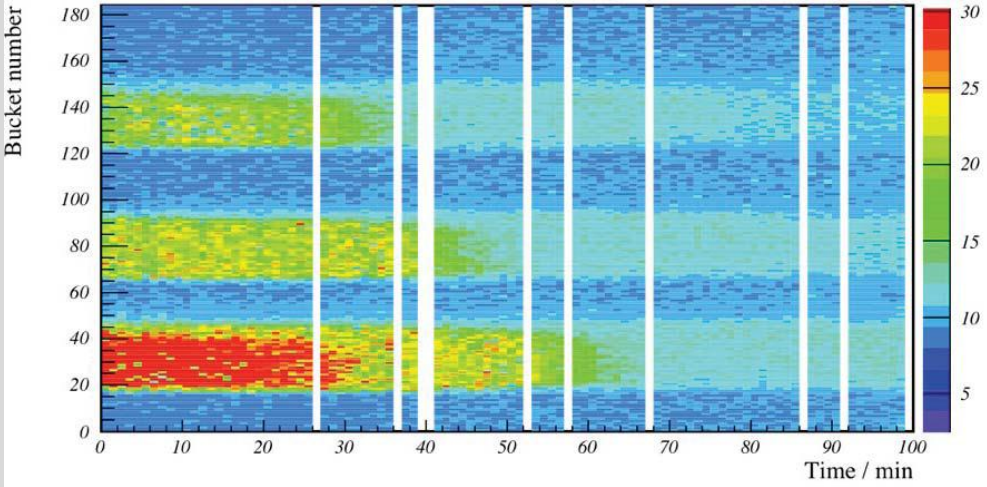
Pre-production board- ANKA Test Beam *March-2012*



ANKA CSR (with NbN HEB detector)



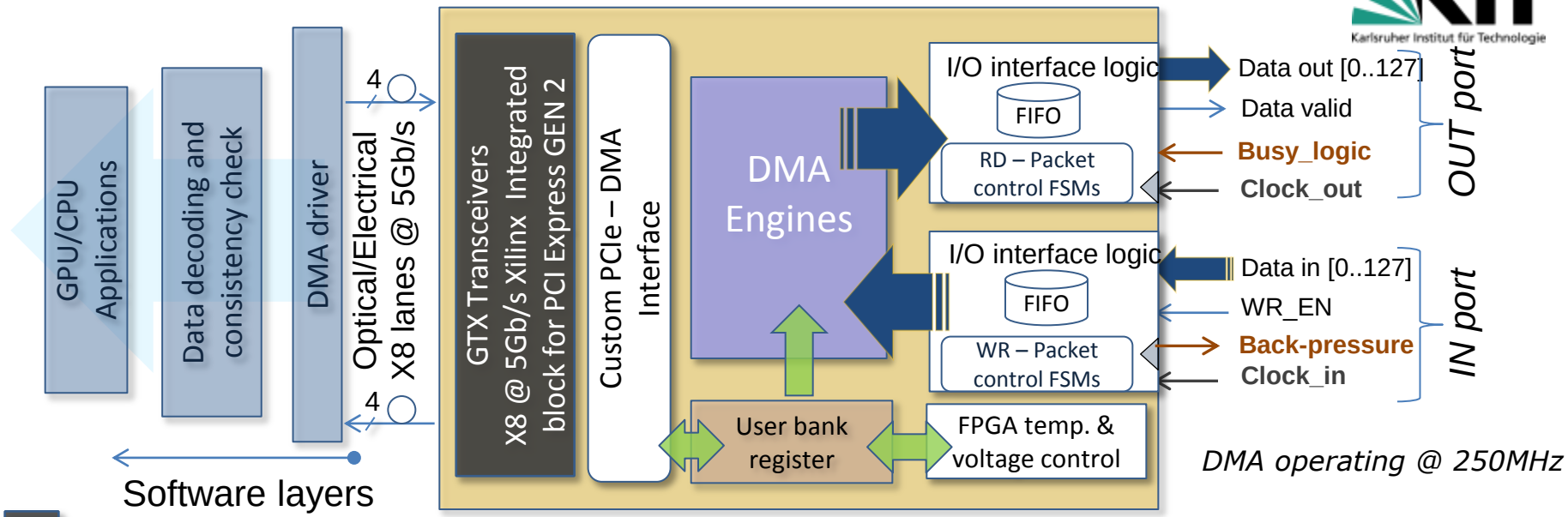
ANKA CSR (long observation time with YBCO HEB detector)



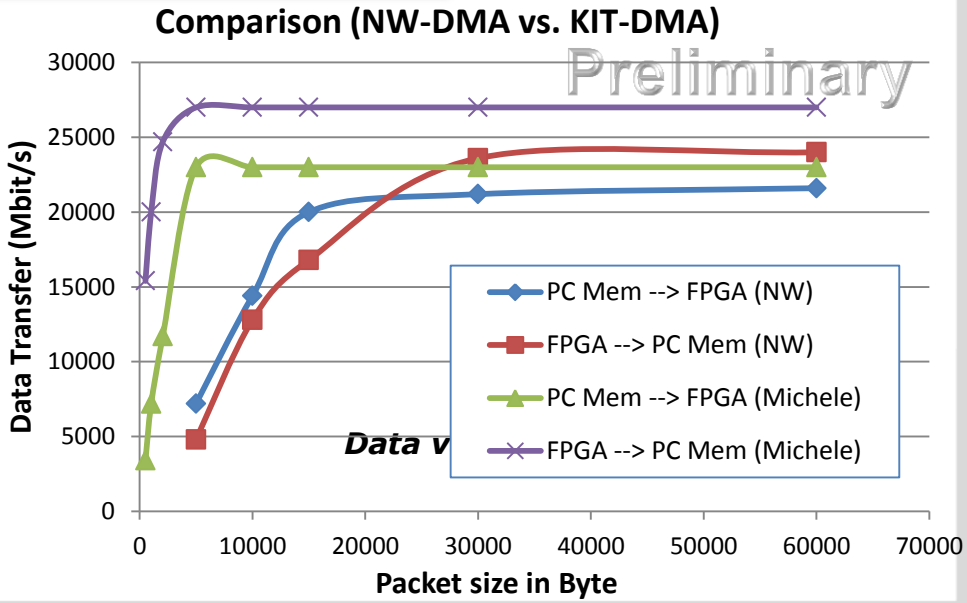
- ✓ Simultaneous turn by turn monitoring of all 184 buckets
- ✓ On-line FPGA/GPU analysis (FFT, time jitter, etc.)
- ✓ Fixed pilot bucket for all measurements
- ✓ Continuously data taking (all bunches all orbits) without dead time

Recording & analysis of time evolution of each bunch

PCIe-Bus Master DMA readout architecture

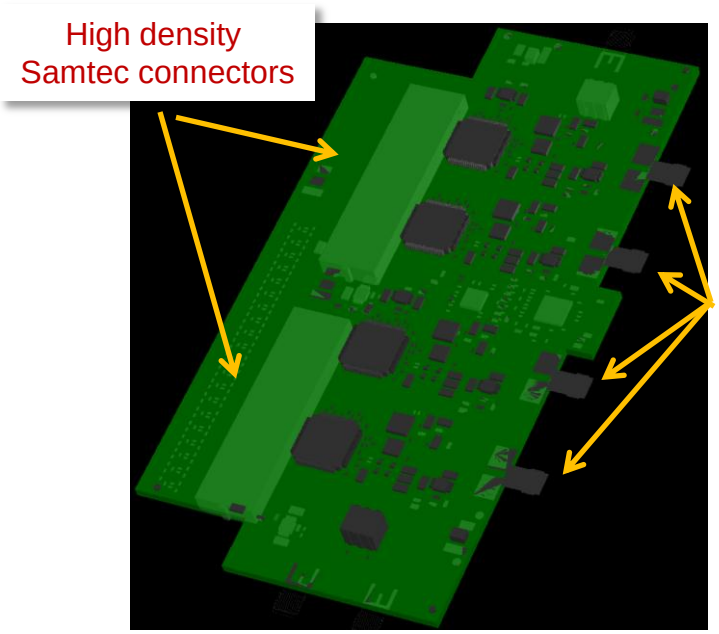


- ✓ Bus Master DMA operating with 8lanes PCIe @ Gen2 (250MHz)
- ✓ Two individual engines for write/read from FPGA (User logic) to PC centre memory
- ✓ IN and OUT FIFO-like interface (for User logic)
- ✓ FIFO used to decouple the time domain between DMA and User custom logic

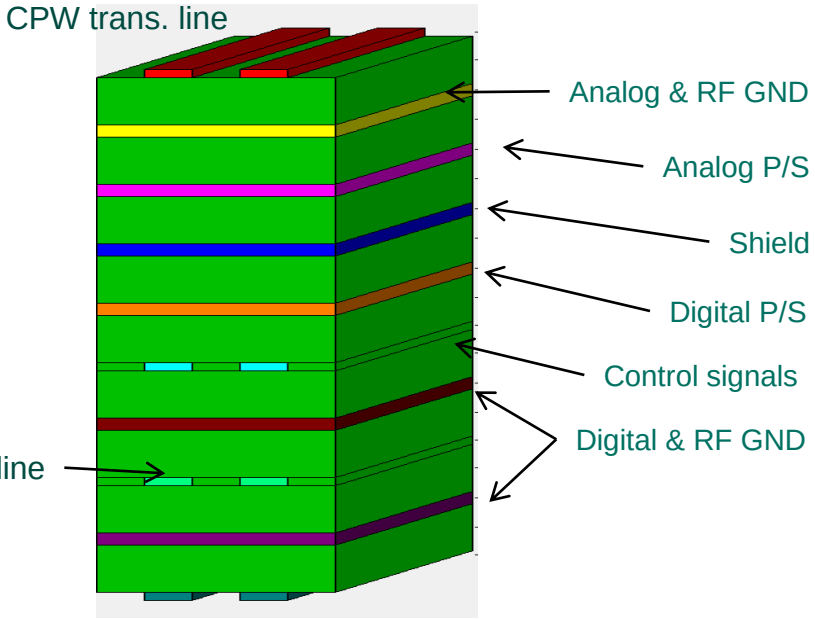


Conclusion & What's next

- 4 channels Fast Pulse shape Sampling board → is completed



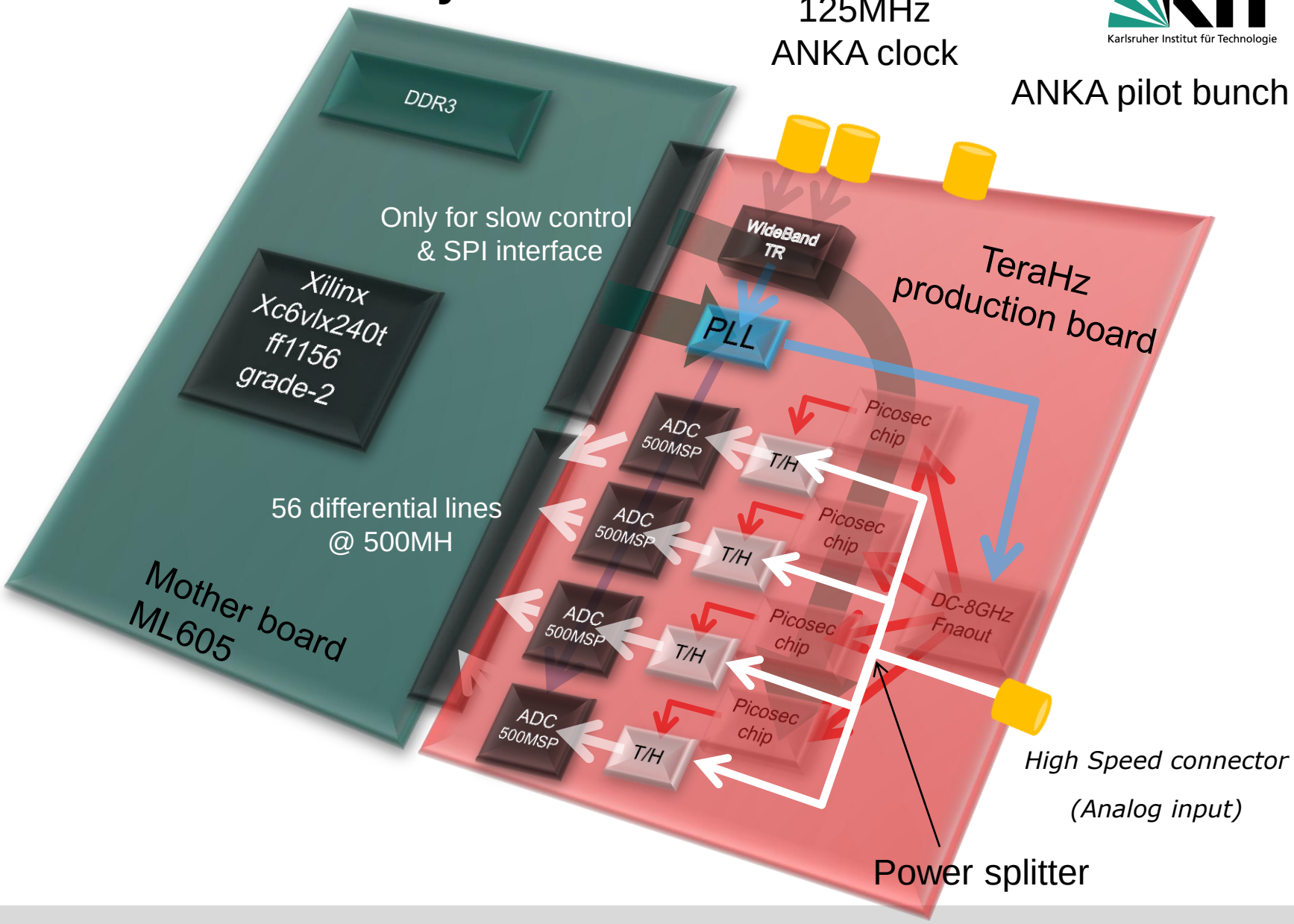
10 layers metal Stack-up



- First board available → mid of February
- Test beam planned → March 2013
- The commissioning for the experimental station → 2013.

Thank you for your attention ….

Production board – Layout



High-band CPW transmission line

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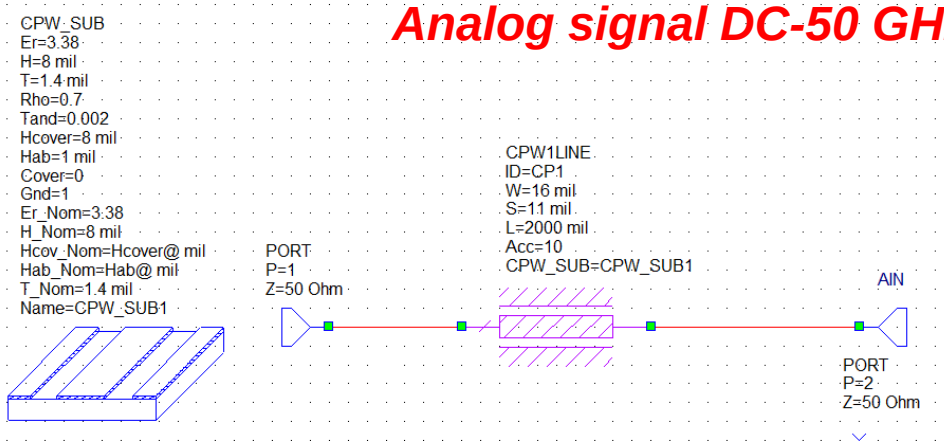
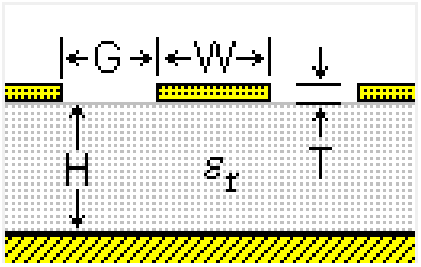
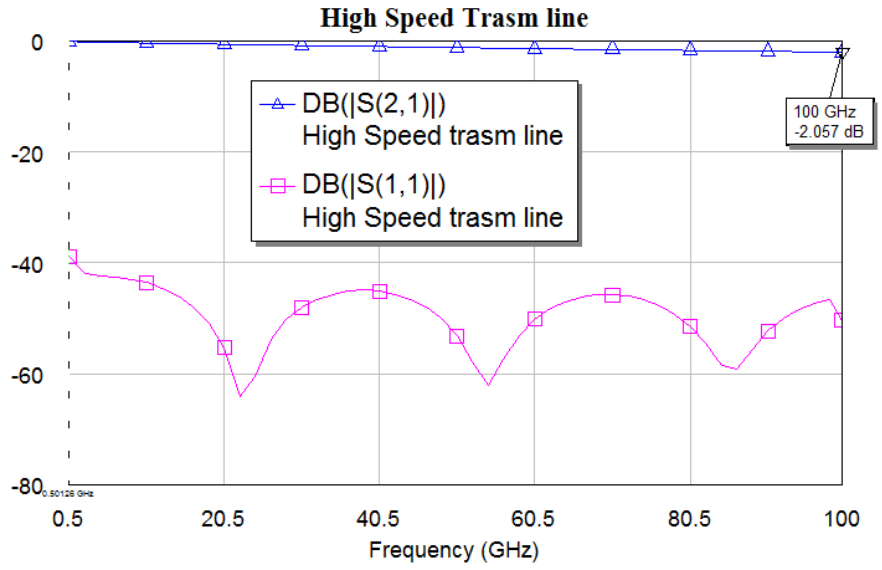
Analog signal DC-50 GHz

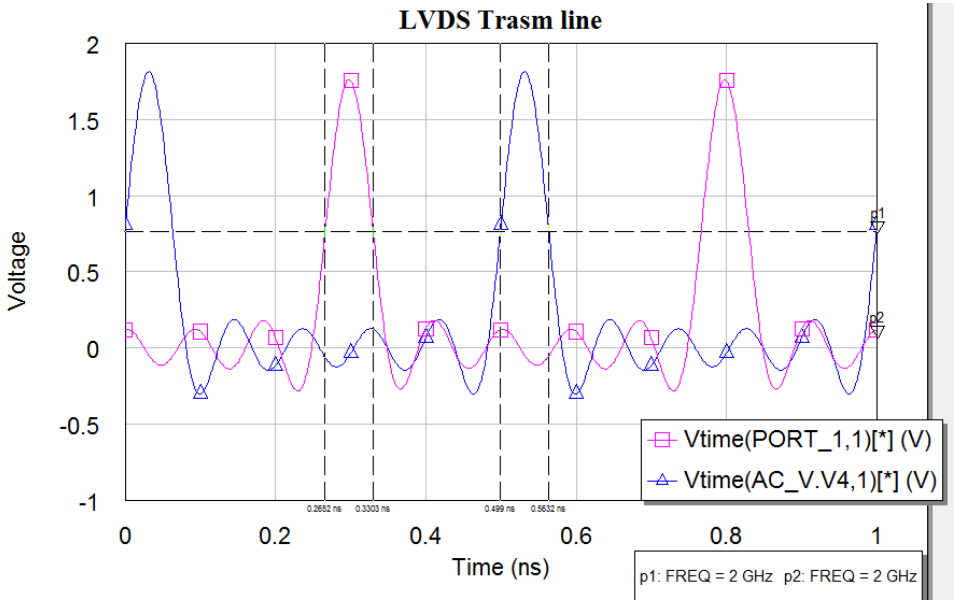




Loss= 38dB/m

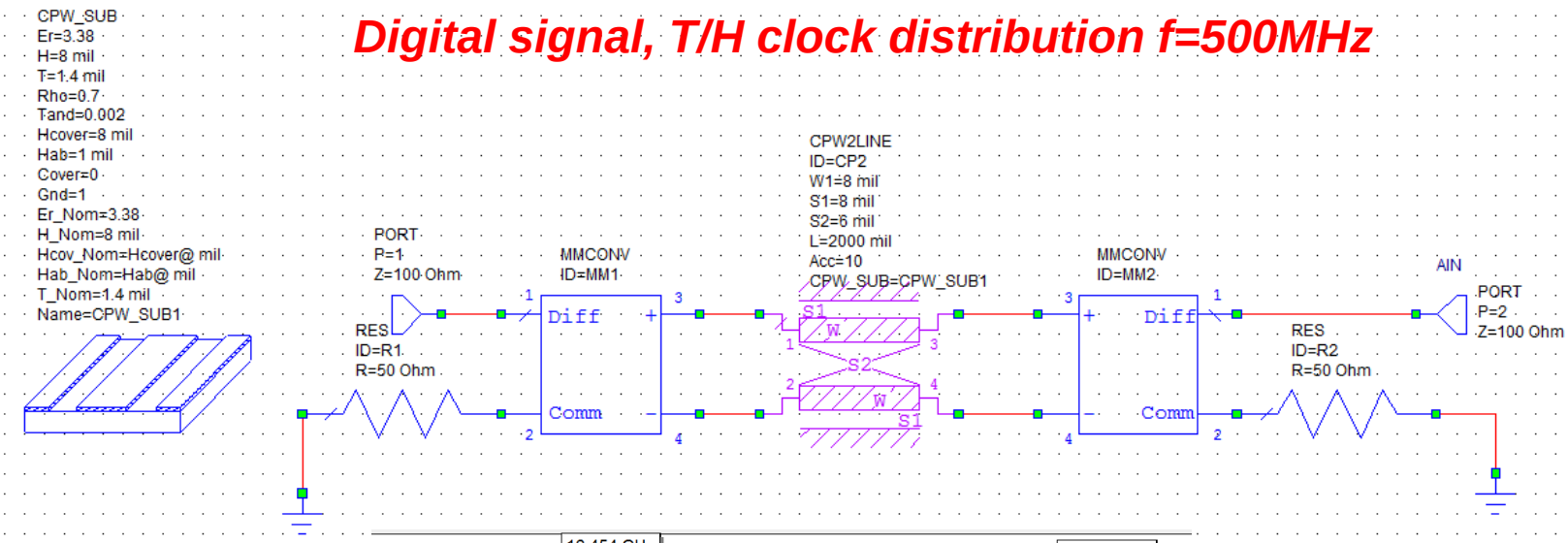
Z0 = 50.7 Ω

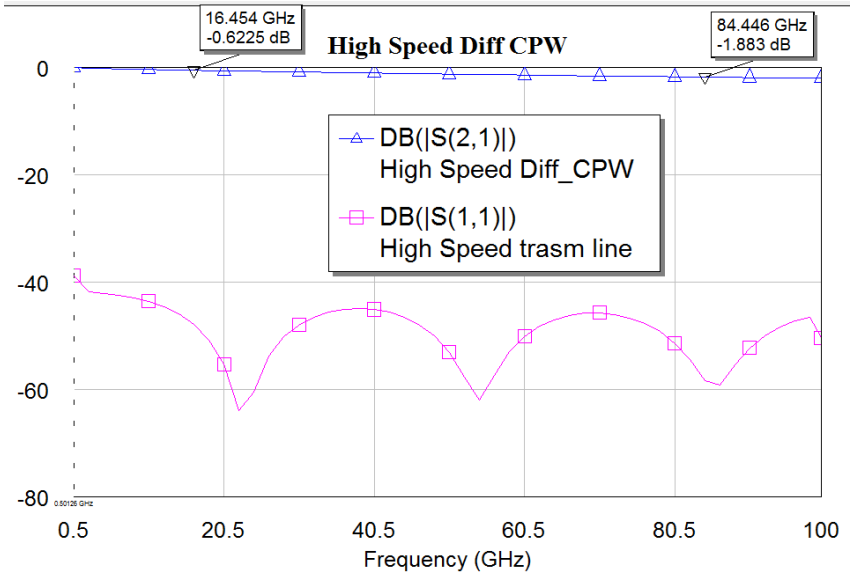




Differential CPW transmission line

Digital signal, T/H clock distribution f=500MHz





Differential Stripline (TL)

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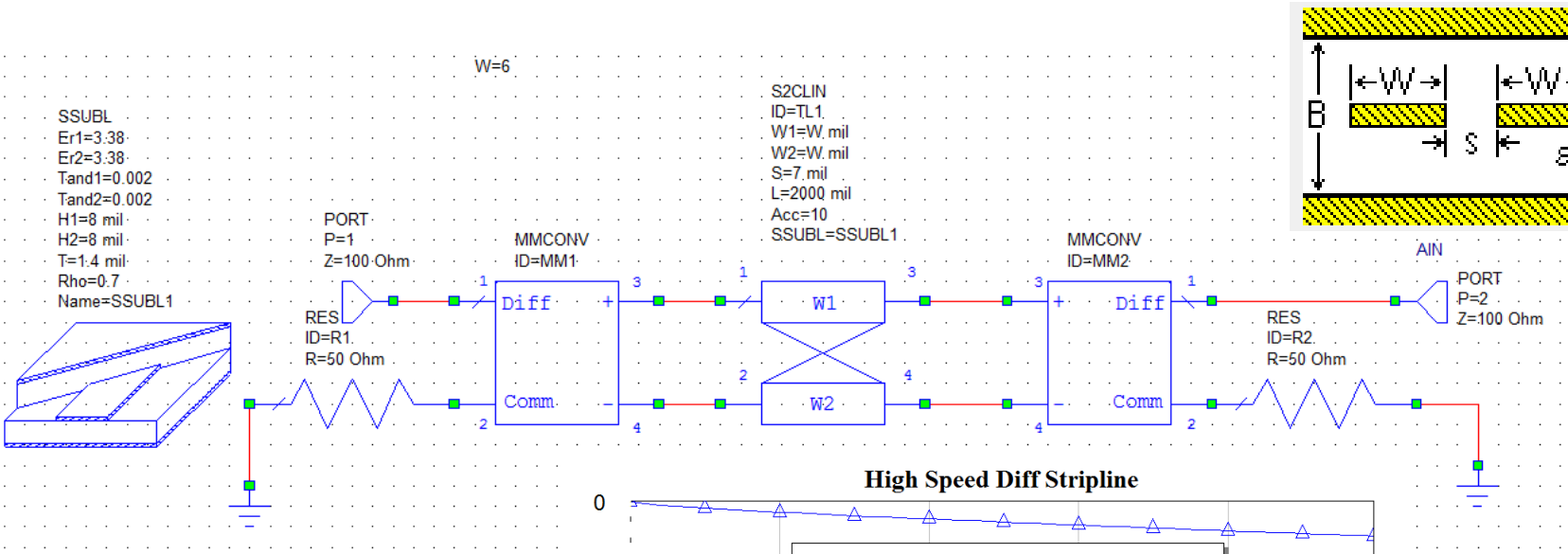
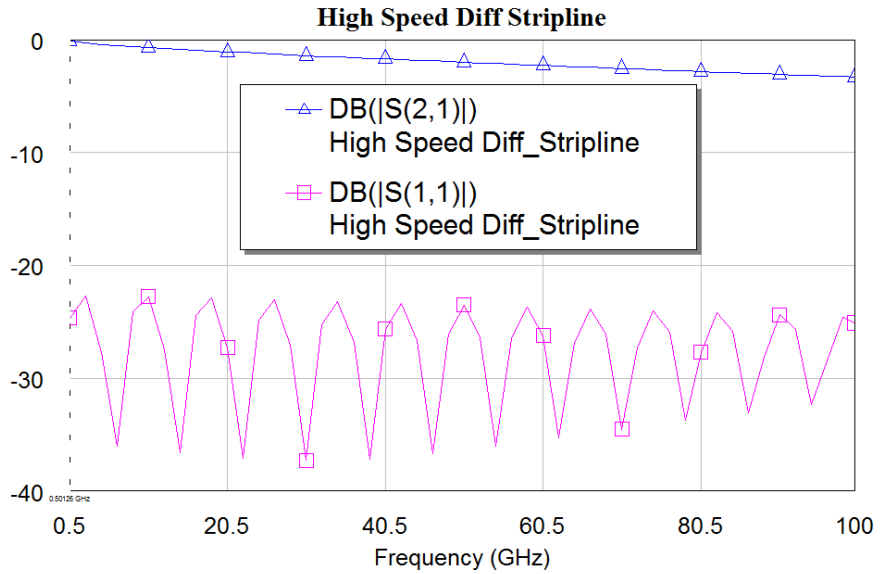
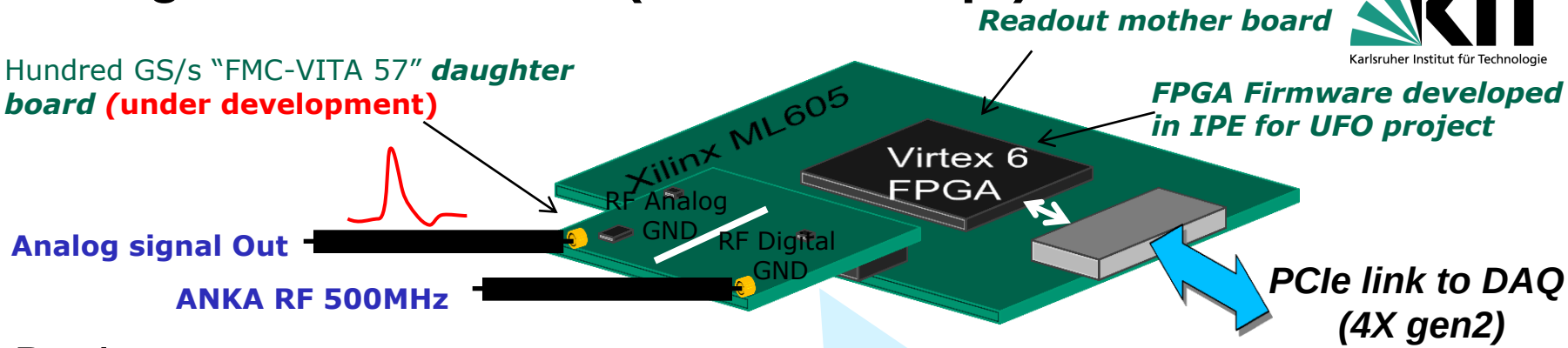
Digital signal, ADC clock distribution f=500MHz

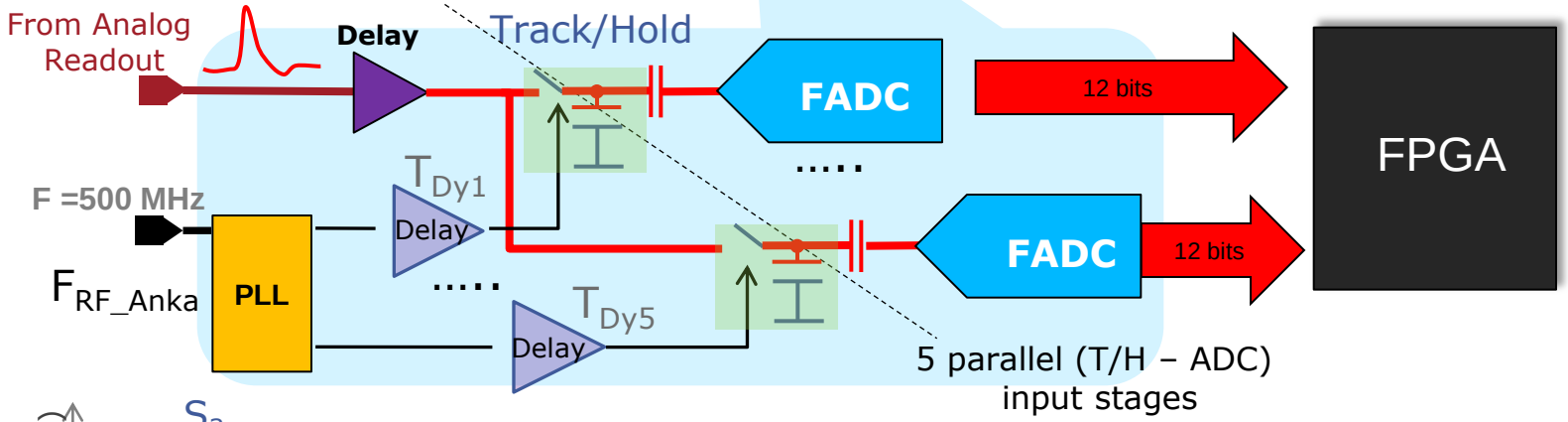


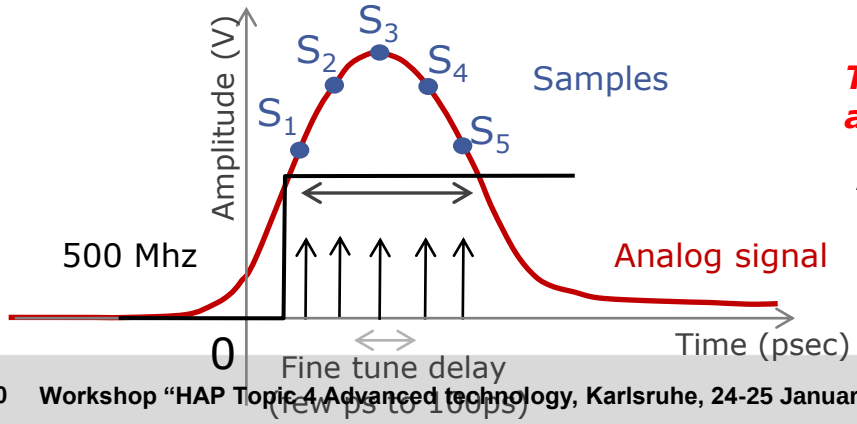


Fast digitalization board (basic concept)



Basic concepts



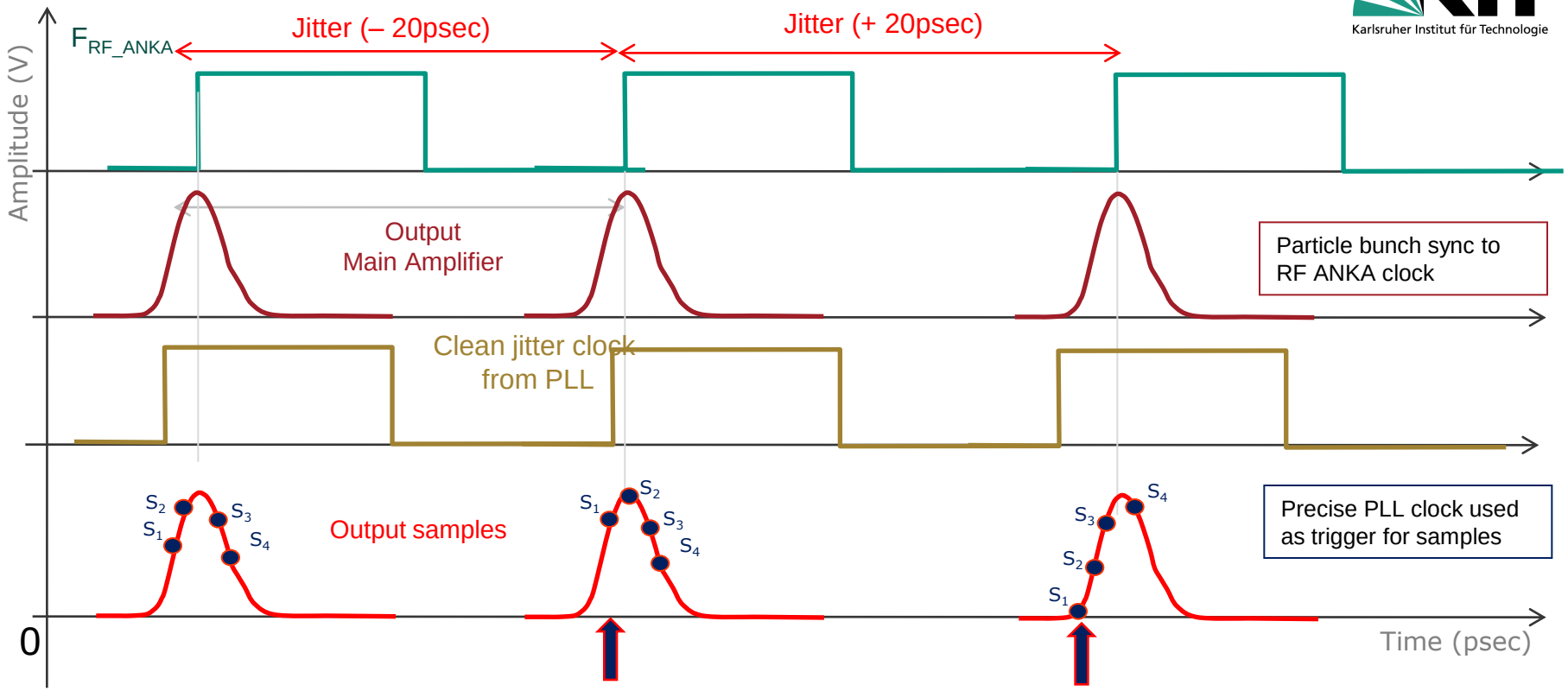


The hundred GS/s concepts → potentially a patent application

A pilot "pre-production" FMC board (a single 500MS/s) under development

Layout and PCB details ***Ref[4]→***

Picosecond time jitter estimation between bunches



Procedure for amplitude and time estimation between buches:

Fast reconstruction of the analog pulse by the 4 samples (FPGA or GPU)

Measuring of the pulse amplitude

Measuring of the time jitter by the position of the samples in the reconstructed pulse