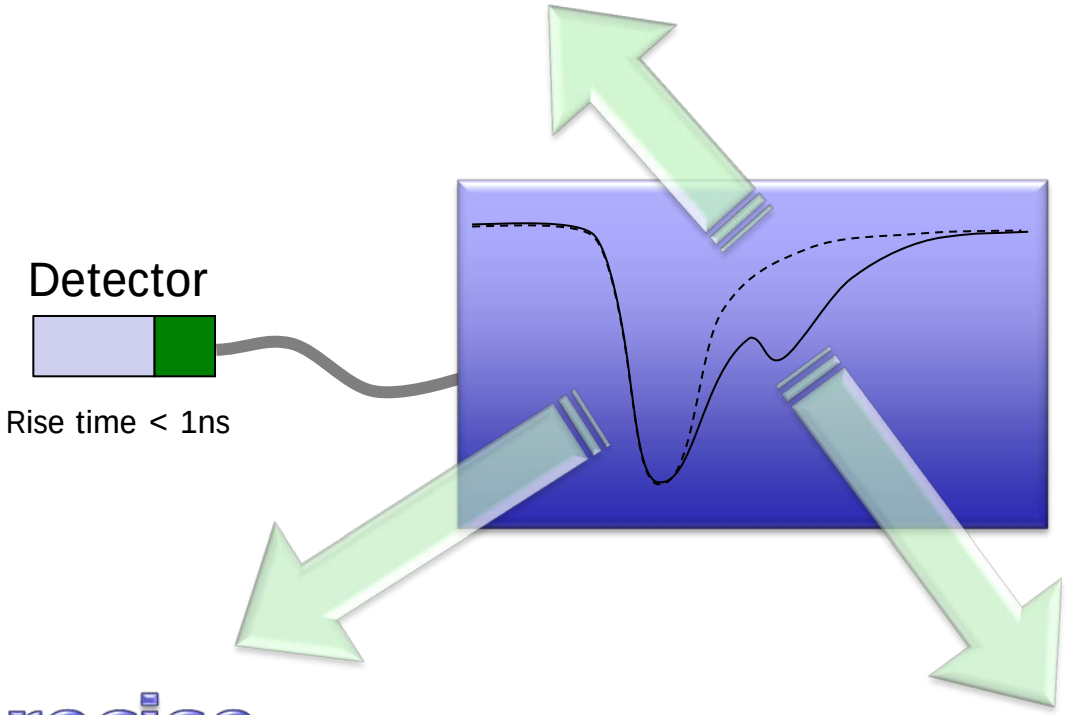
Paul Scherrer Institute
Stefan Ritt

Applications and future of Switched Capacitor Arrays (SCA) for ultrafast waveform digitizing

Why do we need ultrafast waveform digitizing?

Pulse shape discrimination

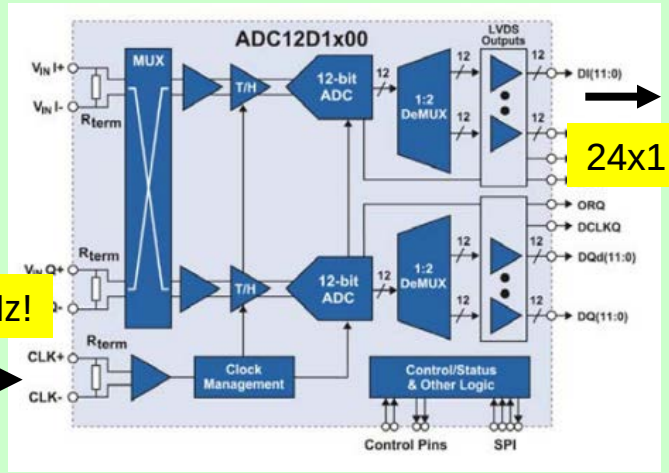


Ultra-precise timing < 10ps

Pile-up recognition

Can it be done with FADCs?

- 8 bits – 3 GS/s – 1.9 W → 24 Gbits/s
- 10 bits – 3 GS/s – 3.6 W → 30 Gbits/s
- 12 bits – 3.6 GS/s – 3.9 W → 43.2 Gbits/s
- 14 bits – 0.4 GS/s – 2.5 W → 5.6 Gbits/s

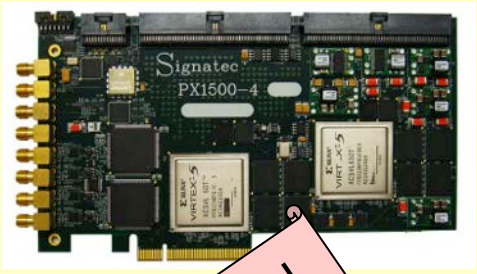


24x1.8 Gbits/s

1.8 GHz!

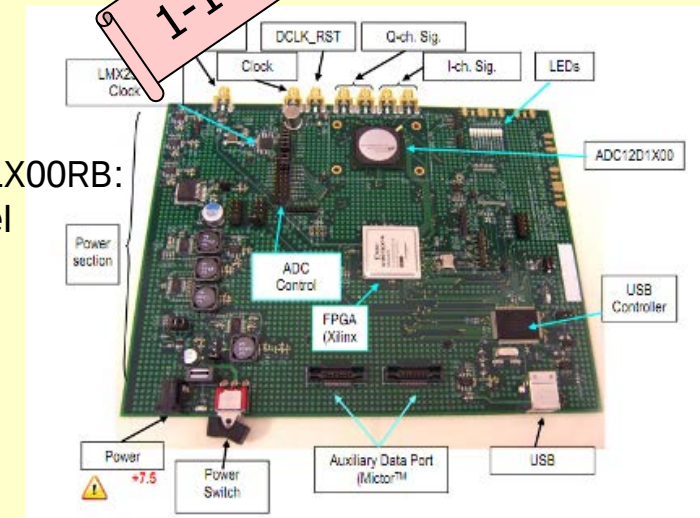
- Requires high-end FPGA
- Complex board design
- FPGA power

PX1500-4:
2 Channel
3 GS/s
8 bits



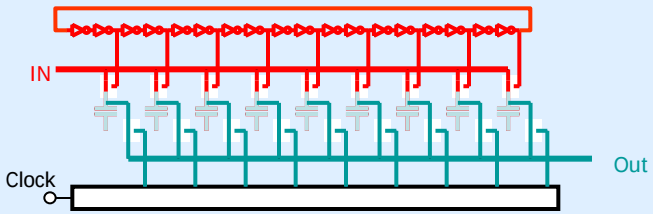
1-10 k€ / channel

ADC12D1X00RB:
1 Channel
1.8 GS/s
12 bits

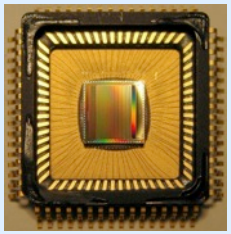


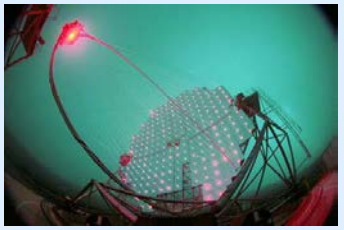
Overview

- Design Principles and Limitations of Switched Capacitor Arrays (SCA)

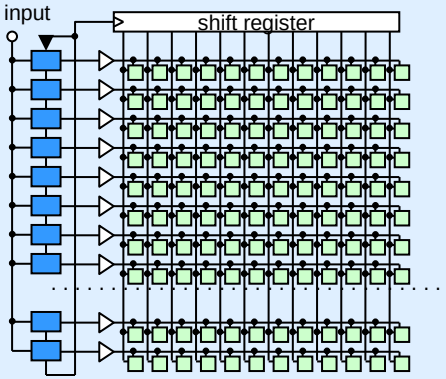


- Overview of Chips and Applications

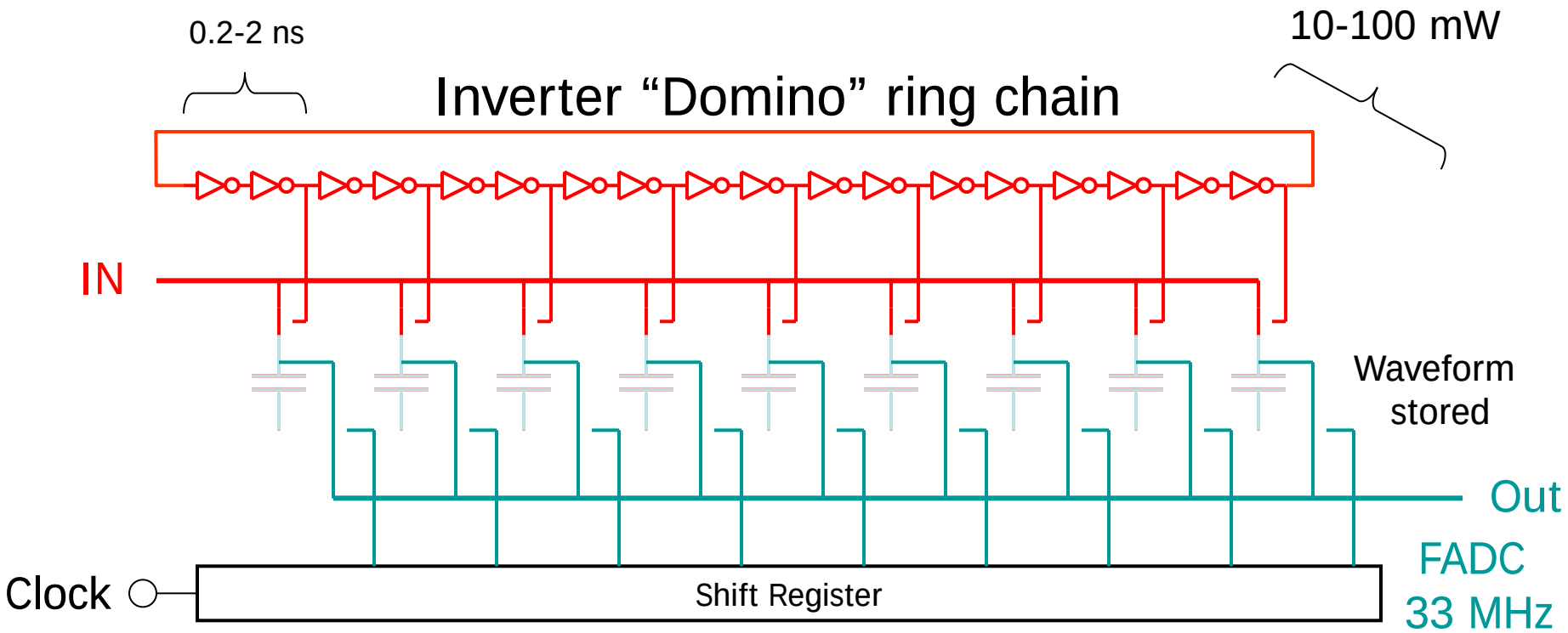




- Future Design Directions

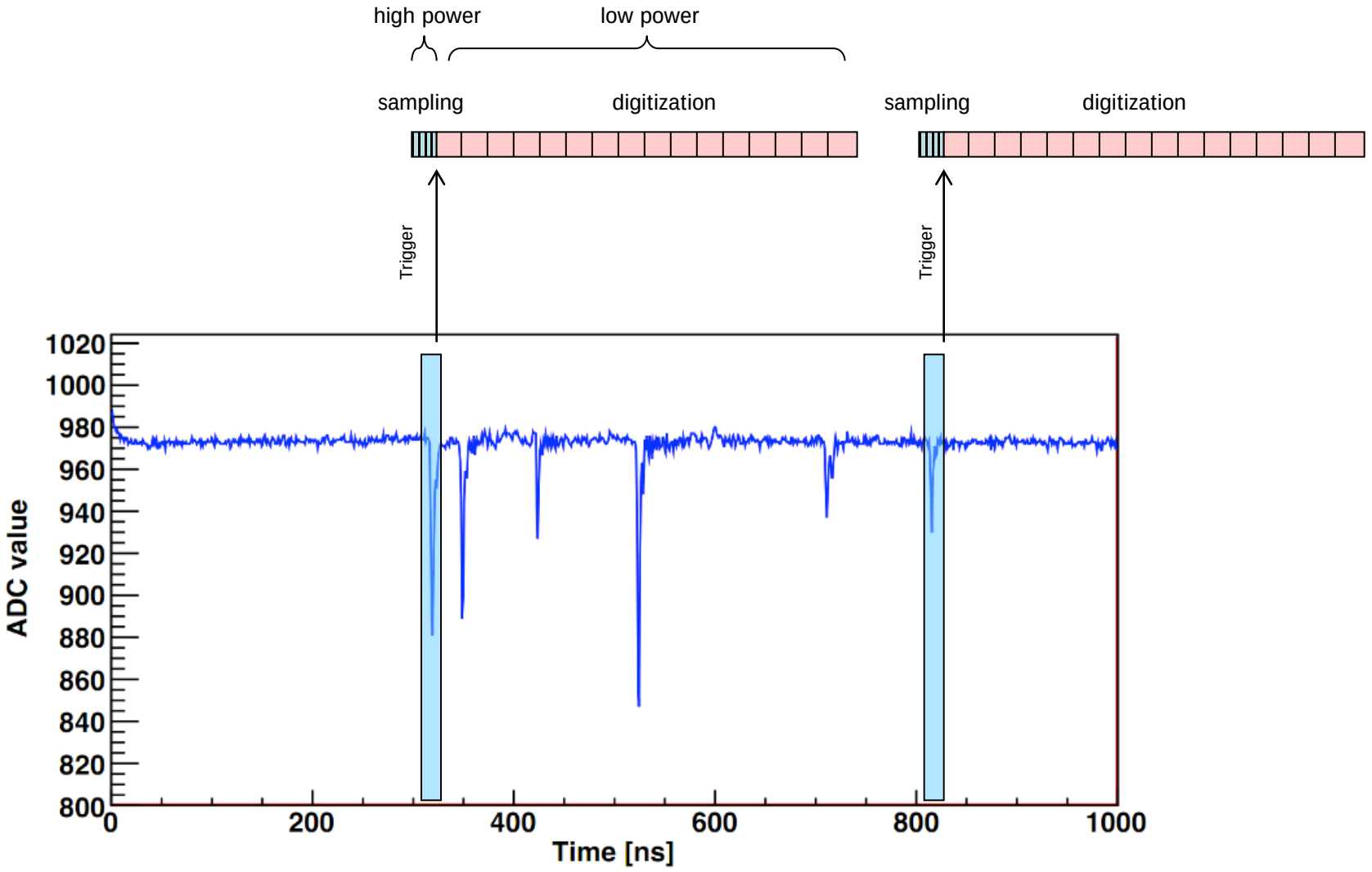


Switched Capacitor Array (Analog Memory)

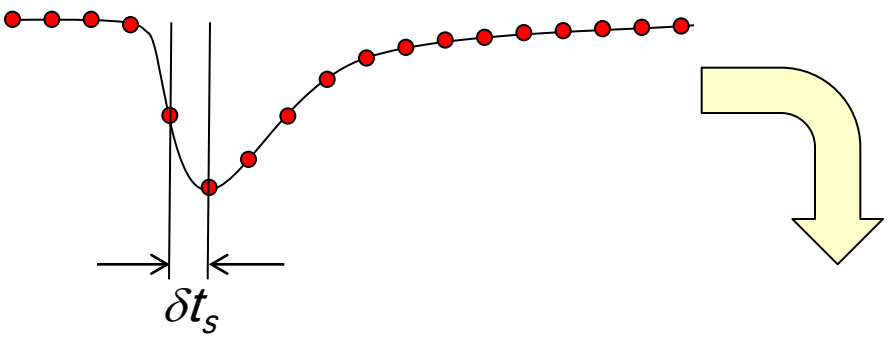


“Time stretcher” GHz → MHz

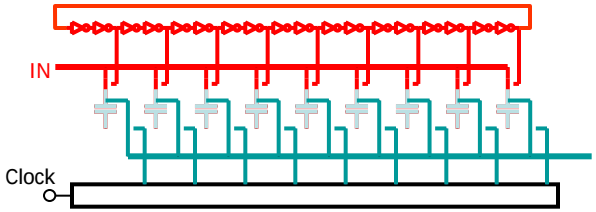
Digitizing only short time windows



Time Stretch Ratio (TSR)



$$TSR \equiv \frac{\delta t_s}{\delta t_d}$$

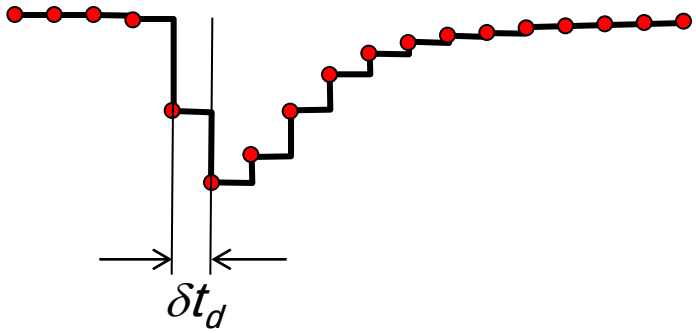


Typical values:

- δt_s = 0.5 ns (2 GSPS)
- δt_d = 30 ns (33 MHz)
  $\rightarrow TSR$ = 60

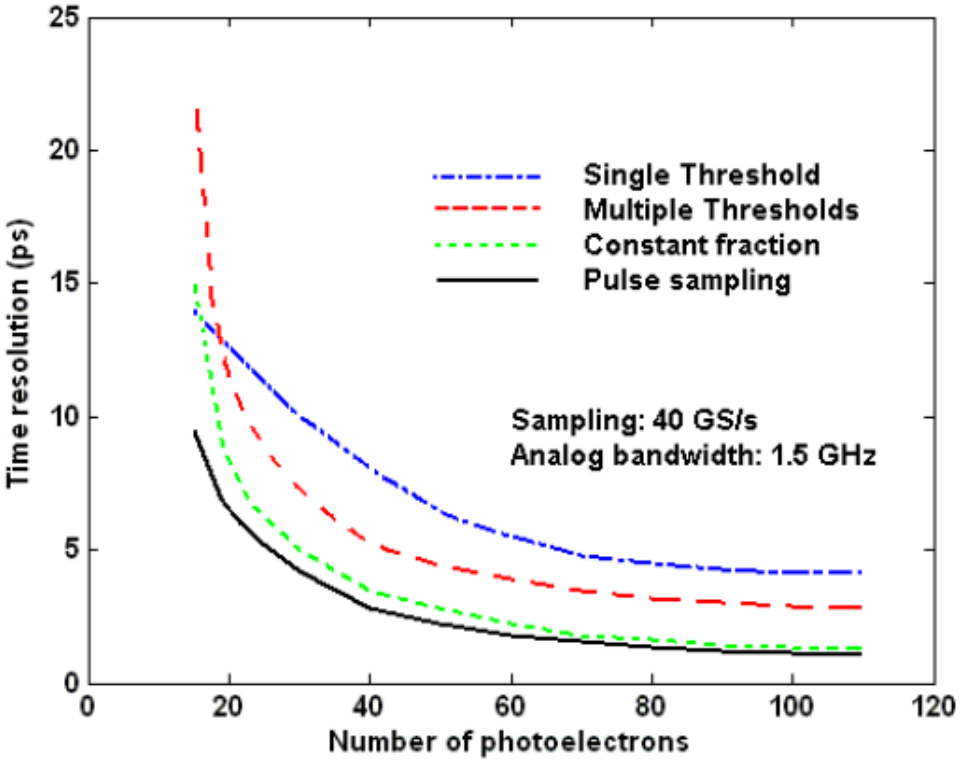
Dead time =
Sampling Window · TSR

(e.g. 100 ns · 60 = 6 μs)



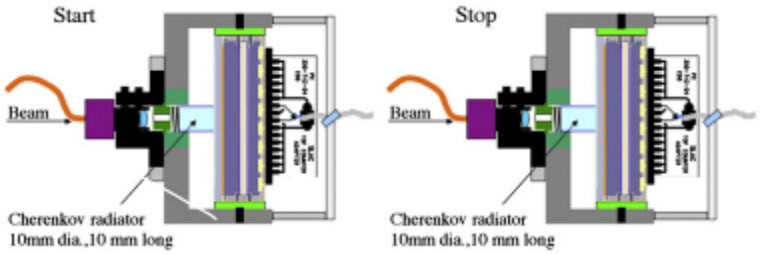
How to measure best timing?

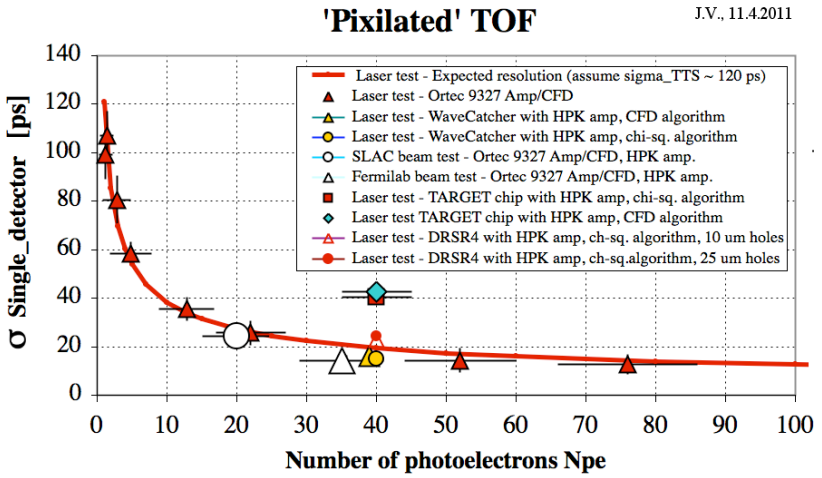
Simulation of MCP with realistic noise and different discriminators



J.-F. Genat et al., arXiv:**0810.5590** (2008)

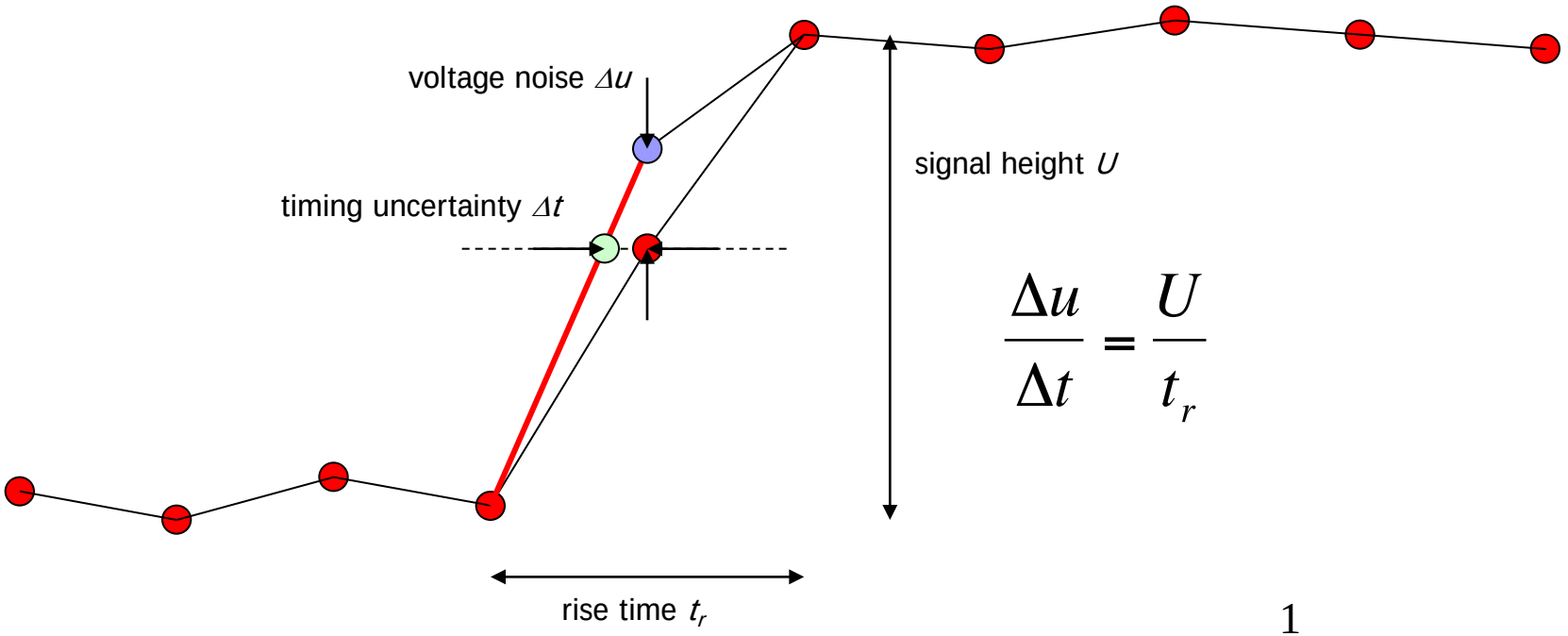
Beam measurement at SLAC & Fermilab





D. Breton et al., NIM **A629**, 123 (2011)

How is timing resolution affected?



$$\frac{\Delta u}{\Delta t} = \frac{U}{t_r}$$

$$t_r \approx \frac{1}{3 f_{3dB}}$$

$$\Delta t = \frac{\Delta u}{U} \cdot t_r = \frac{\Delta u}{U\sqrt{n}} \cdot t_r = \frac{\Delta u}{U} \cdot \frac{t_r}{\sqrt{t_r \cdot f_s}} = \frac{\Delta u}{U} \cdot \frac{\sqrt{t_r}}{\sqrt{f_s}} = \frac{\Delta u}{U} \cdot \frac{1}{\sqrt{3 f_s \cdot f_{3dB}}}$$

number of samples on slope

Simplified estimation!

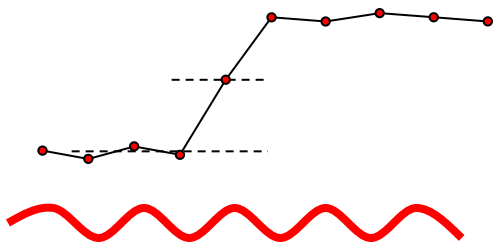
How is timing resolution affected?

$$\Delta t = \frac{\Delta u}{U} \cdot \frac{1}{\sqrt{3 f_s \cdot f_{3dB}}}$$

Assumes zero aperture jitter

	U	Δu	f_s	f_{3db}	Δt
today:	100 mV	1 mV	2 GSPS	300 MHz	~10 ps
optimized SNR:	1 V	1 mV	2 GSPS	300 MHz	1 ps
next generation:	100 mV	1 mV	10 GSPS	3 GHz	1 ps

includes detector noise
in the frequency region of the rise time
and aperture jitter



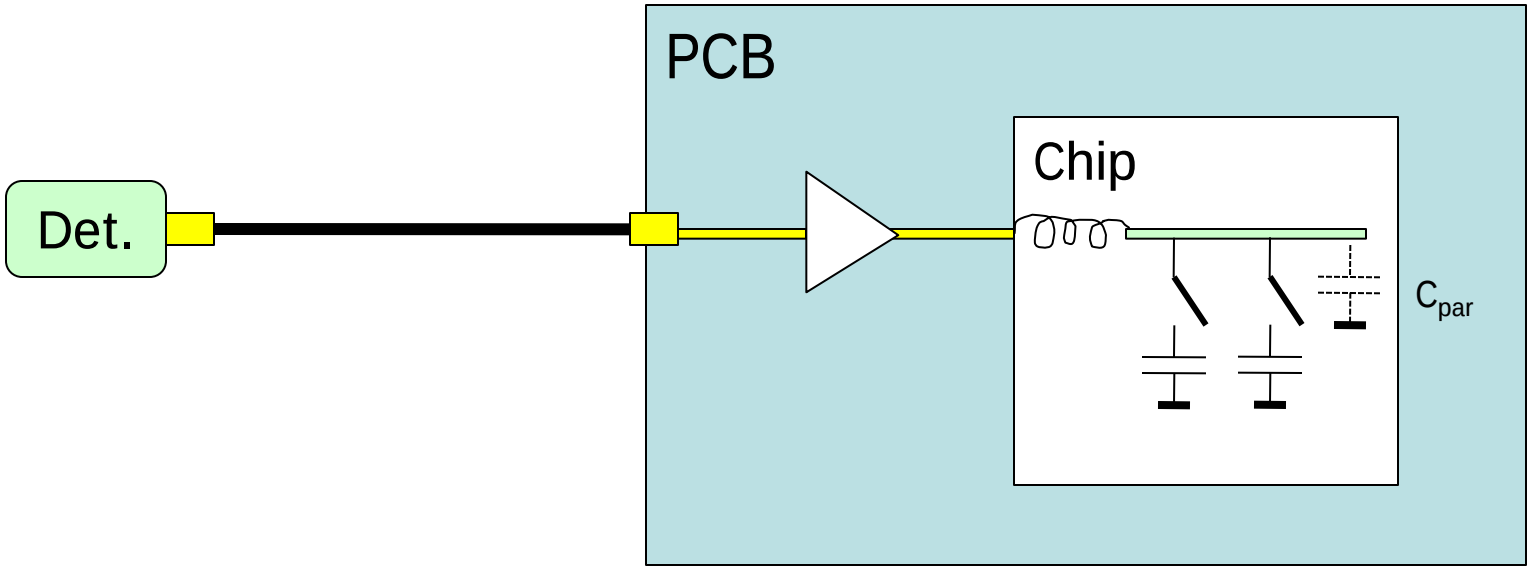
Limits on analog bandwidth

- External sources
  - Detector
  - Cable
  - Connectors
  - PCB
  - Preamplifier
- Internal sources
  - Bond wire
  - Input bus
  - Write switch
  - Storage cap

Low pass filter

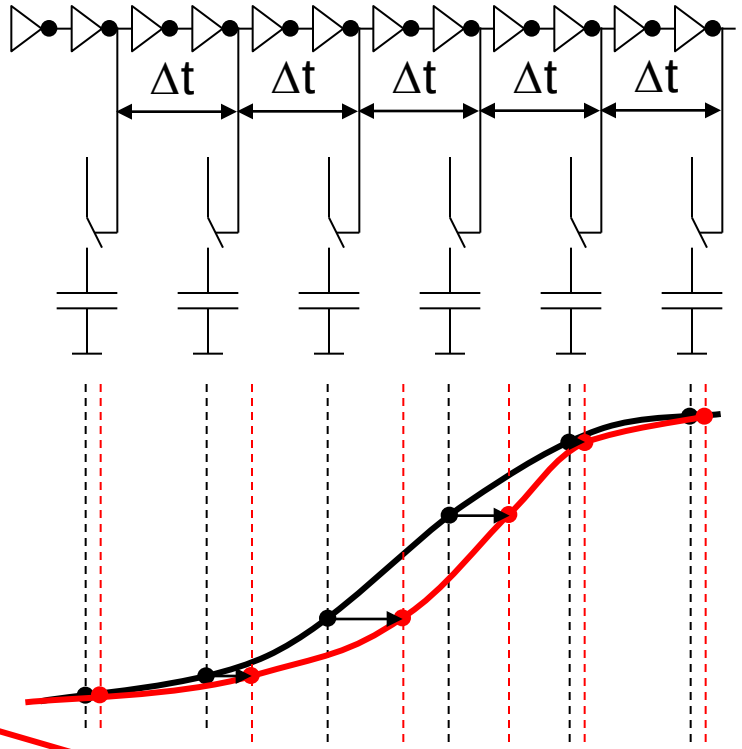
Low pass filter

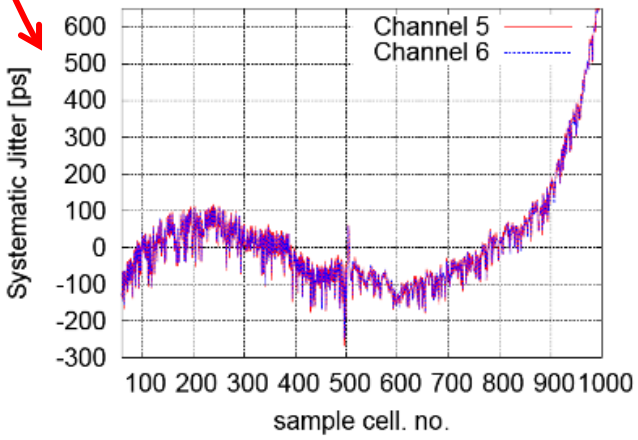
$$f_{3db} = \frac{1}{2\pi RC}$$

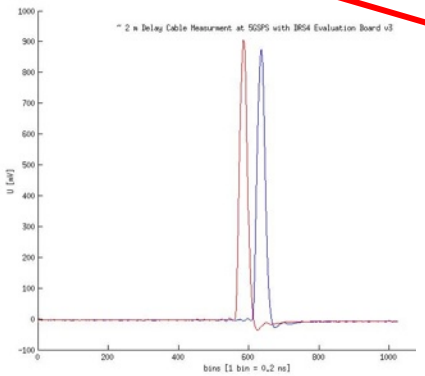


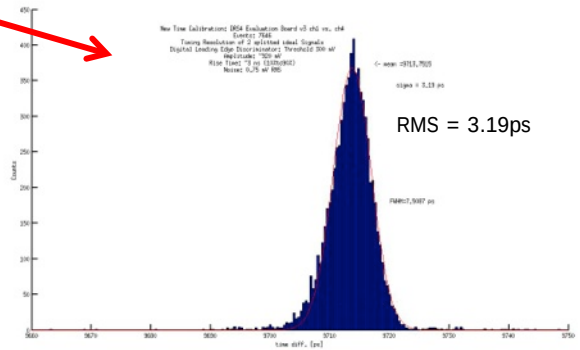
Timing Nonlinearity

- Bin-to-bin variation:
  "differential timing nonlinearity"
- Difference along the whole chip:
  "integral timing nonlinearity"
- Nonlinearity comes from size (doping) of inverters and is stable over time
  → can be calibrated
- Residual random jitter:
  <4 ps RMS exceeds best TDC



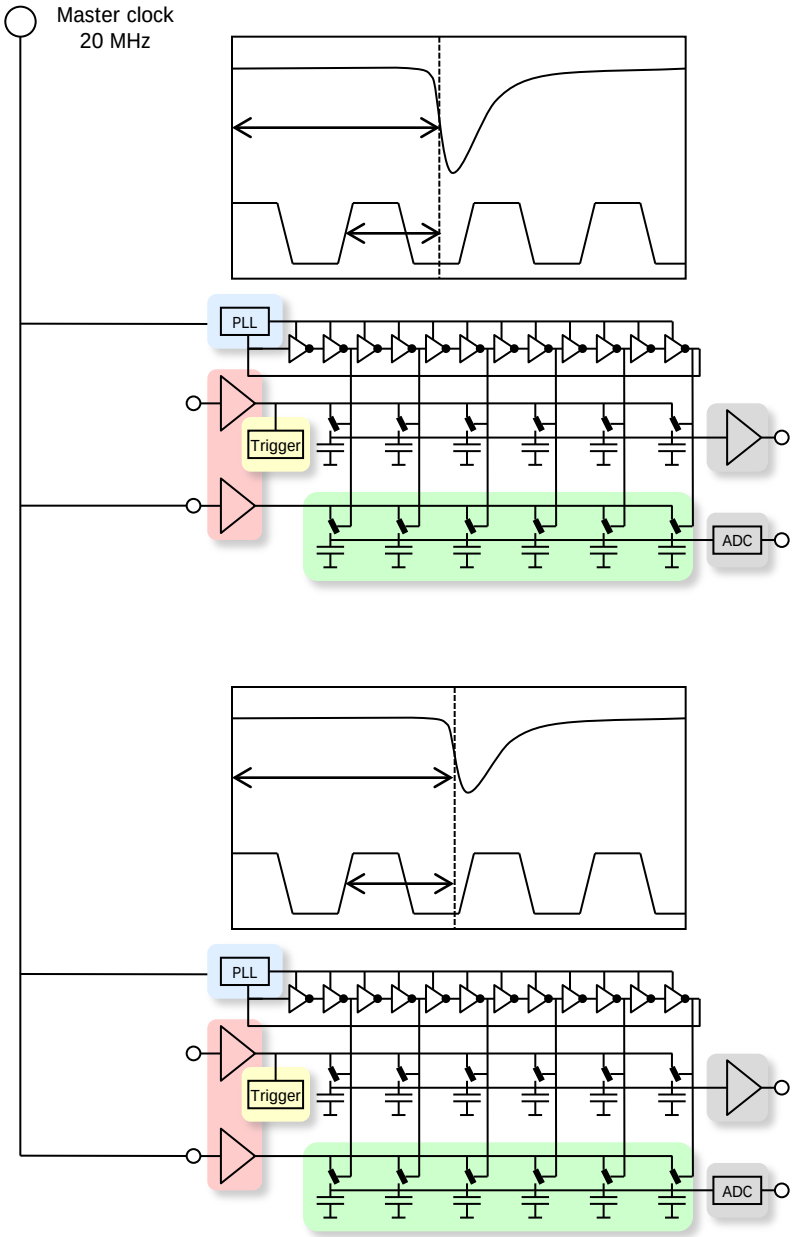


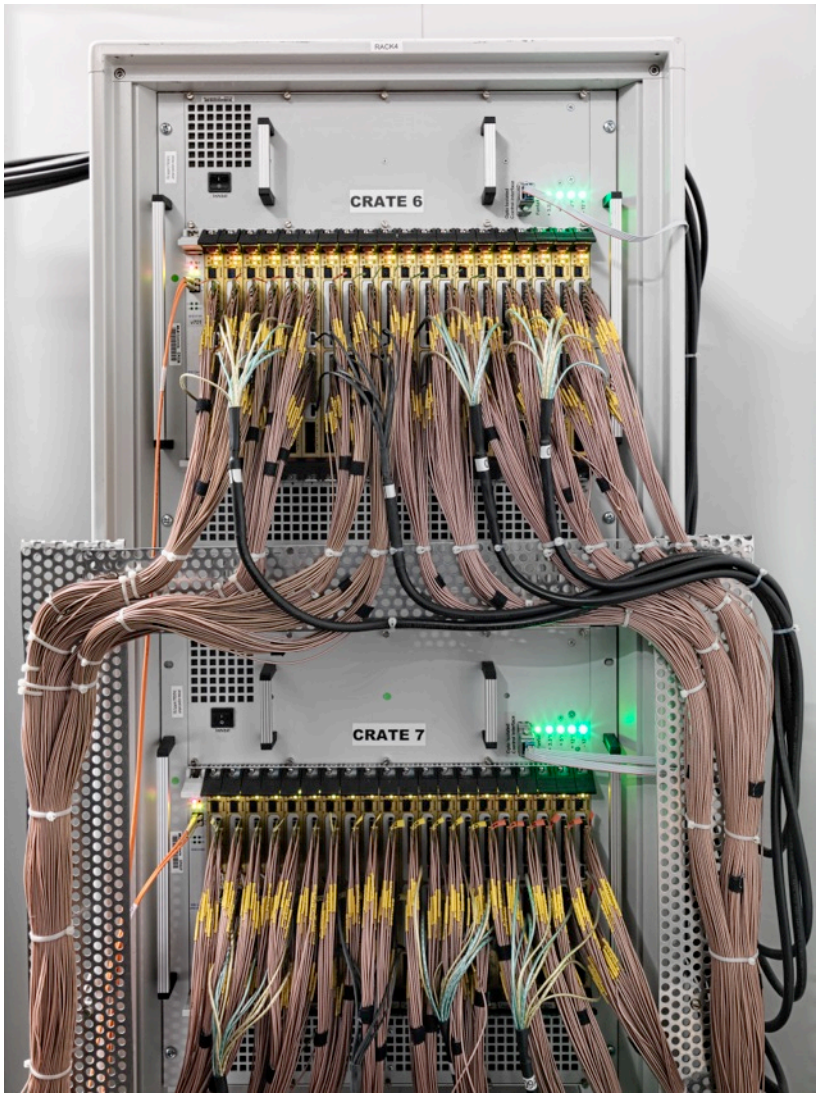




D. Stricker-Shaver, private communication

Synchronization

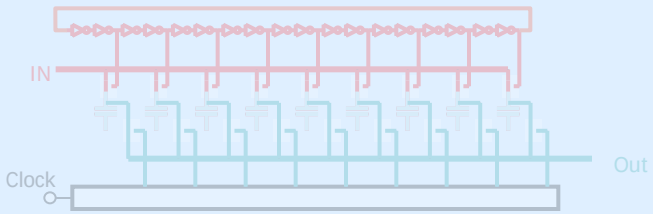




MEG @ PSI: 40 ps over 3000 channels

Part 2

- Design Principles and Limitations



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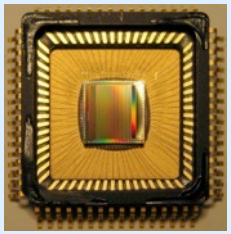
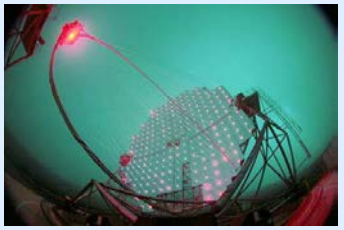
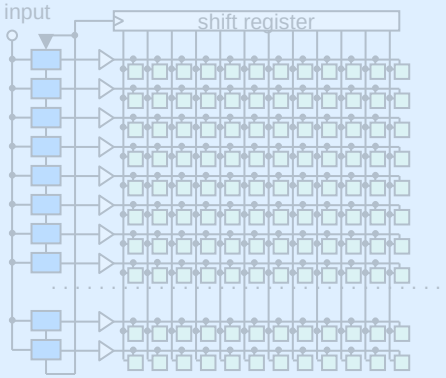


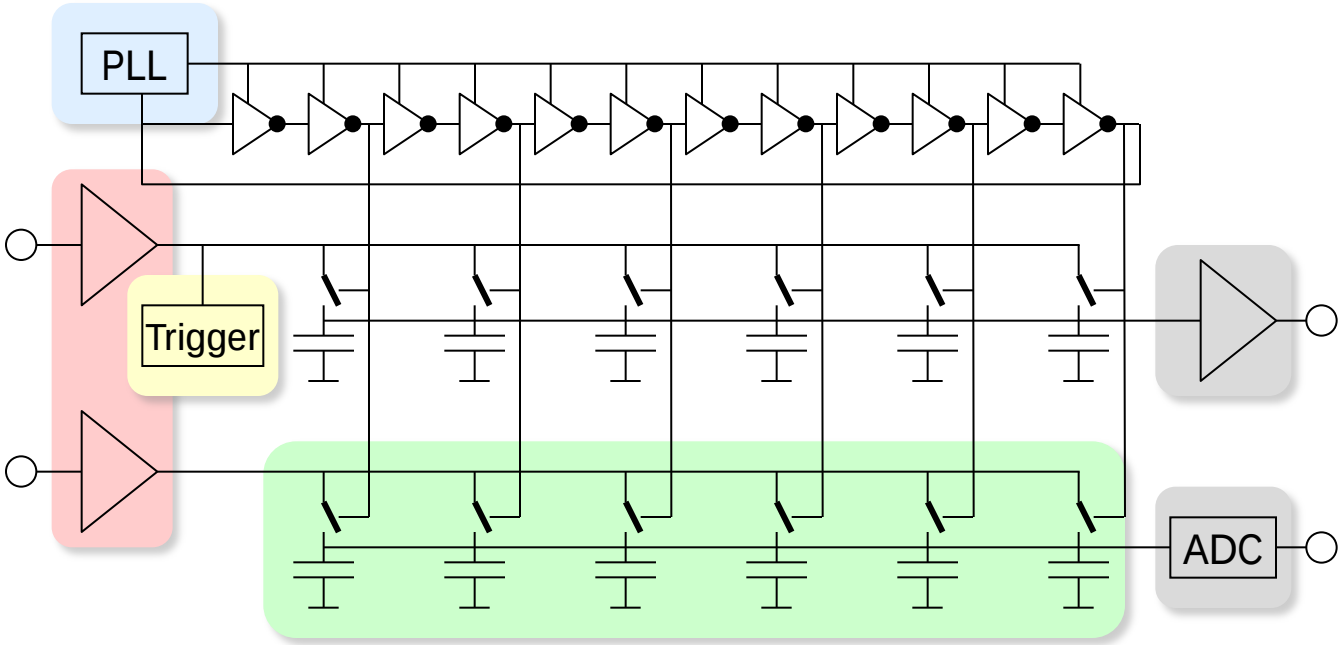


- Future Design Directions

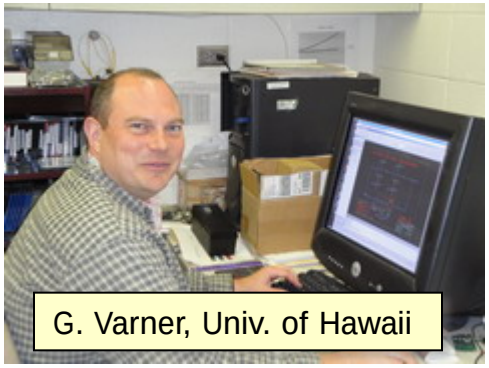


Design Options

- CMOS process (typically 0.35 ... 0.13 μm) → sampling speed
- Number of channels, sampling depth, differential input
- PLL for frequency stabilization
- Input buffer or passive input
- Analog output or (Wilkinson) ADC
- Internal trigger
- Exact design of sampling cell



Switched Capacitor Arrays for Particle Physics

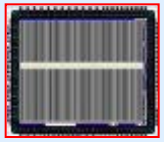


G. Varner, Univ. of Hawaii

E. Delagnes
D. Breton
CEA Saclay

H. Frisch et al., Univ. Chicago

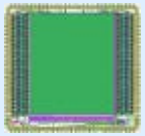
STRAW3 LABRADOR3 TARGET



- 0.25 μm TSMC
- Many chips for different projects (Belle, Anita, IceCube ...)

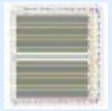
www.phys.hawaii.edu/~idlab/

AFTER SAM NECTAR0



- 0.35 μm AMS
- T2K TPC, Antares, Hess2, CTA

matacq.free.fr

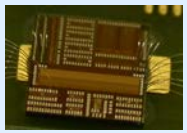


PSEC1 - PSEC4

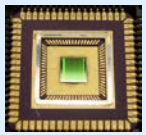
- 0.13 μm IBM
- Large Area Picosecond Photo-Detectors Project (LAPPD)

psec.uchicago.edu

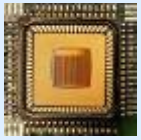
DRS1 DRS2 DRS3 DRS4



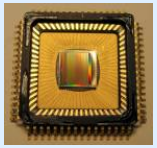
2002



2004



2007



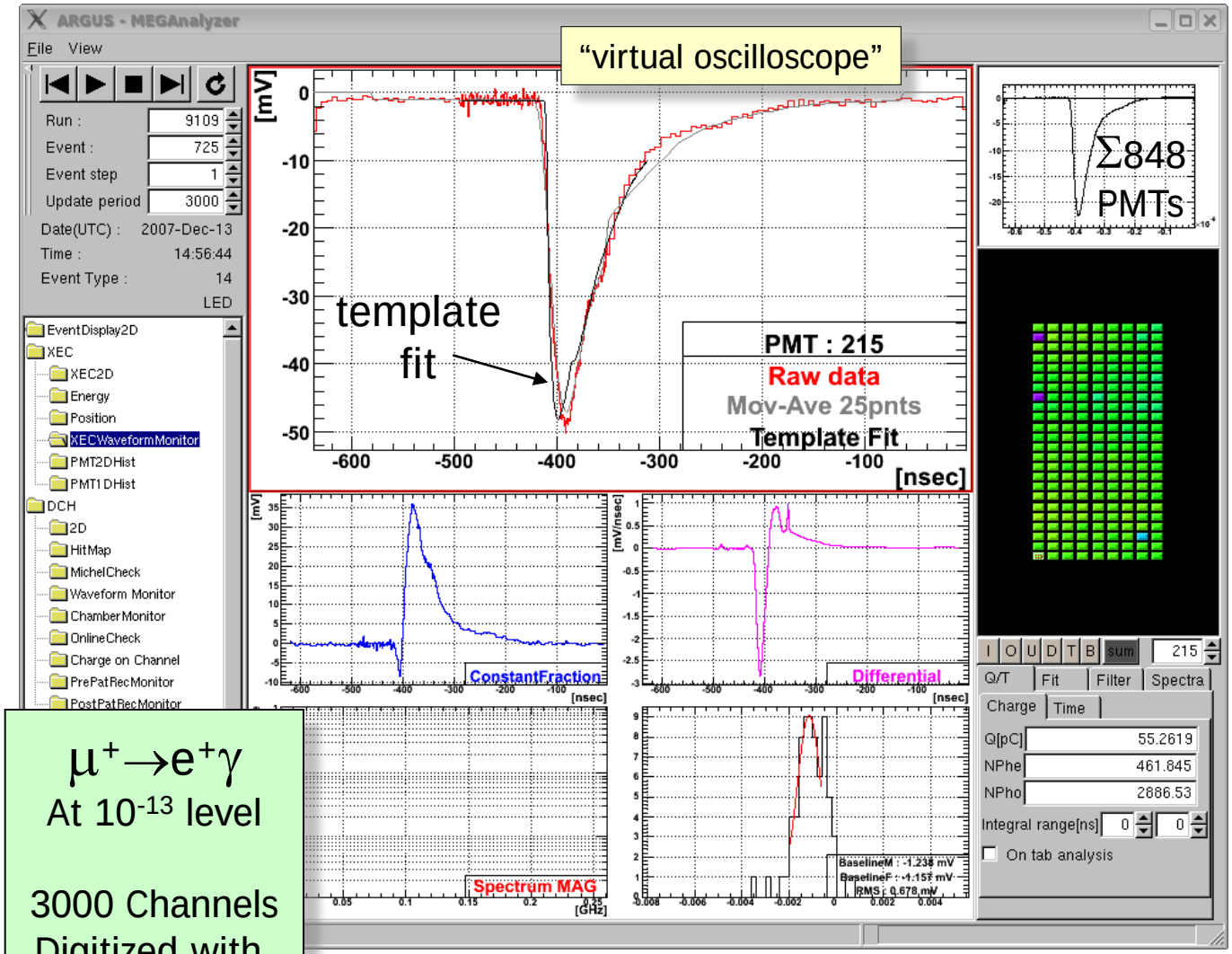
2008

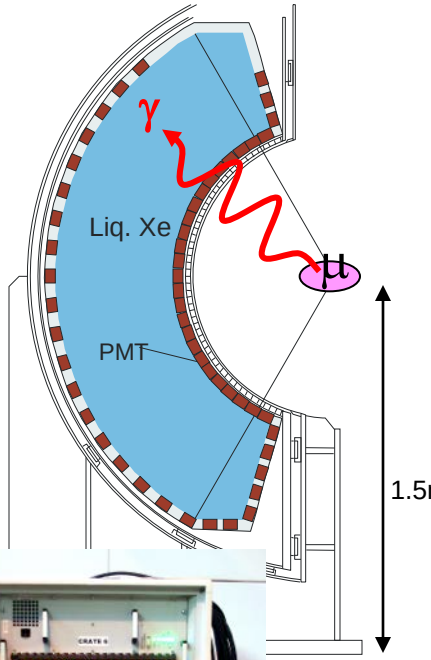
- 0.25 μm UMC
- Universal chip for many applications
- MEG experiment, MAGIC, Veritas, TOF-PET

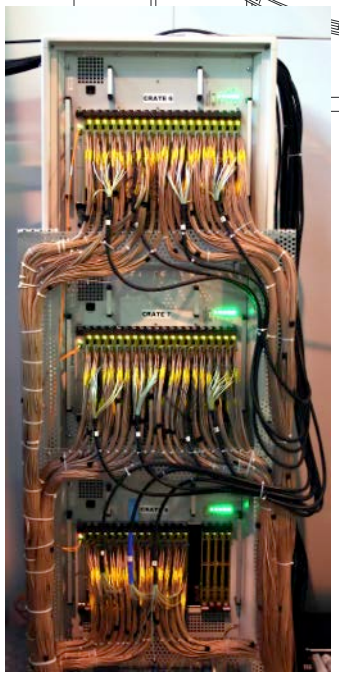
SR
R. Dinapoli
PSI, Switzerland

drs.web.psi.ch

MEG On-line waveform display





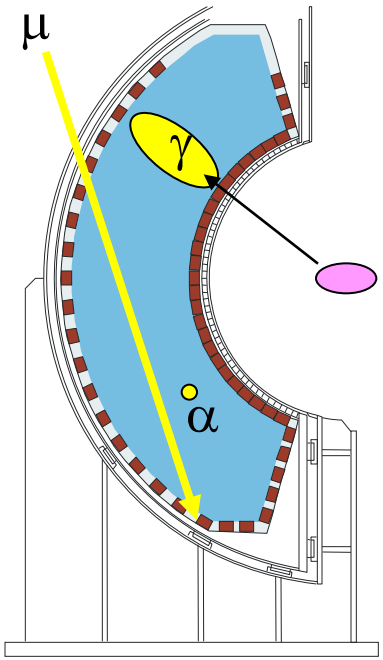


$\mu^+ \rightarrow e^+\gamma$
At 10^{-13} level

3000 Channels Digitized with **DRS4 chips** at 1.6 GSPS

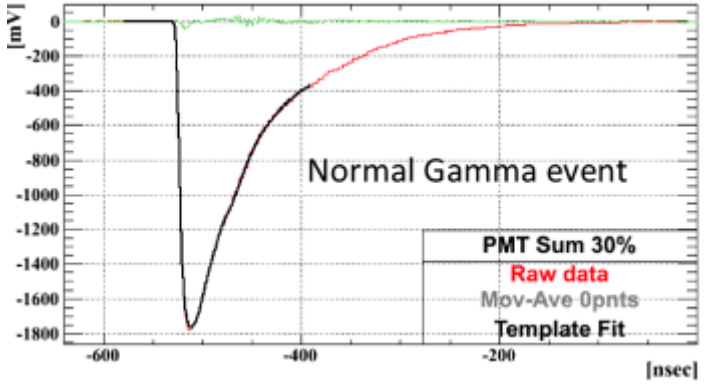
Drawback: 400 TB data/year

Pulse shape discrimination

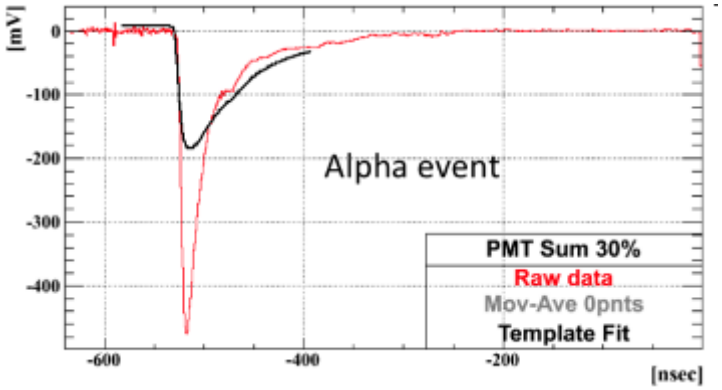


Discovered offline !

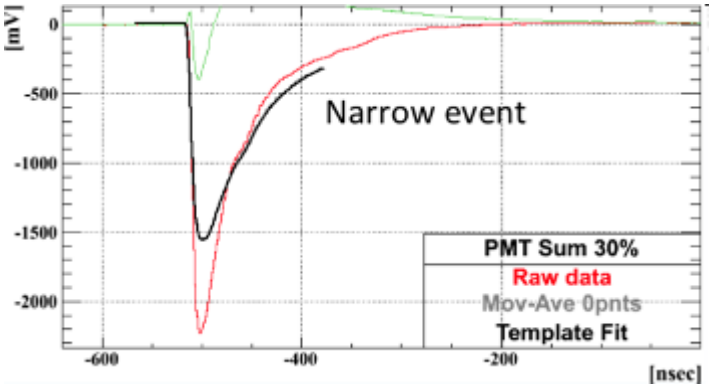
γ



α

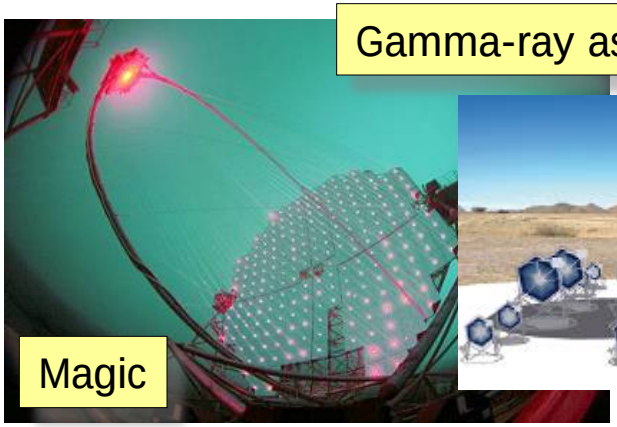


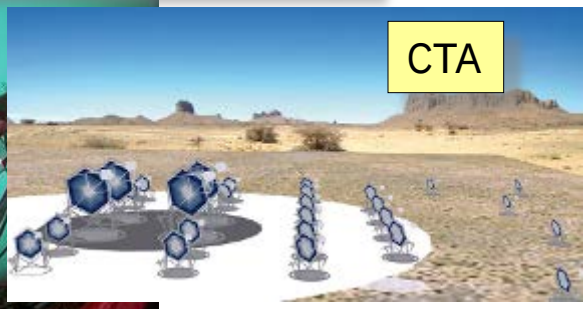
μ

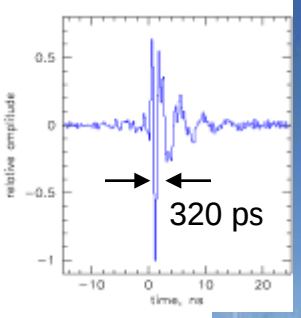


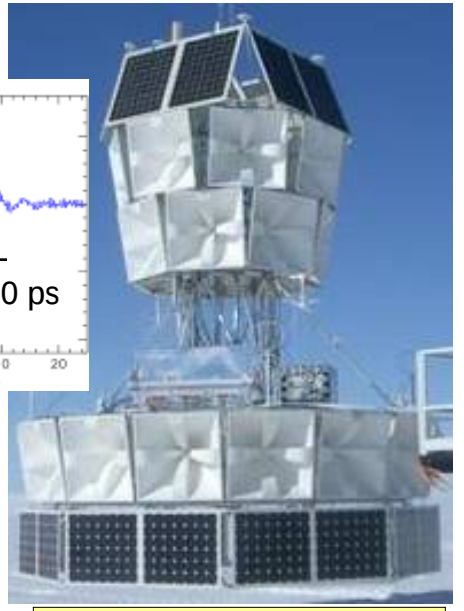
Other Applications

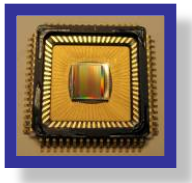
Gamma-ray astronomy

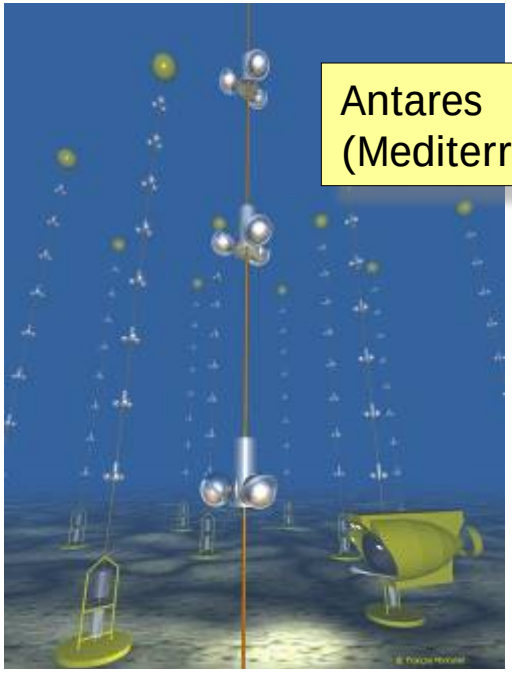






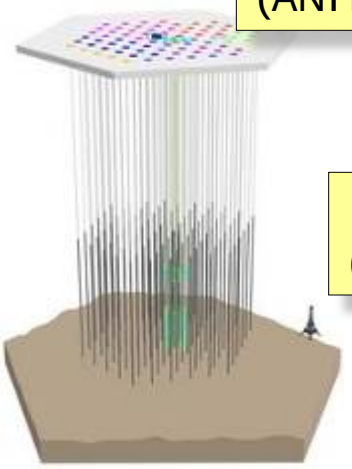






Antares (Mediterranian)

Antarctic Impulsive Transient Antenna (ANITA)

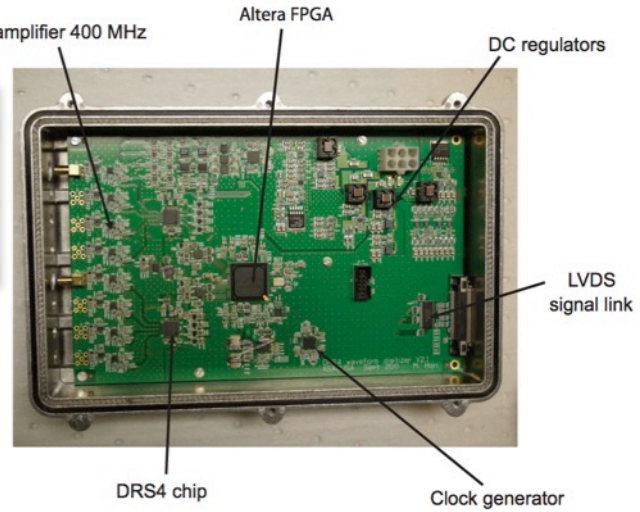


IceCube (Antarctica)

Things you can buy and make

- DRS4 chip (PSI)
- 32+2 channels
- 12 bit 5 GSPS
- > 500 MHz analog BW
- 1024 sample points/chn.
- 110 µs dead time

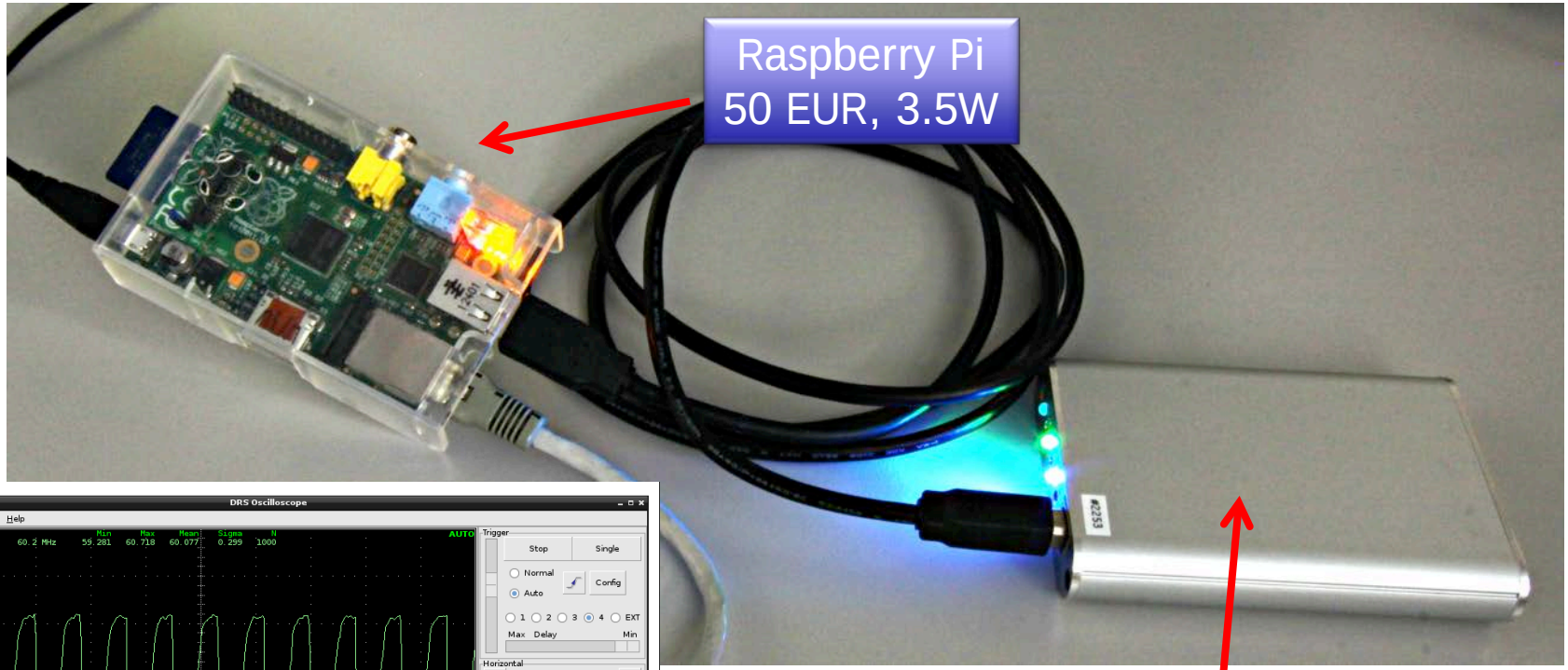
- M. Hori (CERN)
- DRS4 chip
- 8 channels
- LVDS links

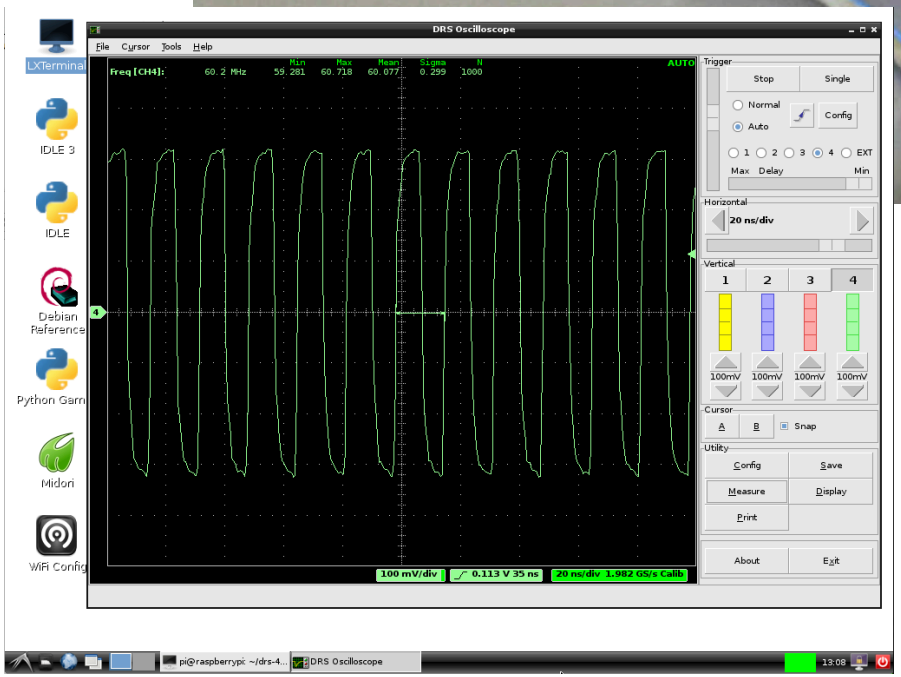


- DRS4 Evaluation Board
- 4 channels
- 12 bit 5 GSPS
- 750 MHz analog BW
- 1024 sample points/chn.
- 500 events/sec over USB 2.0

- SAM Chip (CEA/IN2PD)
- 2 channels
- 12 bit 3.2 GSPS
- 300 MHz analog BW
- 256 sample points/chn.
- On-board spectroscopy

The smallest DAQ system



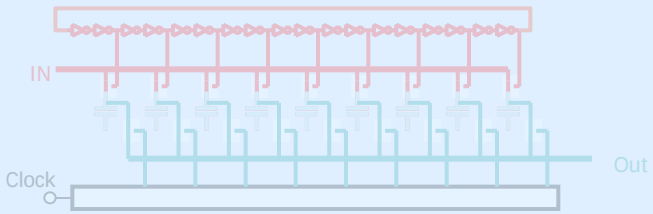


DRS4 Evaluation Board
900 EUR, 2.5W

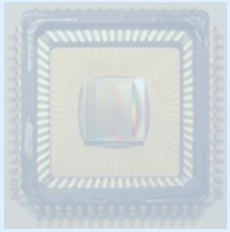
Idea: Martin Brückner HU Berlin for HiSCORE

Part 3

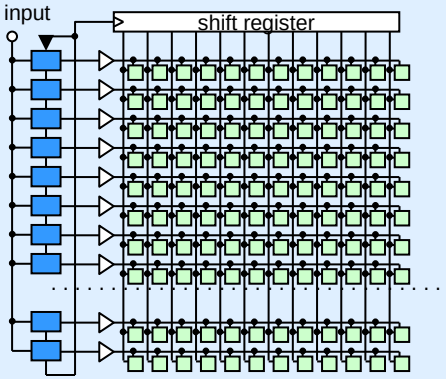
- Design Principles and Limitations



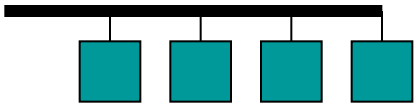
- Overview of Chips and Applications

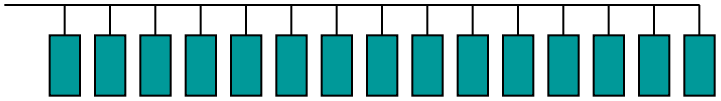


- Future Design Directions

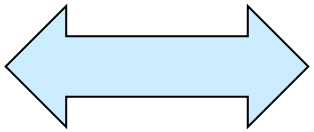


Next Generation SCA





Short sampling depth



Deep sampling depth

- Low parasitic input capacitance
- Wide input bus
- Low R_{on} write switches

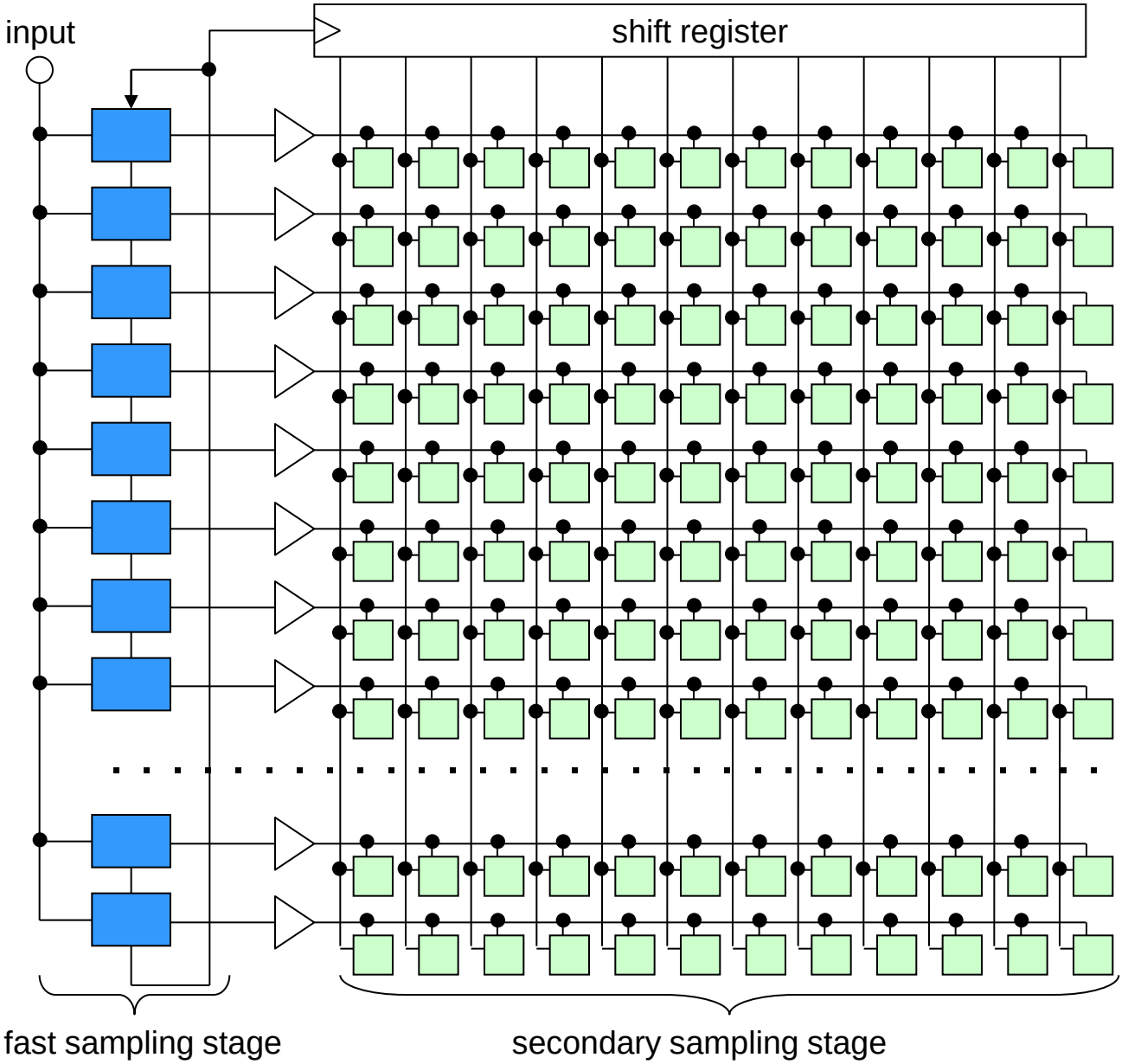
  → High bandwidth

How to combine best of both worlds?

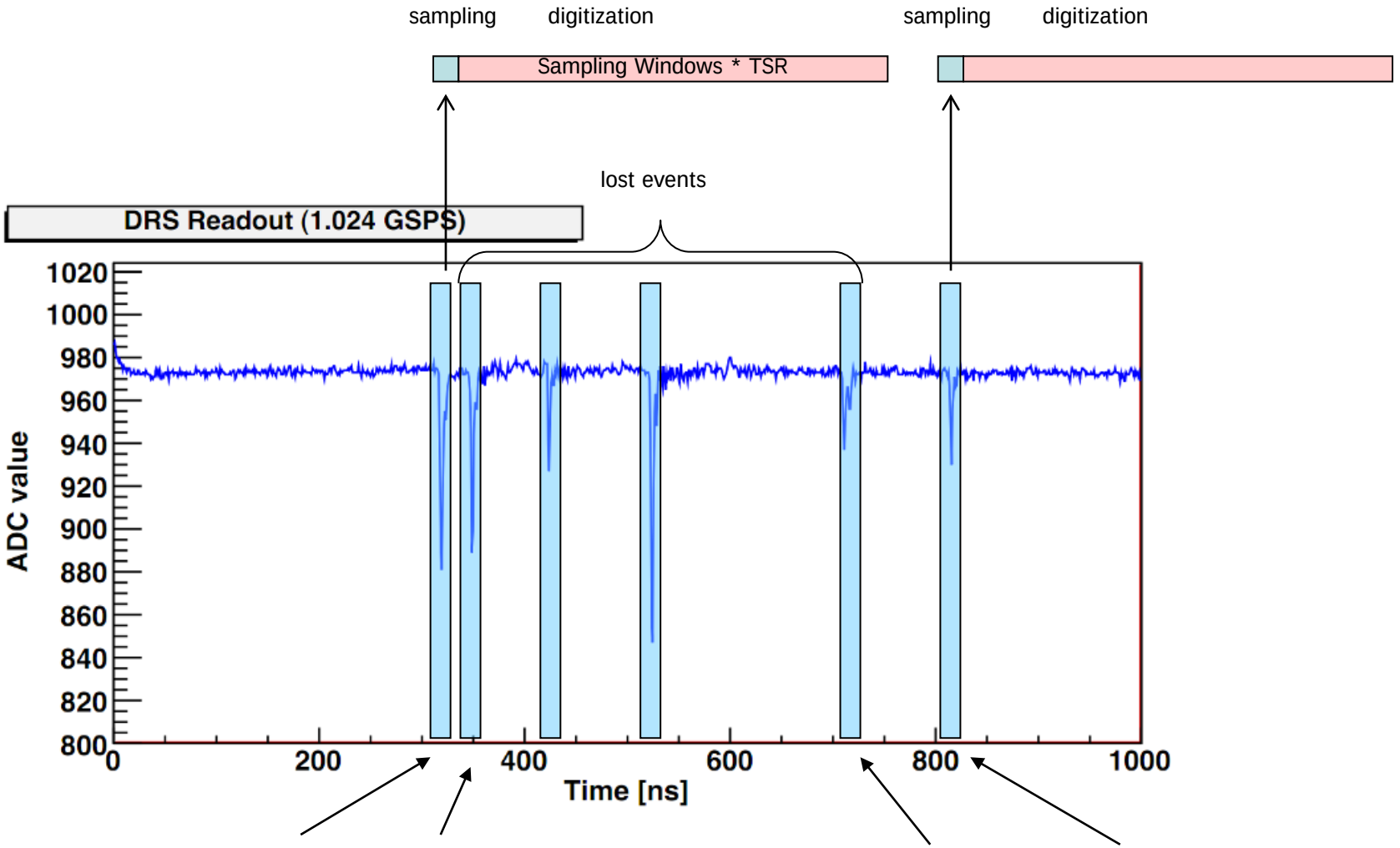
- Digitize long waveforms
- Accommodate long trigger delay
- Faster sampling speed for a given trigger latency

Cascaded Switched Capacitor Arrays

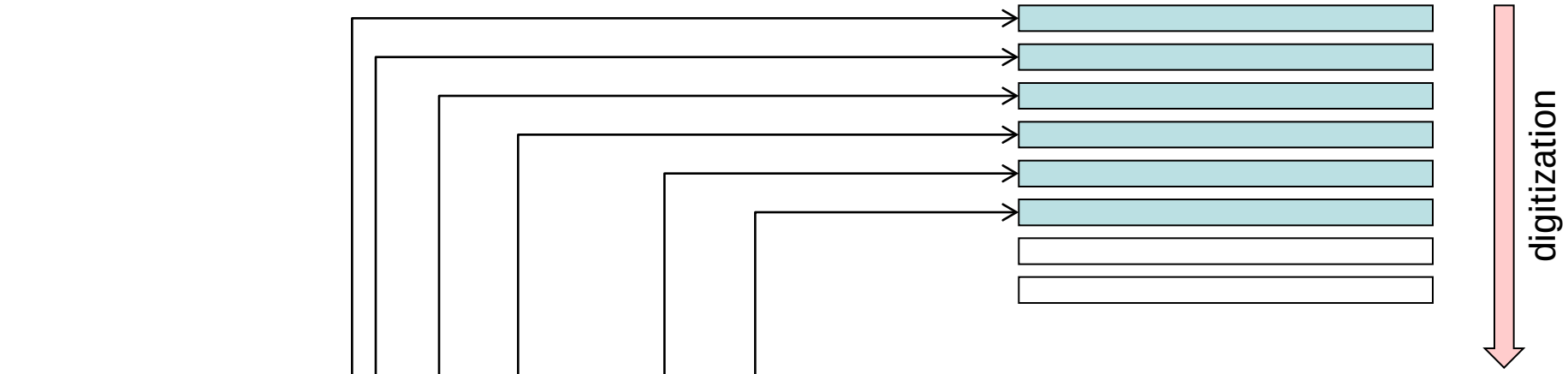
- 32 fast sampling cells (10 GSPS)
  → small capacitance, high bandwidth
- 100 ps sample time, 3.1 ns hold time
- Hold time long enough to transfer voltage to secondary sampling stage with moderately fast buffer (300 MHz)
- Shift register gets clocked by inverter chain from fast sampling stage

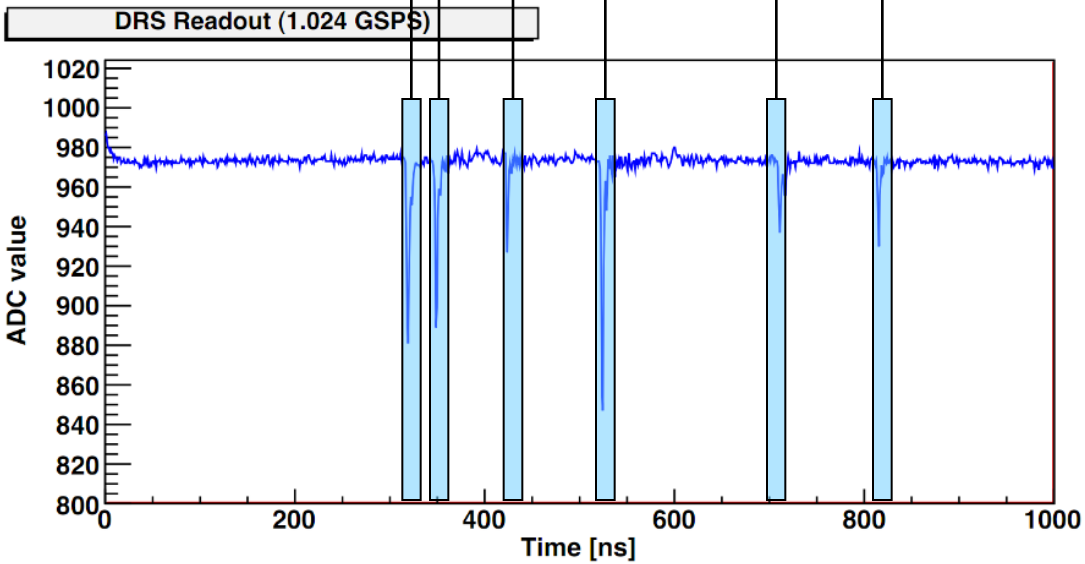


The dead-time problem



FIFO-type analog sampler





- FIFO sampler becomes immediately active after hit
- Samples are digitized asynchronously
- “De-randomization” of data
- Can work **dead-time less** up to average rate = 1/(window size * TSR)
- Example: 2 GSPS, 10 ns window size, TSR = 60 → rate up to **1.6 MHz**

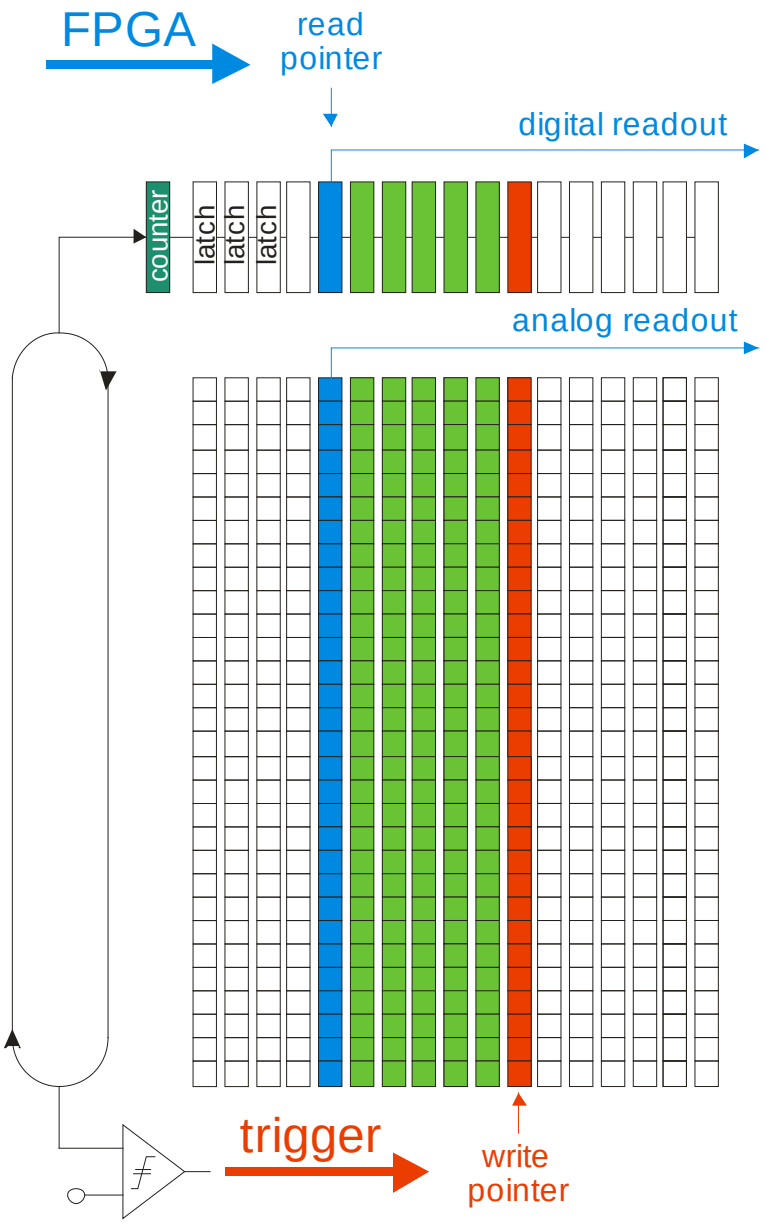
Plans

DRS5 (PSI)

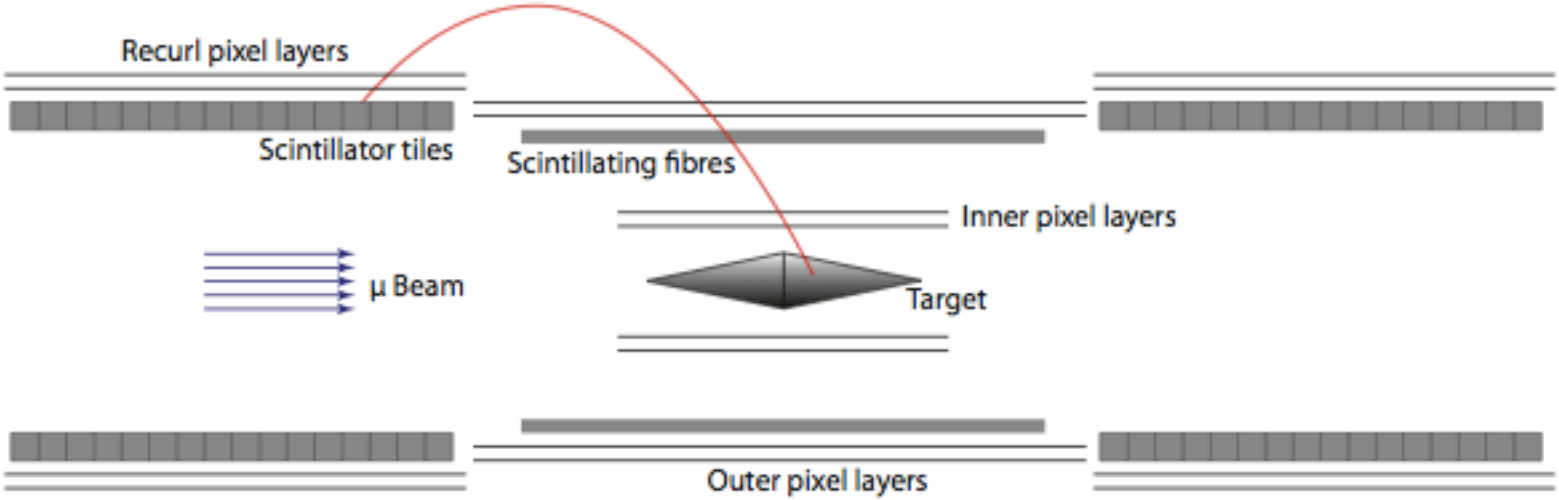
- Self-trigger writing of 128 short 32-bin segments (4096 bins total)
- Storage of 128 events
  - Accommodate long trigger latencies
  - Quasi dead time-free up to a few MHz,
  - Possibility to skip segments
    → second level trigger
- Attractive replacement for CFG+TDC
- First version planned for 2014

CEA/Saclay

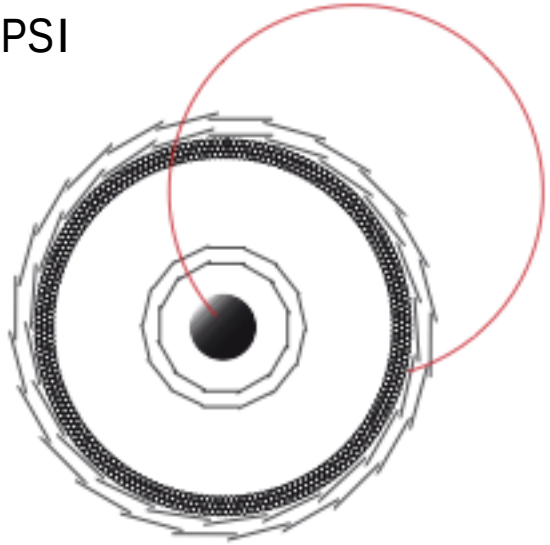
- Dual gain channels
- Dynamic power management (Read/Write parts)
- Region-of-interest readout



$\mu^+ \rightarrow e^+e^-e^+$



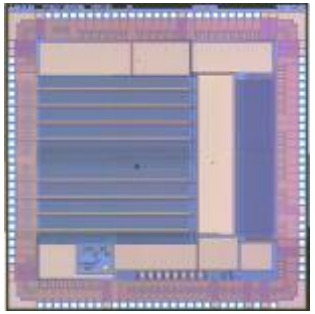
- Mu3e experiment planned at PSI with a sensitivity of 10^{-16}
- $2*10^9$ μ stops/sec
- Scintillating fibres & tiles
  - 100ps timing resolution
  - 2-3 MHz hit rate
- Can only be done with DRS5!

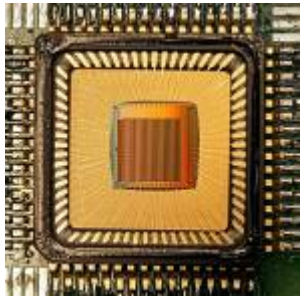


DRS4 Usage

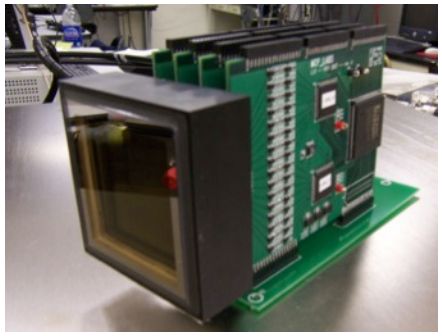
http://drs.web.psi.ch

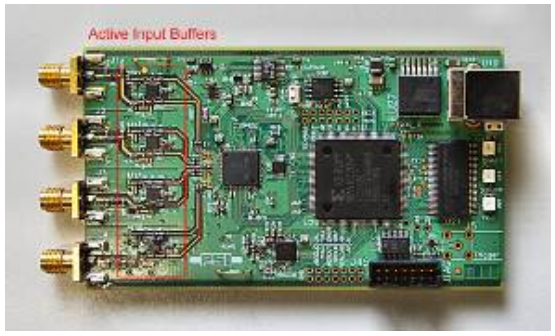
Conclusions

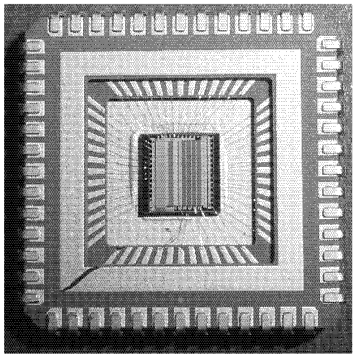




- SCA technology offers tremendous opportunities
- Several chips and boards are on the market for evaluation
- New series of chips on the horizon might change front-end electronics significantly

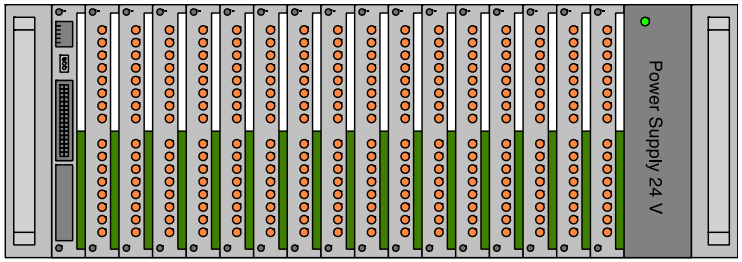


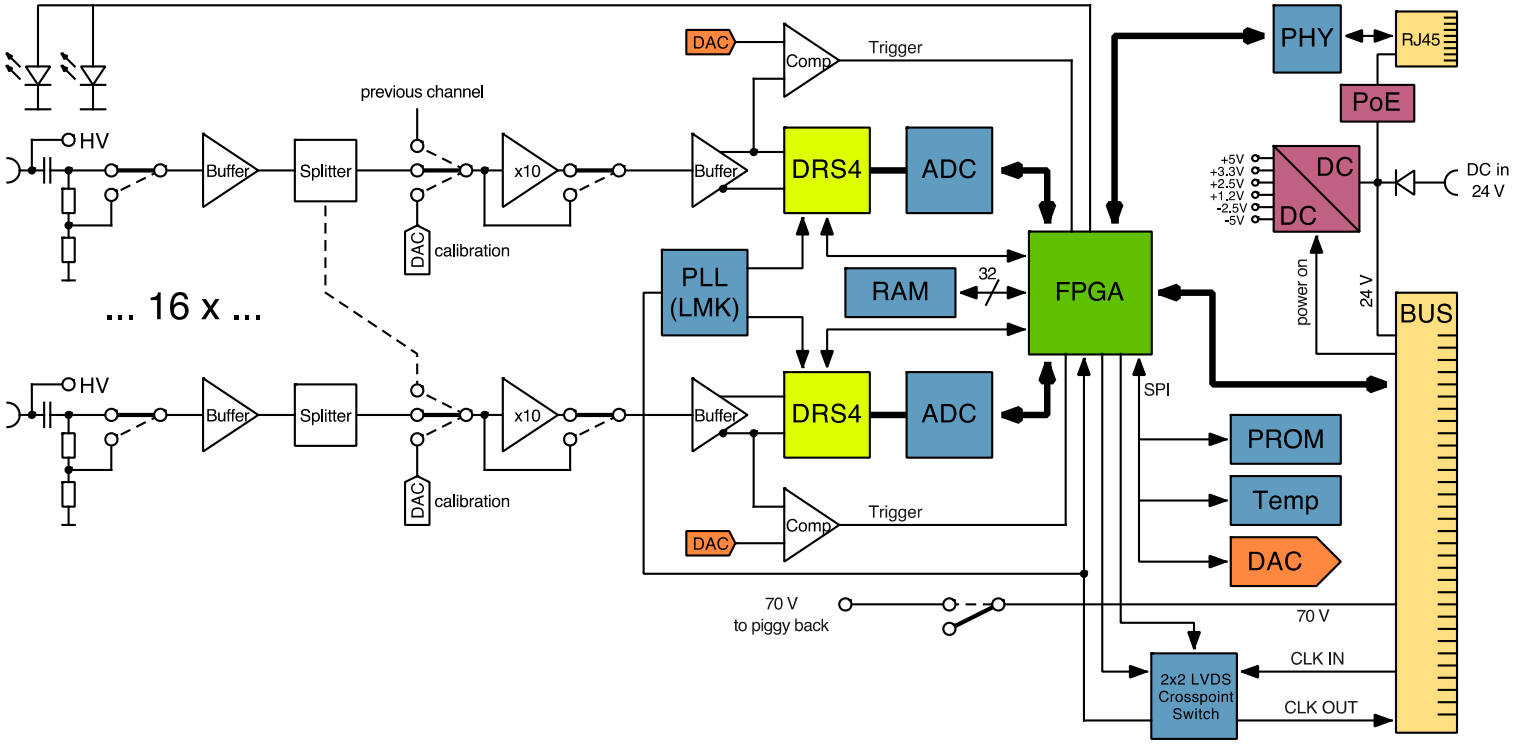




WaveDREAM board

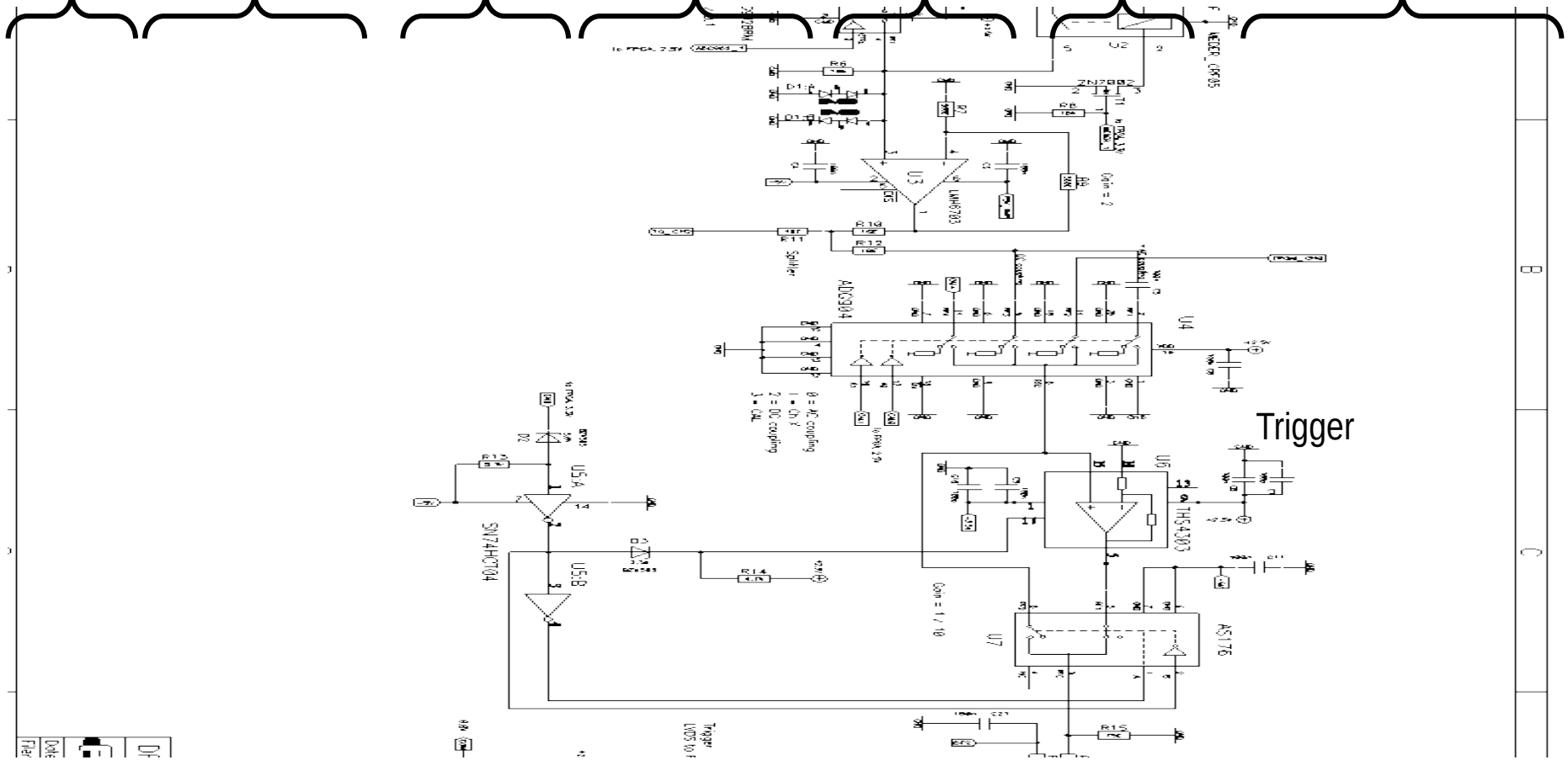
- 16 channels standalone (GBit Ethernet) or 3HE crate (256 channels)
- Variable gain 0.1/1/10 or 1/10/100
- Flexible integrated triggering
- Global clock synchronization
- Integrated SiPM biasing (up to 200V)
- Currently under development at PSI





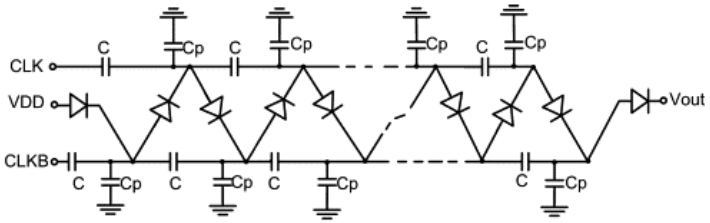
WaveDREAM analog front-end

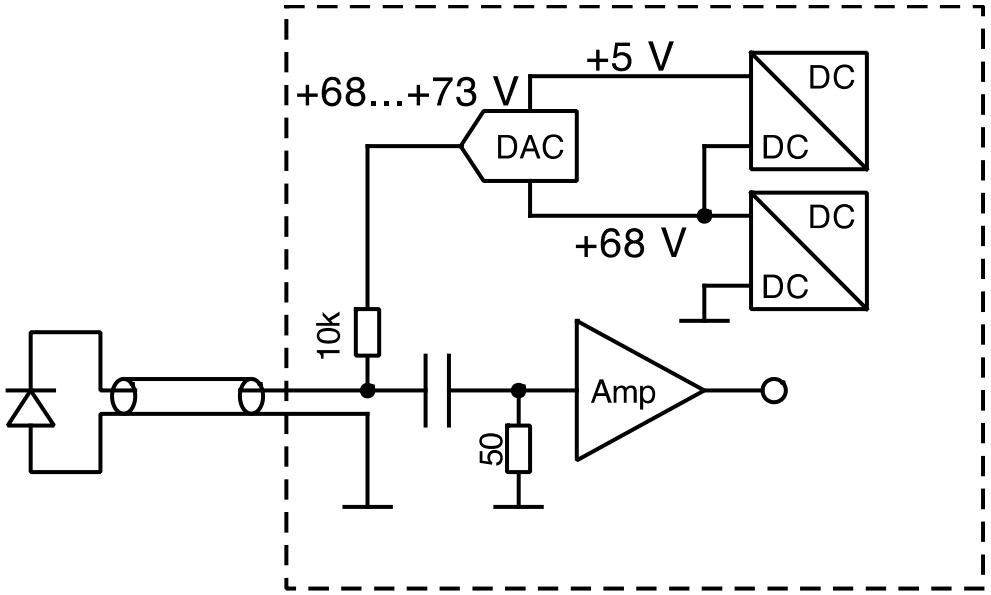
HV biasing | switchable Attenuator | Gain 2-10 | Coupling AC/DC/Calib | Gain 10 | Gain Selector | Differential Driver



SiPM High Voltage on WaveDREAM board

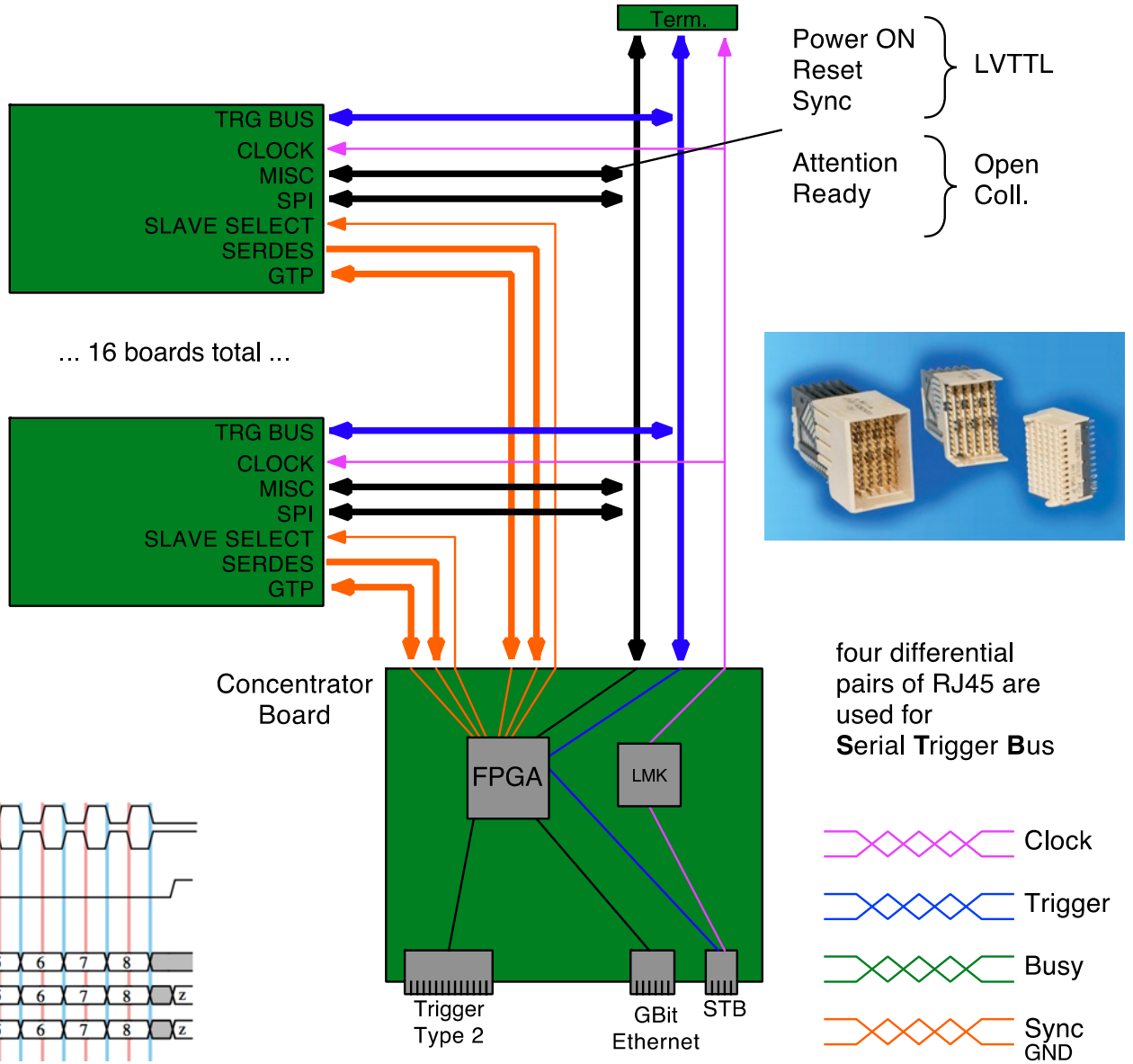
- Whole circuit works on virtual +68 V gound
- Connectors can stay on ground
- Regulation +68 V ... +73 V
- Current sense ~1 nA resolution
- ADC/DAC: ~8 EUR/channel
- Common DC-DC converter: +1 EUR / channel
  (Commercial or Cockroft-Walton)

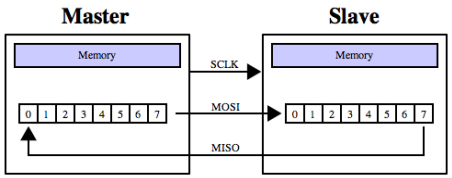


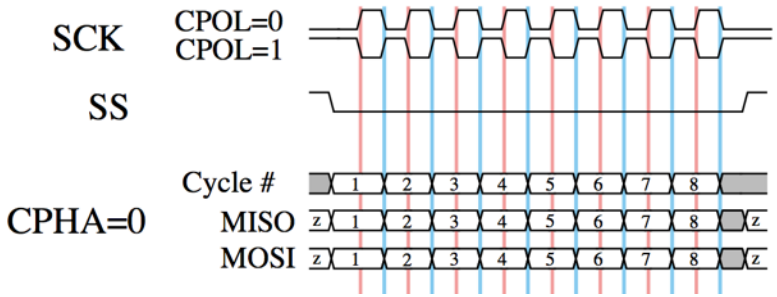


Crate backplane & Clock distribution

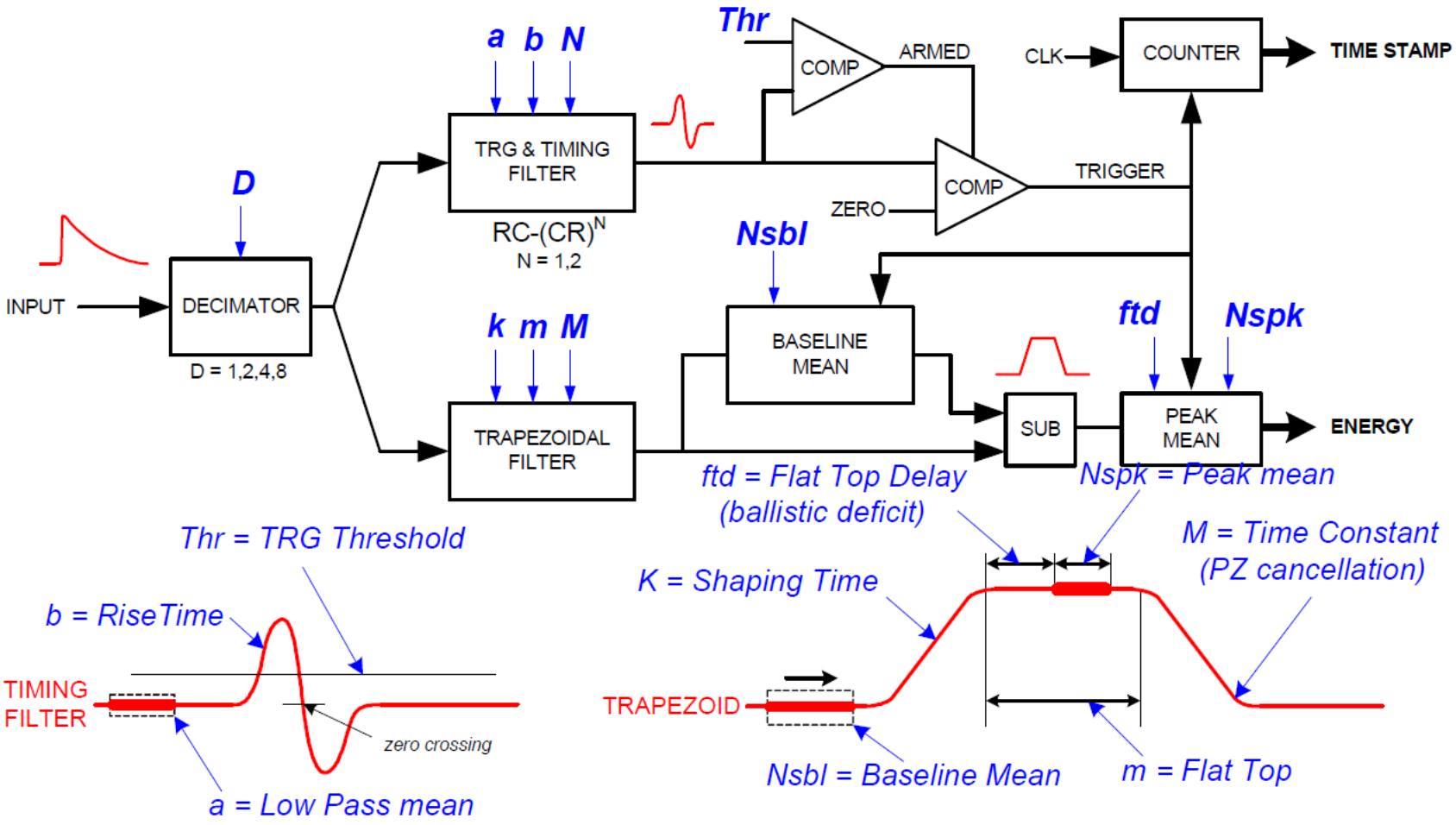
- Star connectivity for
  - GTP
  - SERDES
  - Slave Select
- Bus connectivity for
  - SPI (except SS)
  - MISC
  - Clock
  - Trigger







Digital Pulse Processing (DPP)

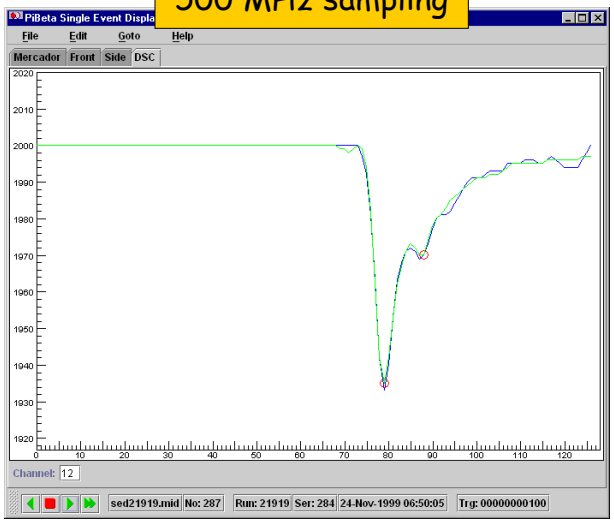


C. Tintori (CAEN)
V. Jordanov *et al.*, NIM **A353**, 261 (1994)

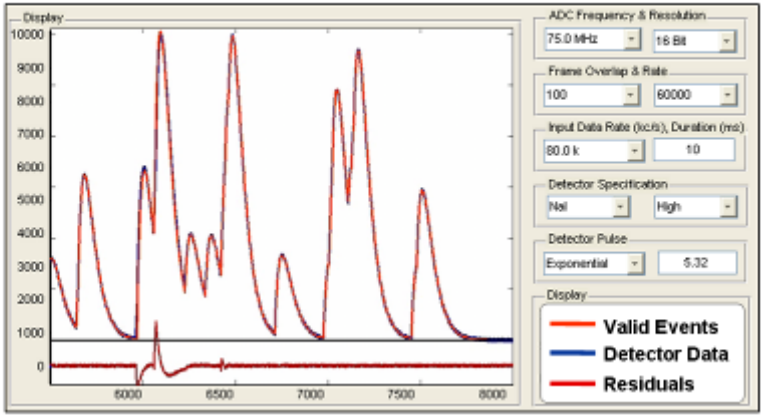
Template Fit

- Determine “standard” PMT pulse by averaging over many events → “Template”
  - Find hit in waveform
  - Shift (“TDC”) and scale (“ADC”) template to hit
  - Minimize χ^2
  - Compare fit with waveform
  - Repeat if above threshold
- Store ADC & TDC values

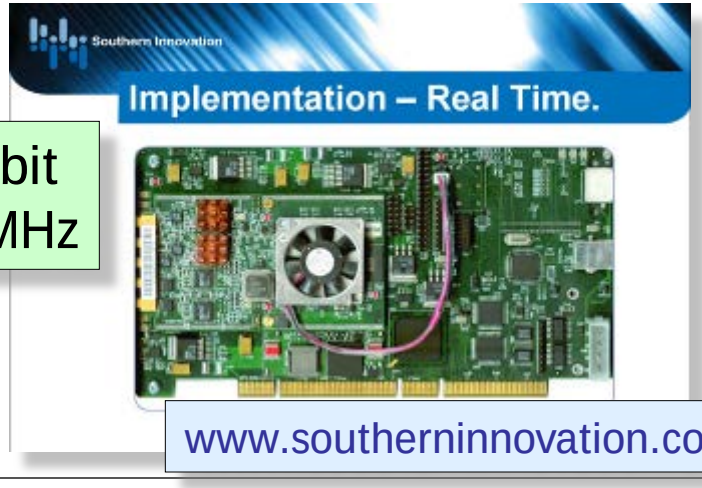
πβ Experiment
500 MHz sampling



- At 1,000 kc/s less than 10% of events cannot be decoded.



14 bit
60 MHz

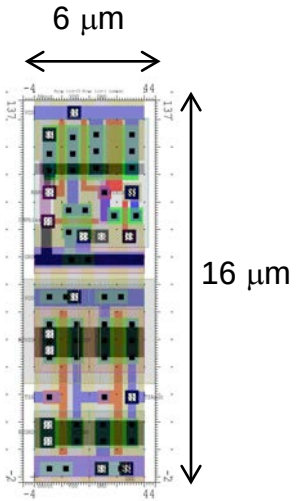


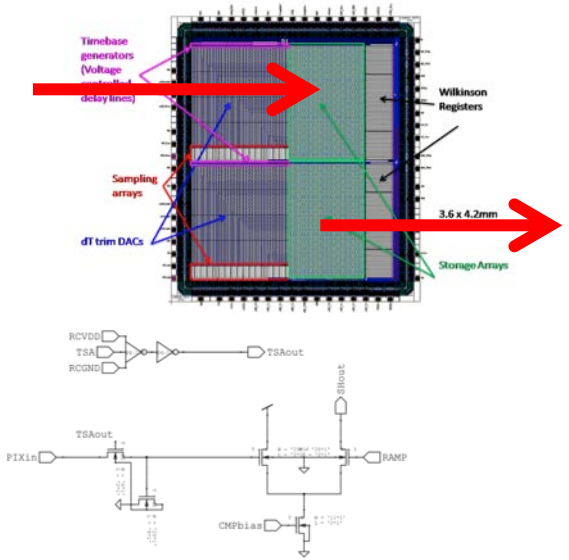
Some specialities

- LAB Chip Family (G. Varner)
  - Deep buffer (BLAB Chip: 64k)
  - Double buffer readout (LAB4)
  - Wilkinson ADC

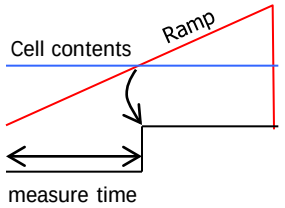
- NECTAR0 Chip (E. Delagnes)
  - Matrix layout (short inverter chain)
  - Input buffer (300-400 MHz)
  - Large storage cell (>12 bit SNR)
  - 20 MHz pipeline ADC on chip

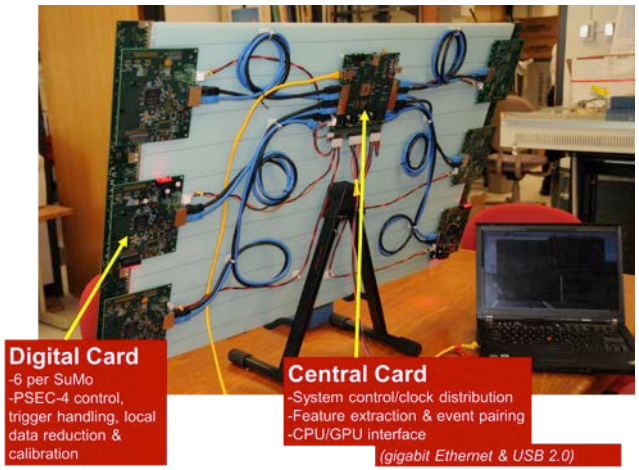
- PSEC4 Chip (E. Oberla, H. Grabas)
  - 15 GSPS
  - 1.6 GHz BW @ 256 cells
  - Wilkinson ADC





Wilkinson-ADC:





How to fix timing nonlinearity?

- LAB4 Chip (G. Varner) uses “Trim bits” to equalize inverter delays to < 10 ps
- Dual-buffer readout for decreased dead time
- Wilkinson ADCs on chip

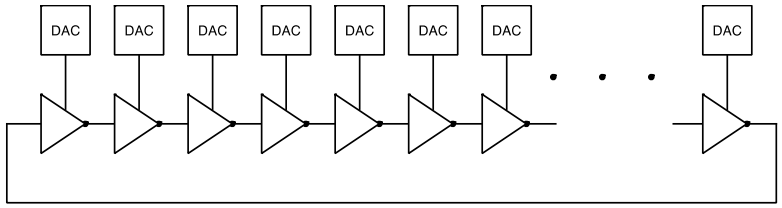
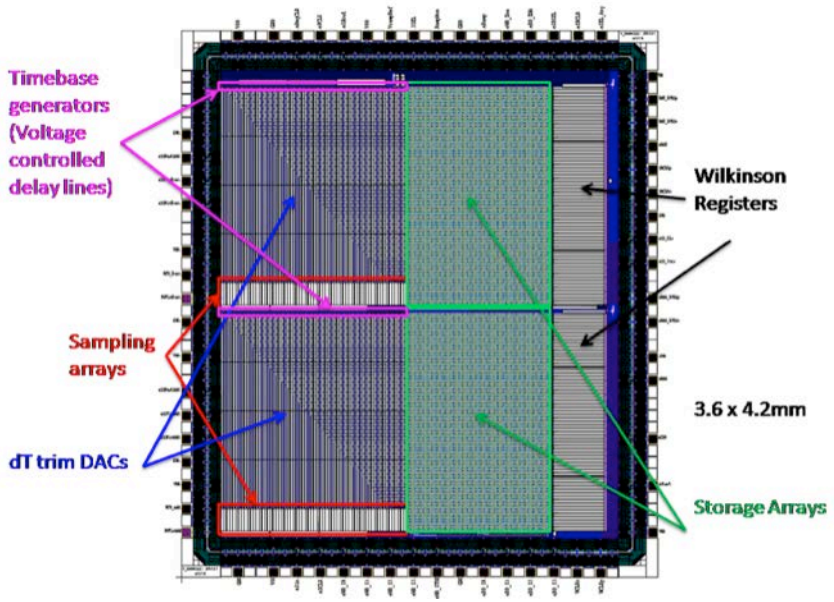


TABLE I
PERFORMANCE SPECIFICATIONS FOR THE LAB4 ASIC.

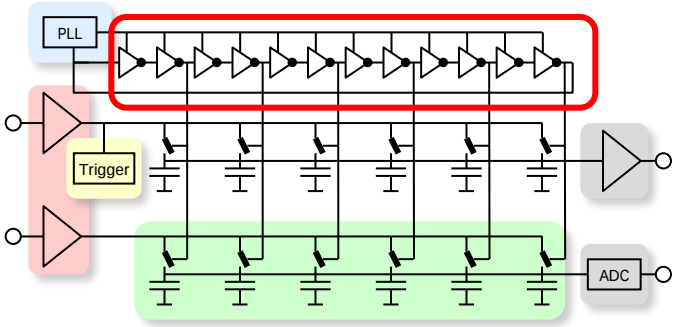
Specification	Parameter
4096	samples/channel
1	channel/ASIC
$\leq$ 10	ps residual timebase error
$\sim$ 10	bits resolution (12-bits ADC)
256	samples convert window ($\sim$64ns)
4	GSa/s sampling
$\leq$100	μs to read all samples
$\geq$1k	Hz sustained readout (multibuffer)

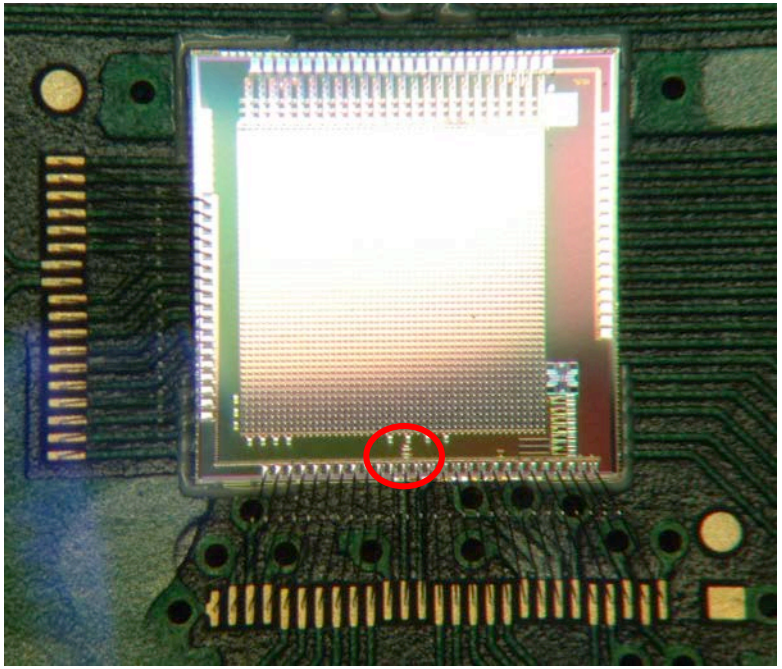


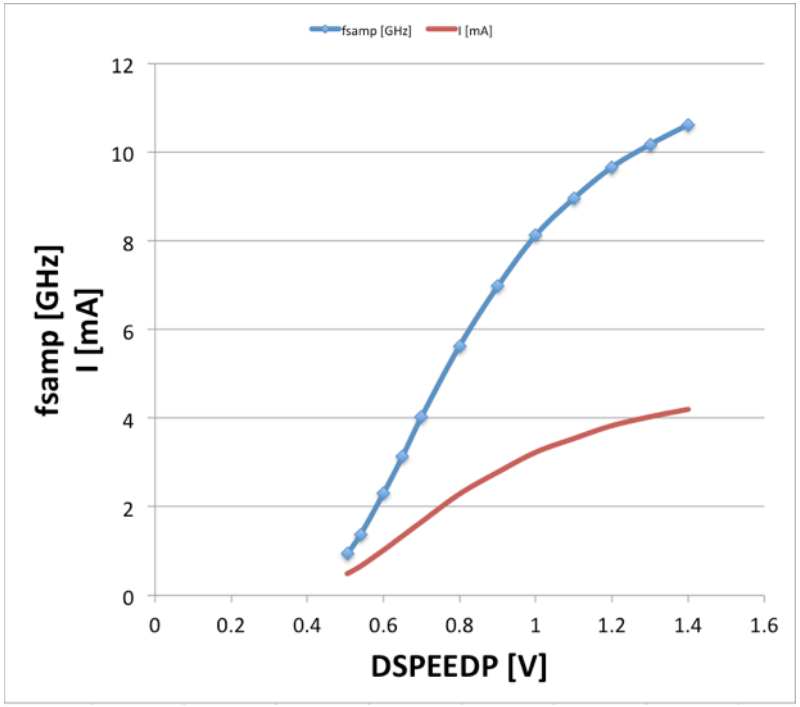
First tests will be reported on RT12 conference June 11-15, Berkeley, CA

DRS5-T1

- First silicon in 110 nm technology
- Implemented just inverter chain with 32 cells
- 4 mA @ 10 GSPS at 1.4 V







New MicroFM Detectors

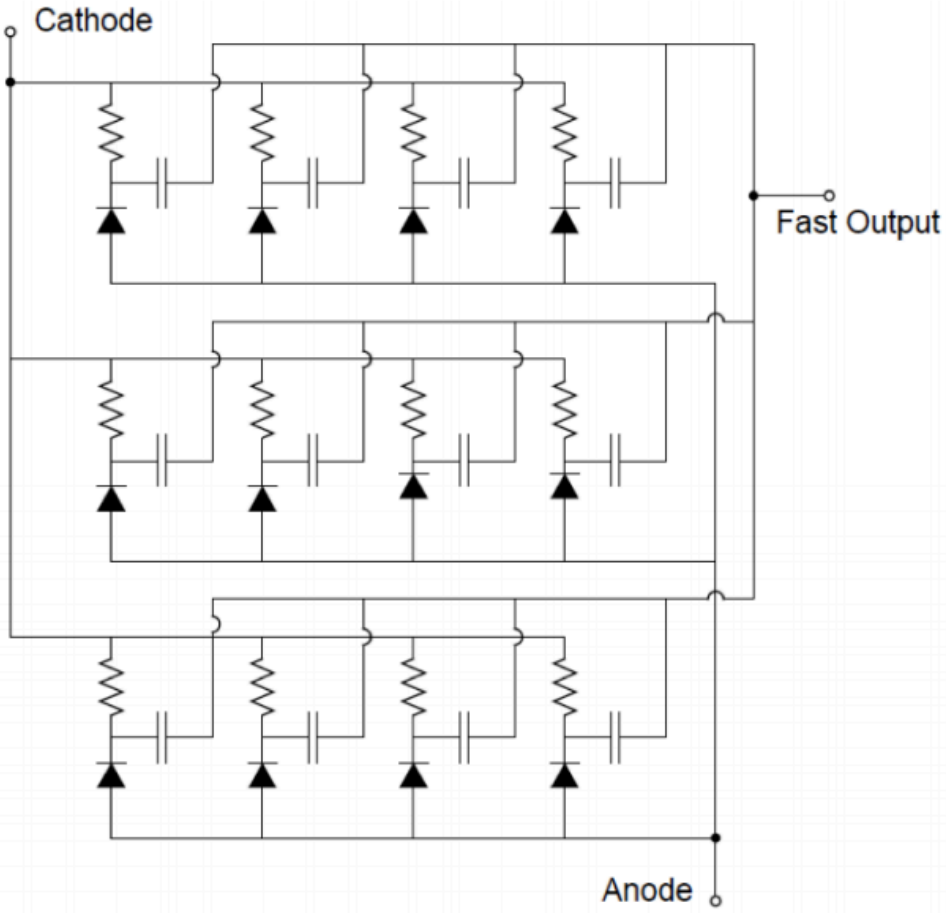


Figure 1, Schematic of the fast output structure

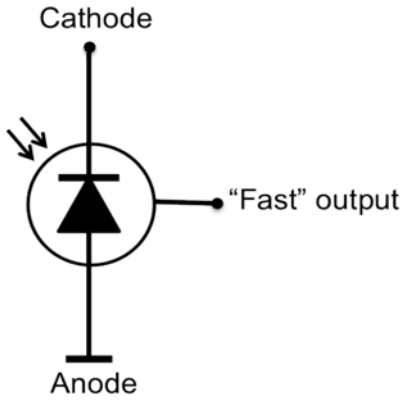


Figure 2, Configuration for fast mode

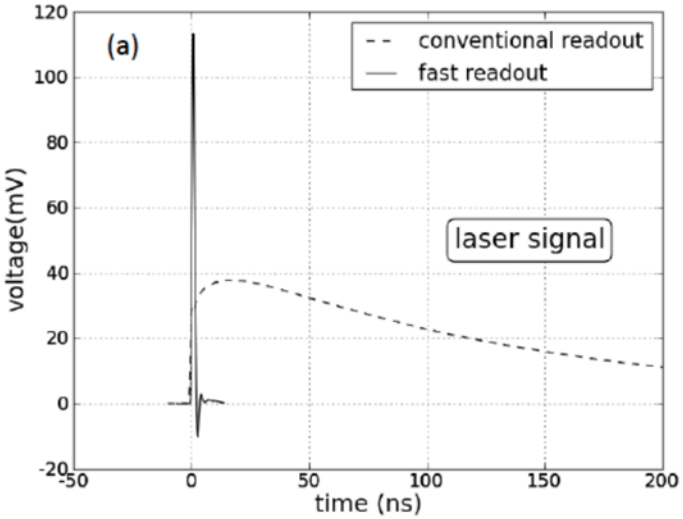
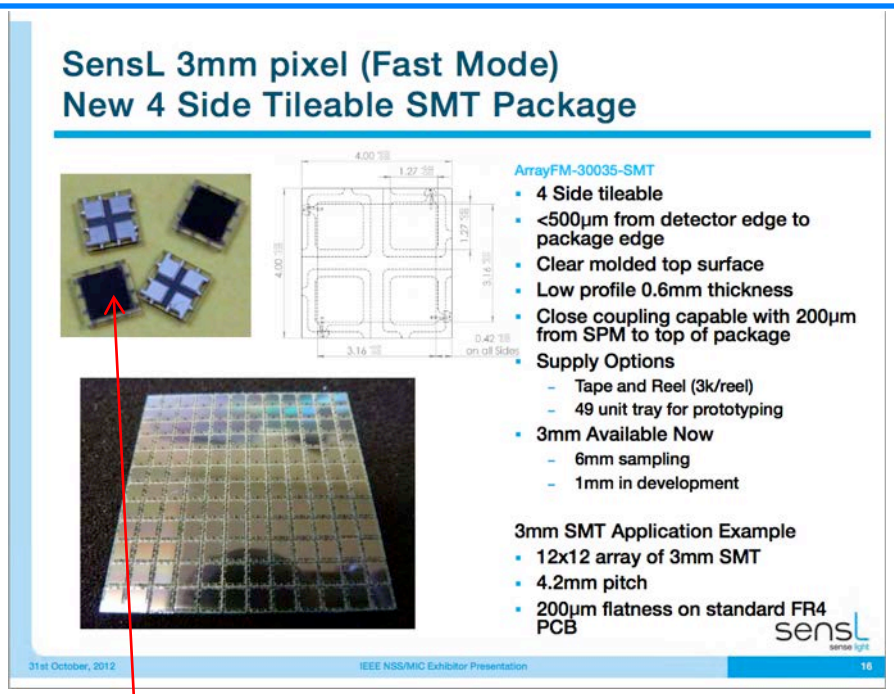
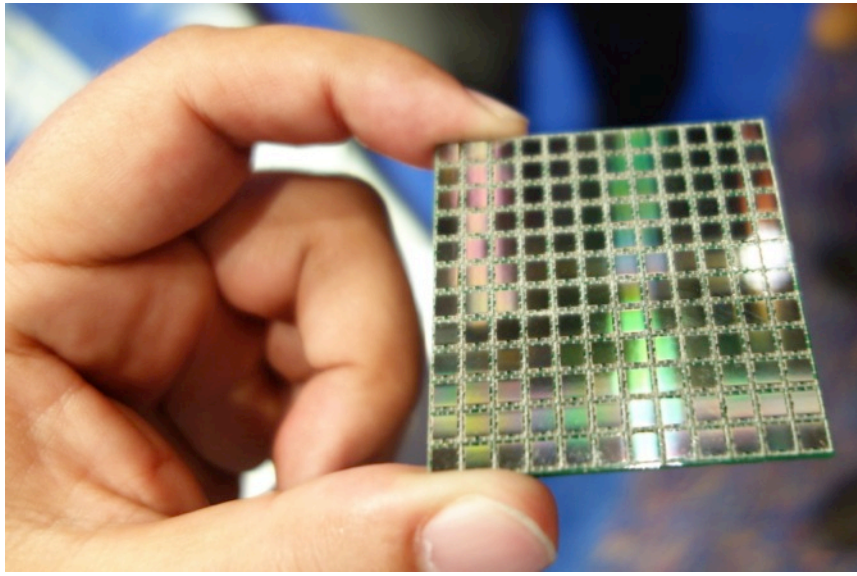


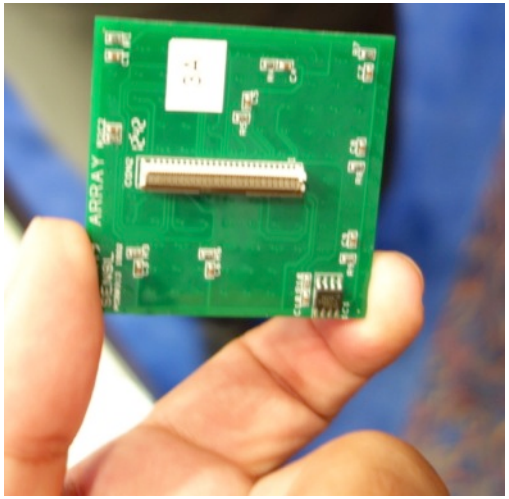
Figure 4, Signals from both modes when illuminated with a 50ps laser pulse.

Rise-time <100 ps possible

New SMD package







3x3 mm SiMP: 18 US$ for >100pc (unverified)

DRS4 documentation

PAUL SCHERRER INSTITUT

9 Channel, 5 GSPS Switched Capacitor Array

DRS4

FEATURES

Single 2.5 V power supply
Sampling speed 700 MSPS to 5 GSPS
8+1 channels with 1024 storage cells each
Cascading of channels or chips allows deeper sampling depth
Differential inputs with 950 MHz bandwidth
Differential outputs for direct ADC interfacing
Transparent mode for integrated triggering
Readout time: 30 ns * number of samples
Simultaneous reading and writing
Multiplexed or parallel analog outputs
Low power: 140 mW typical at 2 GSPS (17.5 mW per channel)
Low integral nonlinearity: 0.5×10^{-3} at 1 V range
High SNR: 69 dB after offset correction
Low Noise: 0.35 mV after offset correction

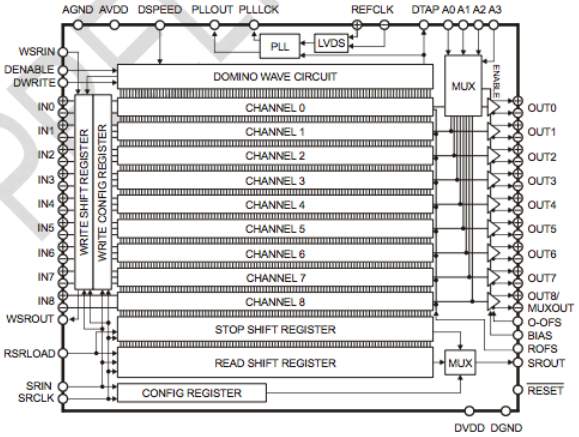
APPLICATIONS

Instrumentation and Measurement
Photomultiplier, Drift Chamber and APD Readout
Low Cost Digital Oscilloscopes
Ultrasound Equipment

GENERAL DESCRIPTION

The Domino Ring Sampler (DRS) is a switched capacitor array (SCA) capable of sampling 9 differential input channels at a sampling speed of 700 MSPS to 5 GSPS (6 GSPS for selected chips). The analog waveform is stored in 1024 sampling cells per channel, and can be read out after sampling via a shift register clocked at 33 MHz for external digitization.
The write signal for the sampling cells is generated by a chain of inverters (domino principle) generated on the chip and stabilized by a PLL. The domino wave is running continuously until stopped by a trigger. A read shift register clocks the contents of the sampling cells either to a multiplexed or to individual outputs, where it can be digitized with an external ADC. It is possible to read out only a part of the waveform to reduce the digitization time.
The high channel density, high analog bandwidth of 950 MHz, and low noise of 0.35 mV (after offset calibration) makes this chip ideally suited for low power, high speed, high precision waveform digitizing. Fabricated on an advanced CMOS process in a radiation hard design, the DRS4 is available in a 76-pin quad flat non-leaded package (QFN).

FUNCTIONAL BLOCK DIAGRAM



REV. 0.9 **Please check for updates at http://drs.web.psi.ch/datasheets**

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DRS4 Evaluation Board User's Manual

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Board Revision 4.0
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Please check for possible updates of this manual under http://drs.web.psi.ch/datasheets