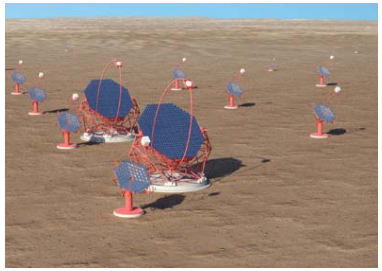
High precision clock distribution in modern astroparticle experiments - White Rabbit

Ralf Wischnewski (DESY) * **

HAP Detector-Technology Workshop
KIT Karlsruhe, 24.1.2013



* Helmholtz Russia Joint Research Group HRJRG-303
(„Measurements of Gamma-Rays and Charged Cosmic Rays in the Tunka-Valley by innovative technologies“)
** In collaboration with Martin Brückner (HU-Berlin)

DESY

Outline

- Time Synchronization in large AP experiments
  - Upcoming projects with nsec-requirements: can proprietary solutions be avoided ?
- White Rabbit (WR) - a new sub-nsec time transfer standard
  - The principles; Open Hardware/Software; the community
- HiSCORE - WR in a first astroparticle project
  - Installed 10/2012 @Tunka: initial results from laboratory & field
- Discussion - Need your own nsec-synchronization ?
  - Example: triggering - a simple case
- Conclusion - Sub-nsec timing over ethernet is working.

DESY

Time Synchronization in large AP-Experiments

> nsec-scale time synchronization in distributed DAQ-Systems is a typical challenge for large AP-experiments

- Large Volume / Surface / Distance detectors: typical: >>km-size;
  NeutrinoTel, CR-, Radio-, Gamma-telescope arrays; LBL-exp Opera !
- Important : Timing determines data quality;
- Difficult : requires extensive verification / calibration / monitoring
- So far : only custom-solutions were developed.
  Antares, Baikal, IceCube, Kascade,Tunka,…, Lopes, Lofar,…
  (Auger: GPS, but>>10ns)

> For next generation projects :
> Is there a “standard technique” ?

- “Out-off-the-box”, commercial, long-term supported, …. -
  rather than re-inventing the wheel over and over again ?!
- CTA, HiSCORE, km3Net, LHAASO (AugerNext) will significantly profit

Time Synchronization : The Task

> Time Synchronization of all basic units

- Detectors (stations, cameras,…) generate a "**local trigger** signal" , that is time-stamped ; AND/OR
- Detectors have local clocks that time-stamp the **data permanently** .

> For a timing-system: Two jobs need to be done

(1) **Build the time distribution system**

Synchronize clocks in all detector units to a common central clock with nsec precision; with optionally better phase alignment

Aim: relative timing between detector units must be correct at any moment (not the absolute time)

(2) **Verify the time distribution system**

Long-term monitor / control in-situ, for at least a subset of the installed array.

Verification by an *independent* system is as important as the synchronization; and a comparable technical challenge .

> The complex verification is a main argument to establish a "standard" for the community.

> Note: Any precision timing system can also be used as precision time-calibration source !

White Rabbit - What is it ?

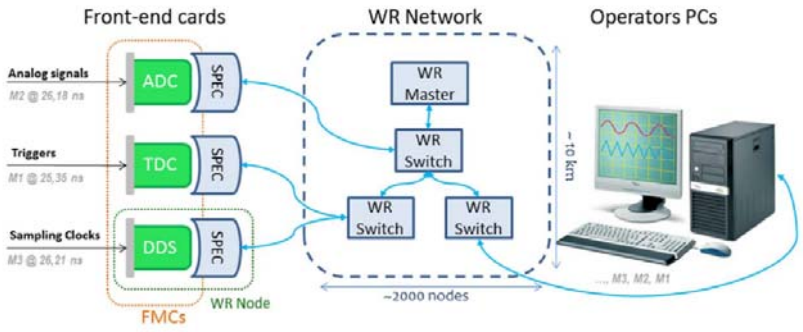
A new CERN-based extension to Ethernet for precision time and frequency transport;

Based on

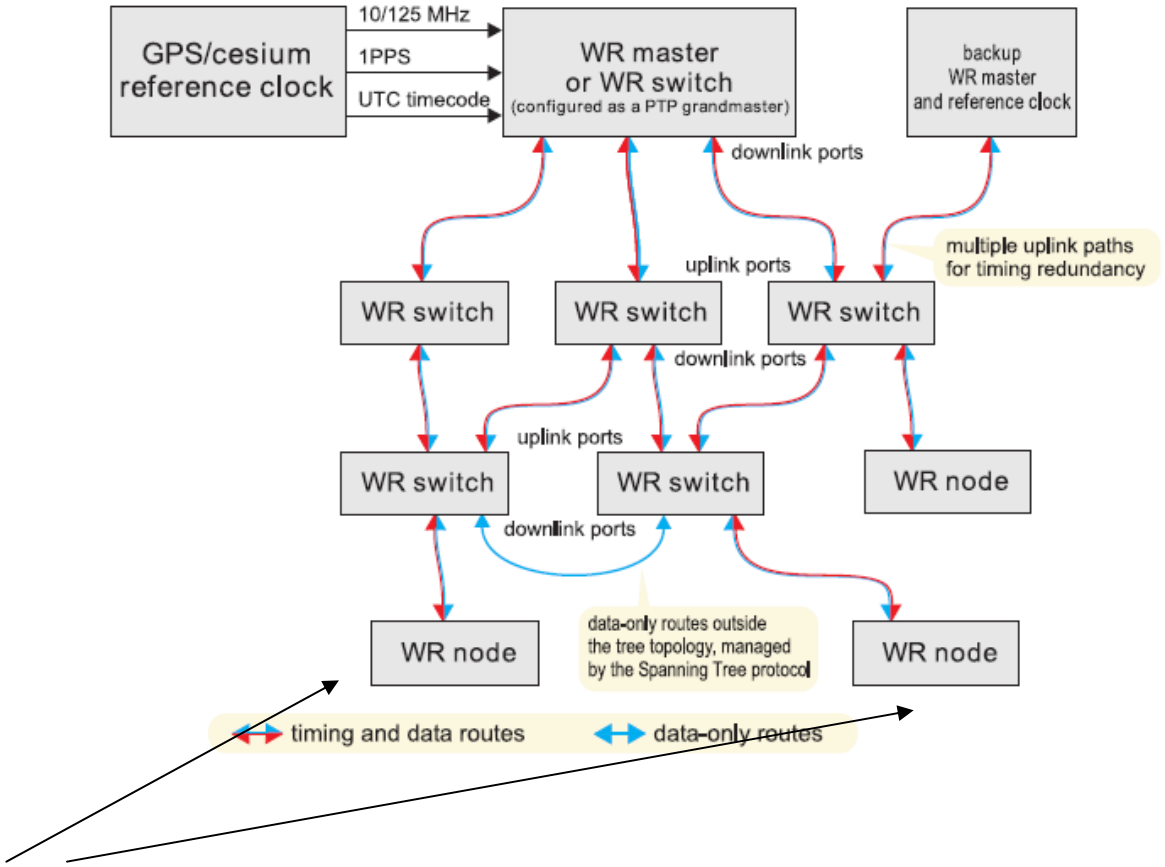
- Synchronous mode (clock synchronization)
- Deterministic routing (package latency guaranteed)

Performance :

- ~1 ns precision, 20 ps jitter
- ~ 10 km fiber links
- up to 2000 nodes



White Rabbit - Network topology



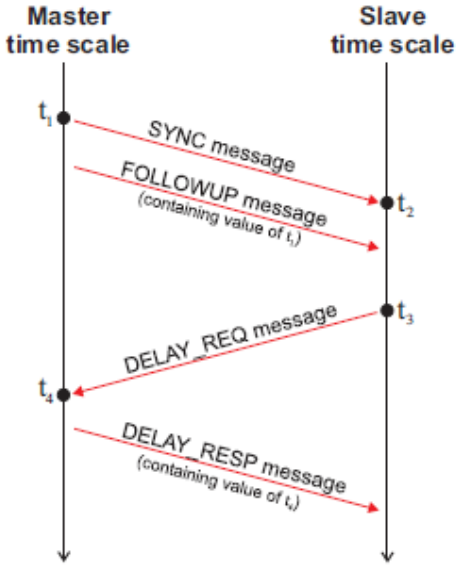
- **WR-Node = User modules with local clocks**
- **WR-Nodes are synchronized over the WR-network to the Master-switch (WRS).**
- **Master-WRS is connected to a reference clock (GPS/Caesium).**

White Rabbit - How does it work ?

> Sub-nsec synchronization reached by 3 ingredients

1. PrecisionTime Protocol (PTP), IEEE1588

   local clock synchronization by
   measuring and compensating
   the master-slave link delay
   (w/ hardware supported timestamps).



2. Synchronous Ethernet

   slave frequency locking; propagating over network

3. DMTD phase tracking

   digital slave phase-offset adjustment (w/ ps-jitter)

DESY

White Rabbit - Why give it a try ?

WR is

- Supported by an active core-team @CERN,
- Planned for the LHC accelerator upgrade
- Growing participation from industry.

First astroparticle applications (“reference”) are underway now.
See below: HiSCORE / CTA. Initial results are extremely encouraging.

<u>Advantages :</u>

> Development for CERN & GSI accelerator complex; much external interest

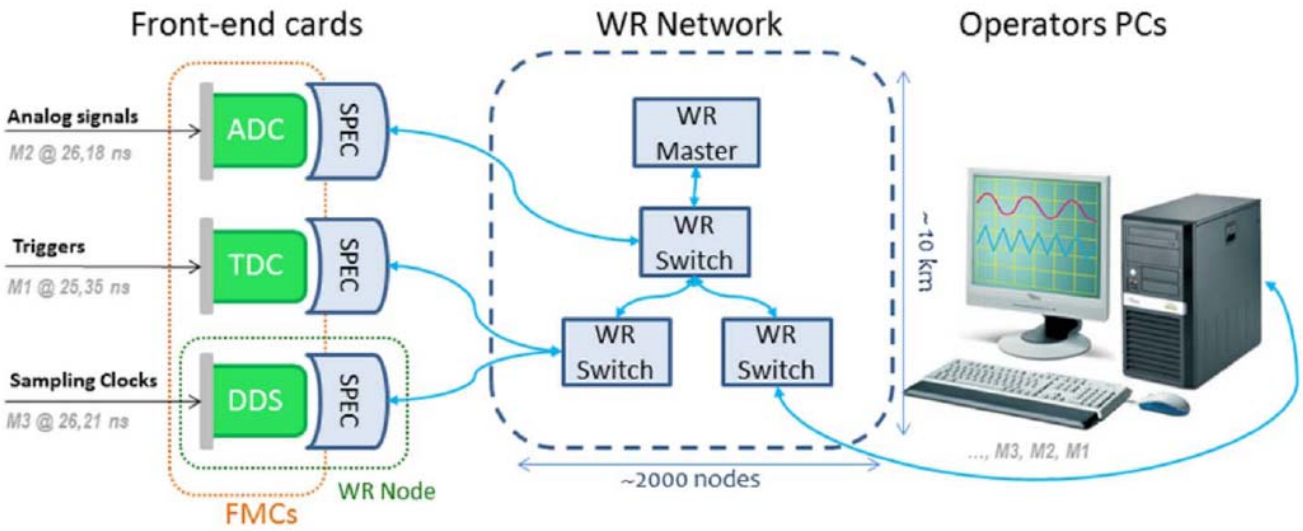
> Open Hardware & SW Project; peer reviewed; fully transparent to the user. Adapting to a use-case is easy and supported.

> Hardware is commercially available (growing #companies),

> Standardization planned (IEEE…)

> A guaranteed large user community: it will be a well debugged system… !!

White Rabbit



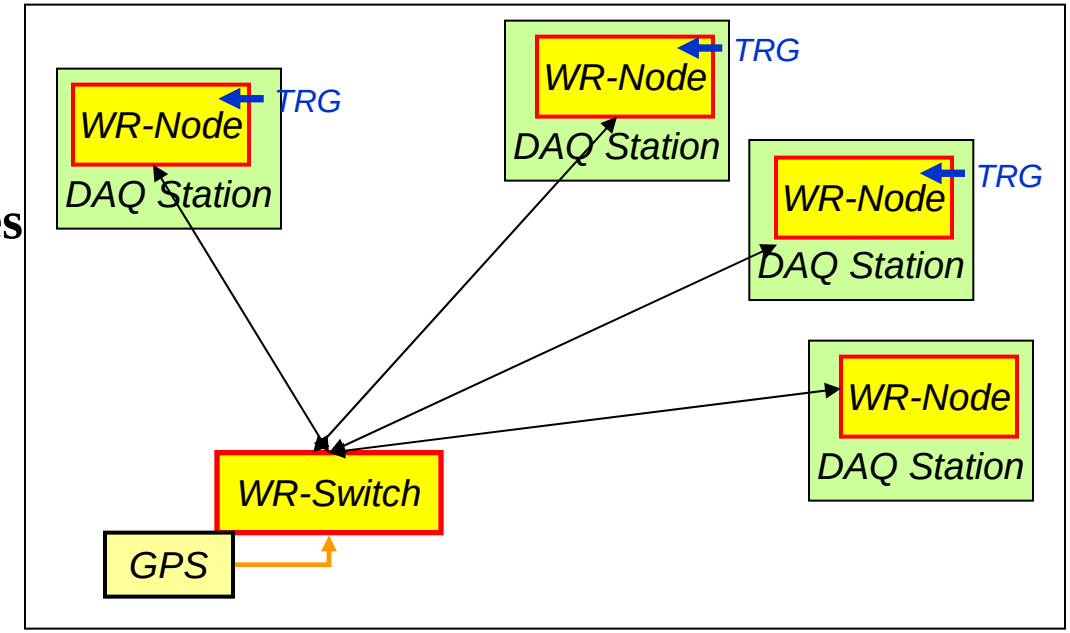
- **See eg: Cern-WR-site http://www.ohwr.org/projects/white-rabbit/wiki and http://znwiki3.ifh.de/TUNKA/**

Basic Layout of a WhiteRabbit based timing DAQ

White Rabbit DAQ architecture:

(1) WR-network
= WRSwitches + GPS/RbCl
to distribute the clock to Nodes

(2) WR-Nodes ('endpoints')
for time-stamping, …



Components

- **WhiteRabbit Switches (WRS)**
- **White-Rabbit Nodes**
  eg. SPEC (*S*imple *P*CI*e* FMC *C*arrier)
  (or build your own board: OWHR)

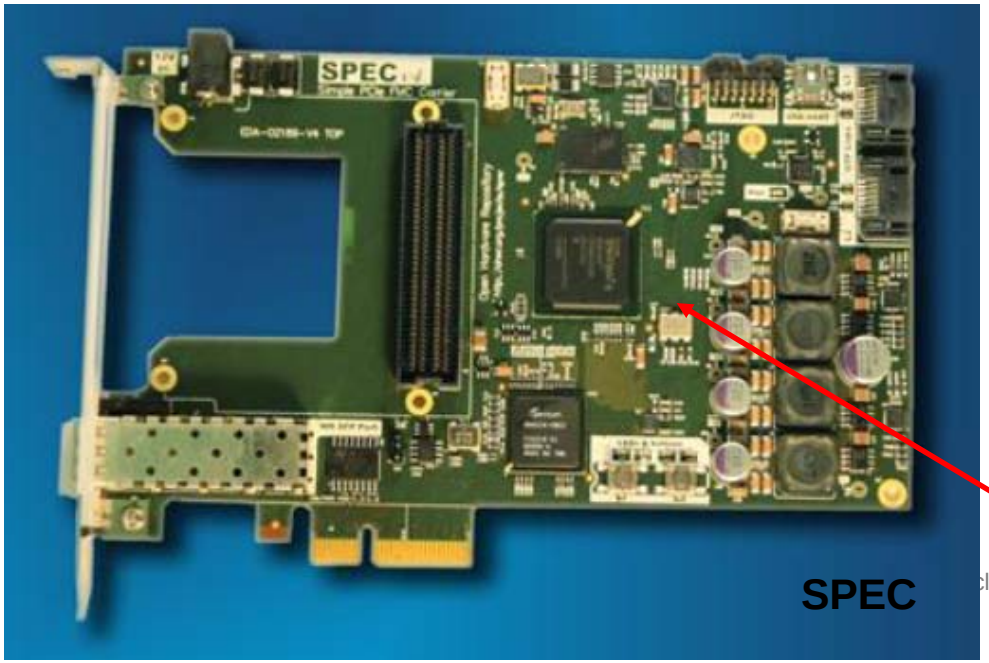
since July/2012

since 2011

The WR Node : SPEC Card

-SPEC ("Simple PCIe FMC Carrier") is the WR node currently available.
(A VME carrier is in production: "SVEC")

- For tests, it can also be configured as WR-Master (used for April/2012 tests).
- It carries the mezzanine-card for your DAQ:
available/planned
  - Digital InpOutFMC / FMC DEL / FMC FADC(100MHz) / TDC;
  - eg. possible: design a DRS4-based mezzanine for HiSCORE/CTA



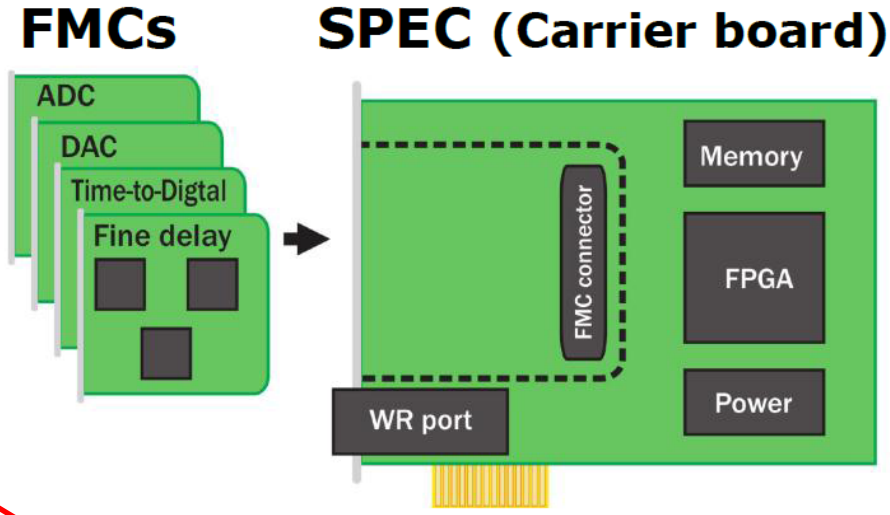


Illustration of the connection of SPEC with FMCs

WR-Clock: 125MHZ, psec-phase

FMC-DIO-5CHTTLA FMC 5-CHANNEL DIGITAL I/O MODULE

The *fmc-dio-5chttla* 5-channel digital I/O module is a simple board for digital I/O on LEMO connectors.
It has been designed for testing White Rabbit functionality as part of the SPEC Demonstration Package for White Rabbit (**manual**), and it can be used for other applications too.

The simplest SPEC-FMC available.

5 x I/O connectors, freely configurable by the SPEC_FPGA.

Used eg. as

- Output: 1-PPS-OUT, Test-Pulse

- Input: TriggerTimeStamping (for FPGA_TDC)

FUNCTIONAL SPECIFICATIONS

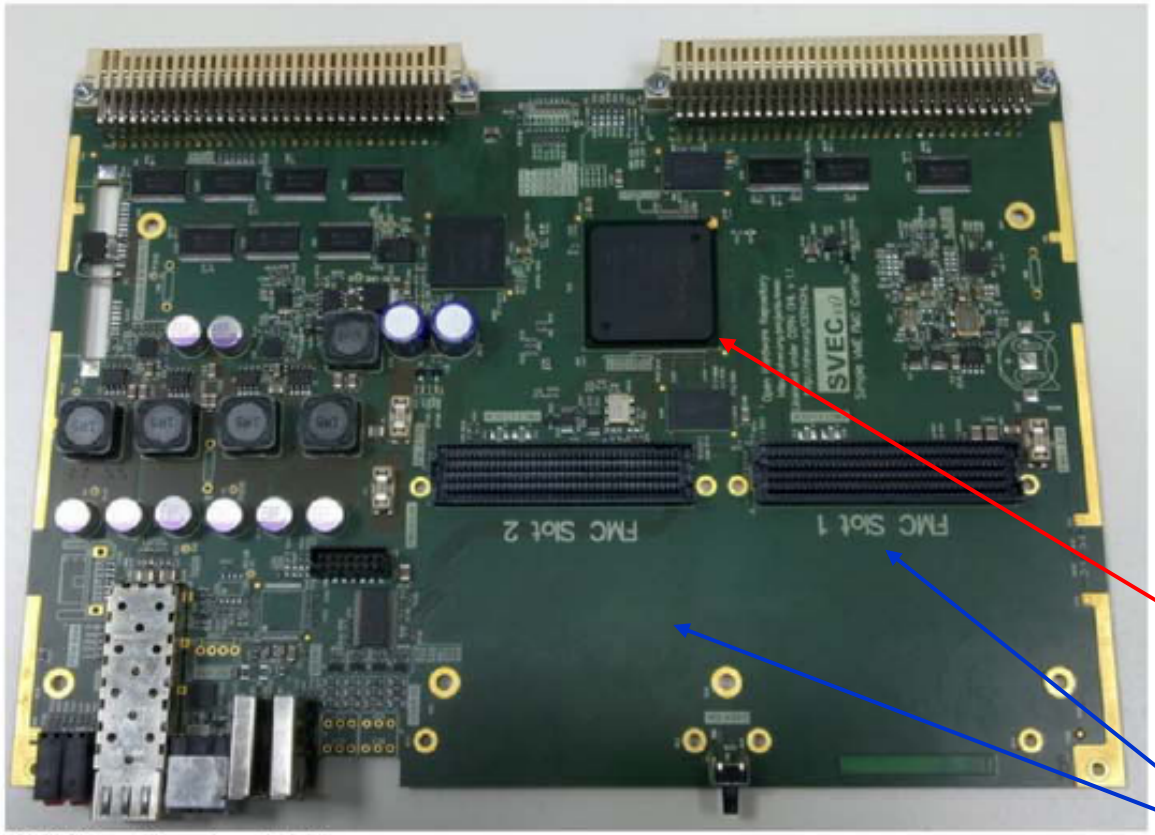
- 5 input/output ports (Lemo 00 connectors)
- Output levels: LVTTL, capable of driving +3.3 V over a 50-Ohm load. At power-up the outputs should be in Hi-Z state
- Input levels: any logic standard from Vih = 1 V to Vih = 5 V (programmable threshold)
- Output Rise/fall times: max. 2 ns
- Input bandwidth: min. 200 MHz
- Programmable 50-Ohm input termination in each channel
- LVDS I/O on the carrier side
- One of the inputs shall be capable of driving a global clock net in the carrier's FPGA
- Inputs need to be protected against +15V pulses with a pulse width of at least 10us @ 50Hz (with protection diodes if possible)
- Withstands a continuous short-circuit on all the outputs at the same time

Simple VME FMC Carrier (SVEC)

Project description

The FMC VME Carrier is an FMC carrier that can hold two FMC cards and an SFP connector. The FMC mezzanine slots use low-pin count (LPC) connectors This board is optimised for cost and will be usable with most of the FMC cards designed within the OHR project (e.g. ADC cards, Fine Delay). For boards needing more possibilities (e.g. programmable clock resources, fast SRAM, fast interconnect between carriers), the **VME FMC Carrier - VFC** can be used.

Other FMC projects and the FMC standard are described in **FMC Projects**.



SVEC V0 prototype board photo

VME-Carrier for 2 FMCs.
For CERN (BeamLine?) in production now.
Soon available commercially.

WR-Clock

2 x FMCs

Main Features

- VME64x interface
- Two Low-Pin Count FMC slots
  - Vadj fixed to 2.5V

Example Layout for HiSCORE clock/trigger (~CTA)

HiSCORE / EA : 20-40 DAQ-Stations (km2 prototype)

CTA : 50-100 Telescopes

> *Array center:*

WR-switches (18 x out) - with N=4 → 67 Stations/Telescopes

(+ 1x GPS / GPS-disciplined Rub.Clock)

> *Dedicated SM-fiber* to every Station / Telescope

> *Every Station / Telescope:*

Houses one WR-SPEC time-latching unit : SPEC

> Price: *O(1100Eur) per station*

= 900 (SPEC+DIO) + 1/17 x 3500 (WRS)

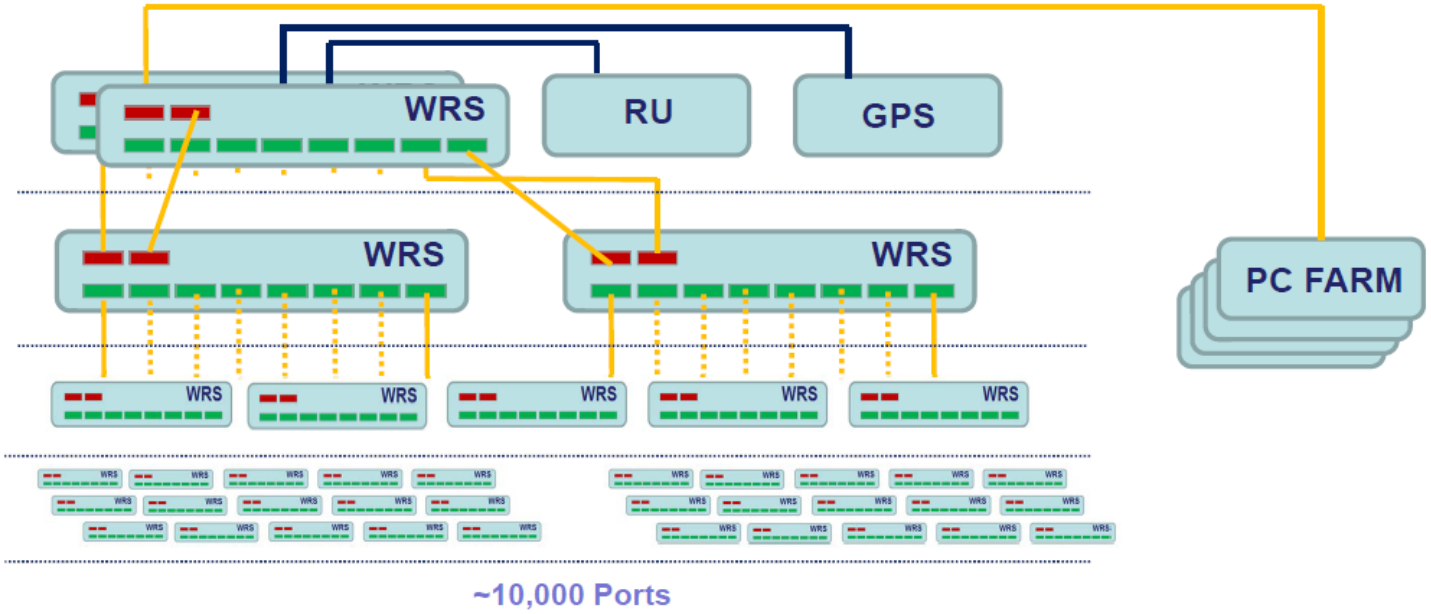
(very conservative)

Example: LHAASO - WhiteRabbit Layout

> Other WR-application proposals:

- **LHAASO : ~10000 nodes to synchronize**

Design study
G.Gong, ICALEPCS, 2011.

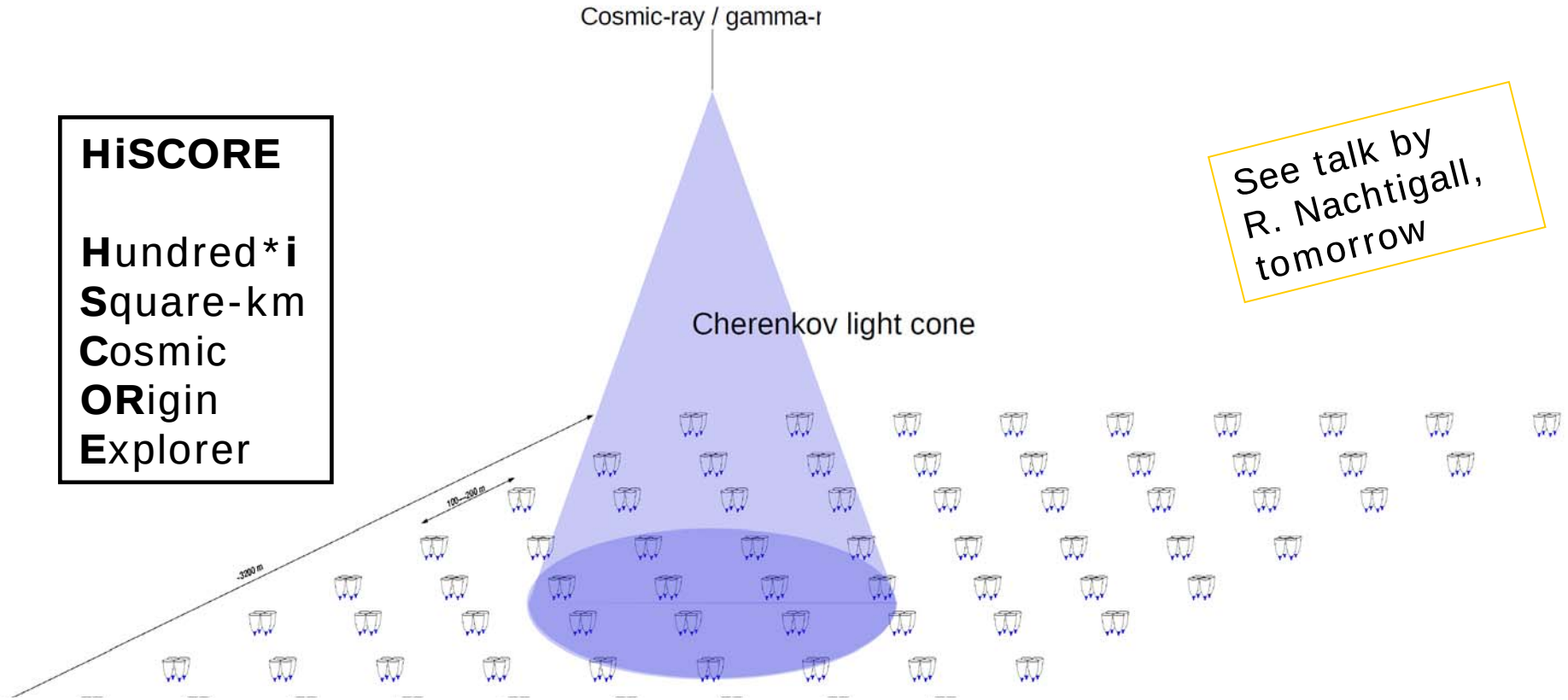


HiSCORE – Verifiying WR in a first AP-Experiment

- HiSCORE – a non-imaging atmospheric Cerenkov Array : UHE-Gamma-Ray (0.03-1PeV) and Cosmic-Ray Physics
  - Proof-of-principle with prototype setup in 2013/14 @ Tunka-valley/Siberia
- DetectorStations (0.5m²) distributed over >1km²-100km²
- Required: nsec precision relative timing in all stations

HiSCORE

Hundred*__i__
Square-km
Cosmic
ORigin
Explorer



See talk by R. Nachtigall, tomorrow

HiSCORE: The DESY - WR SPEC modifications

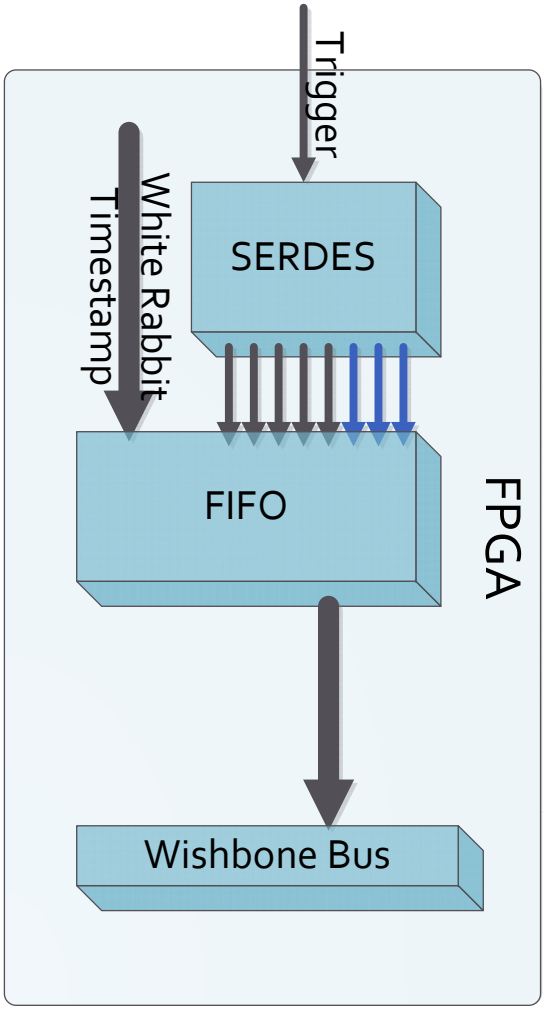
- 8 ns time stamping at first
- Then added an in-FPGA TDC* with a SERDES block
- Current resolution 2 ns (see next slide)
- Connected TDC to Wishbone Bus

- Print trigger timestamp on terminal
- Send timestamp over WR-link via LM32 CPU with a maximal rate of 1 kHz

➔ Standalone mode

➔ Very accurate time base and stamping

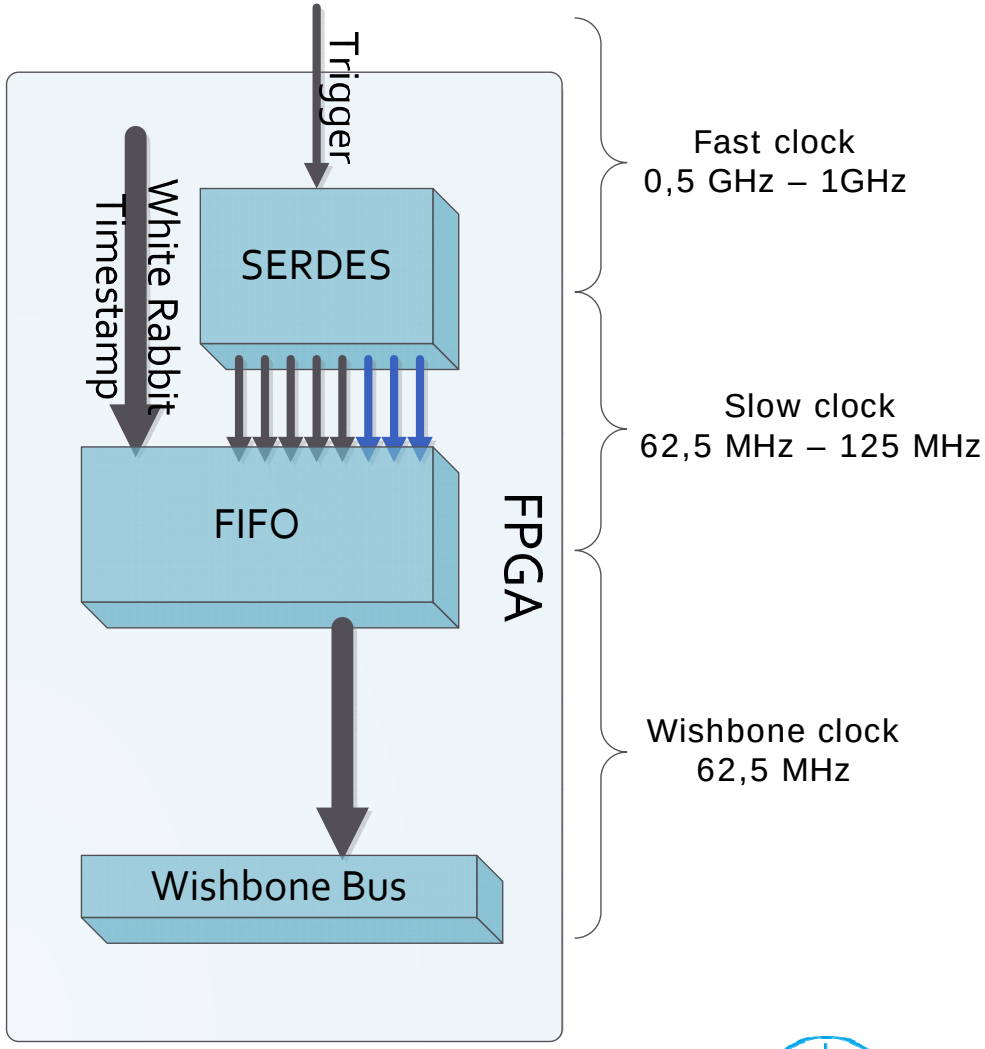
➔ Possibility to send calibration pulses to the detectors



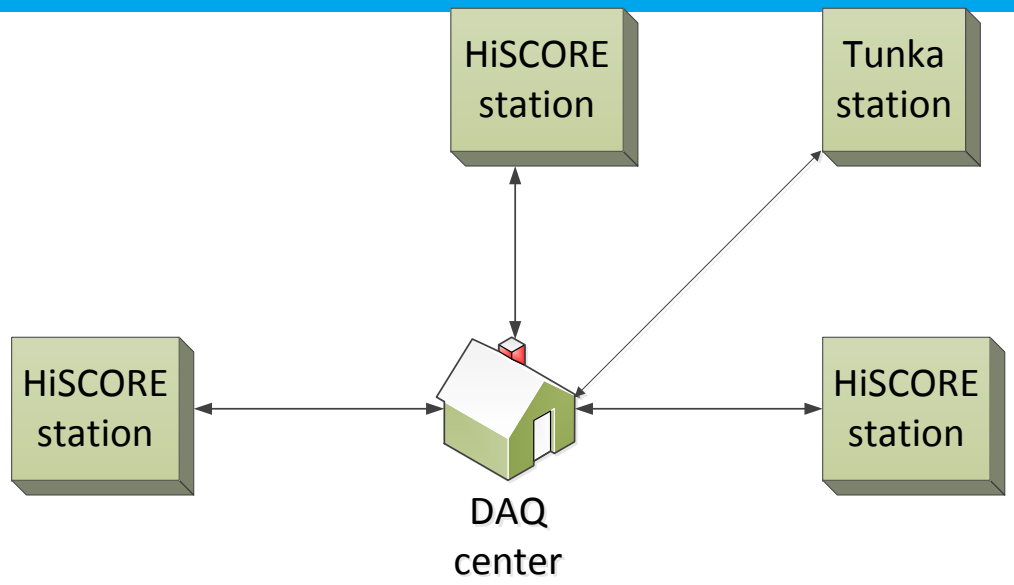
* programmed by Sébastien Bourdeauducq

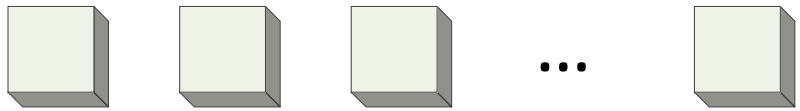
WR modifications – TDC

- SERDES block needs two phase aligned clocks:
  - Serial fast clock
  - Parallel slower clock
- Easy way: Use the same PLL which generates the 62,5 MHz Wishbone Bus clock to get a 500 MHz phase aligned clock for 2 ns accuracy
  - We did this because of not touching too much of the White Rabbit timing system
- Future: Use the WhiteRabbit 125 MHz clock to generate 1GHz for 1 ns accuracy
  - OK, Tom did this ☺ Thanks



HiSCORE - Prototype setup (Oct/2012)



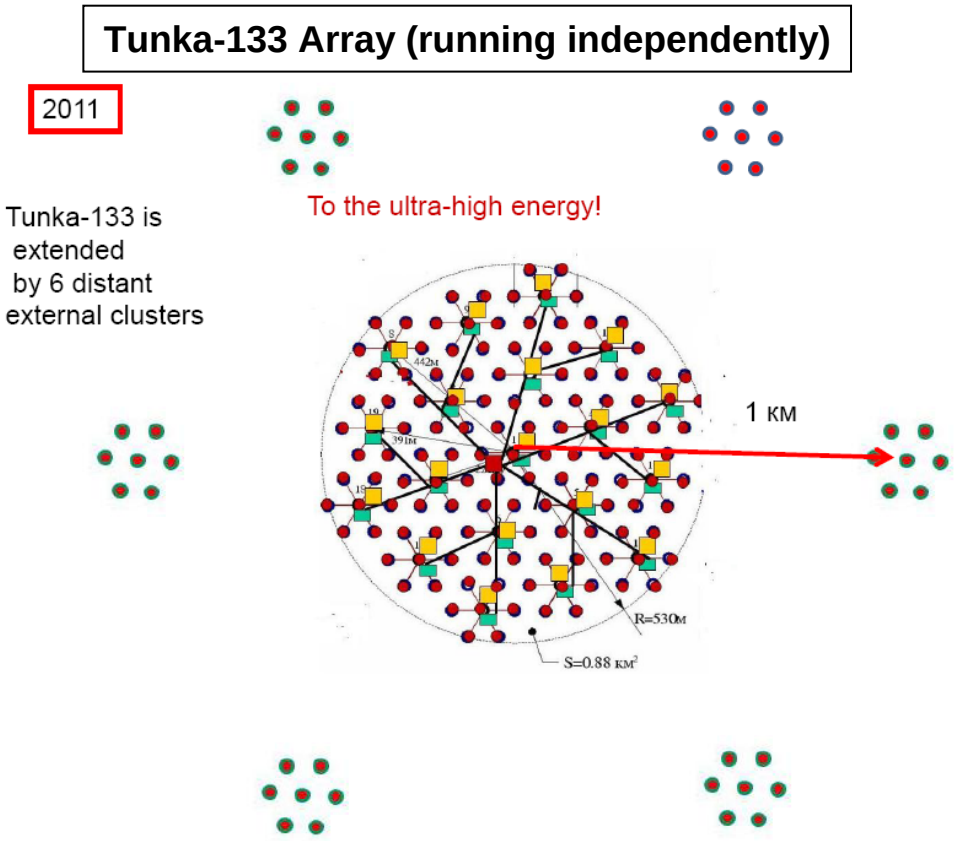


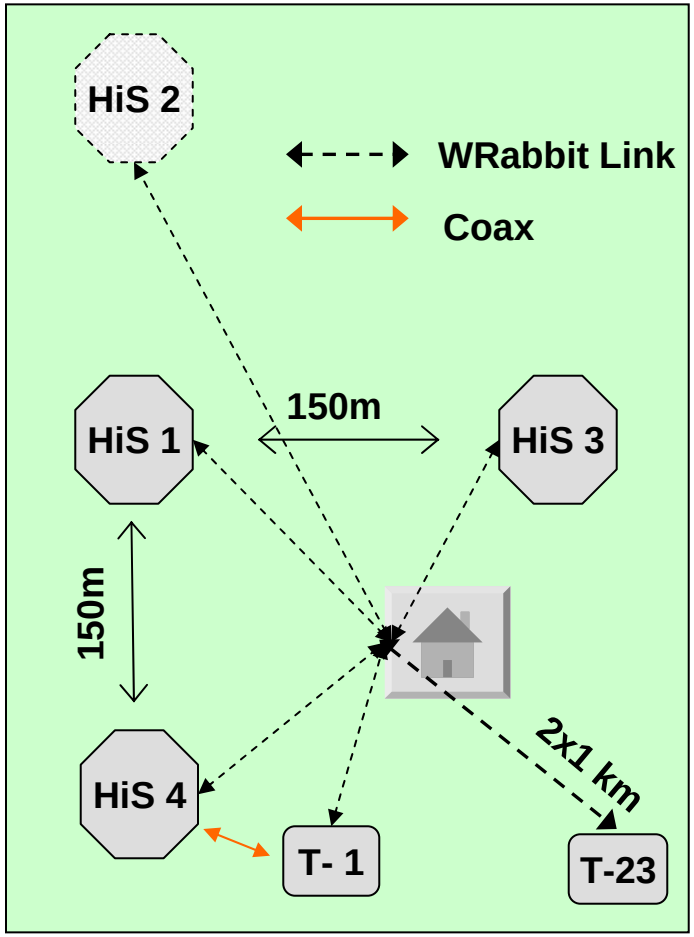
More HiSCORE stations in future

- Prototype Setup: installed Oct.2012
- 1 km² in 2013/14 : 20-40 stations
- 100 km²: > 2000 stations

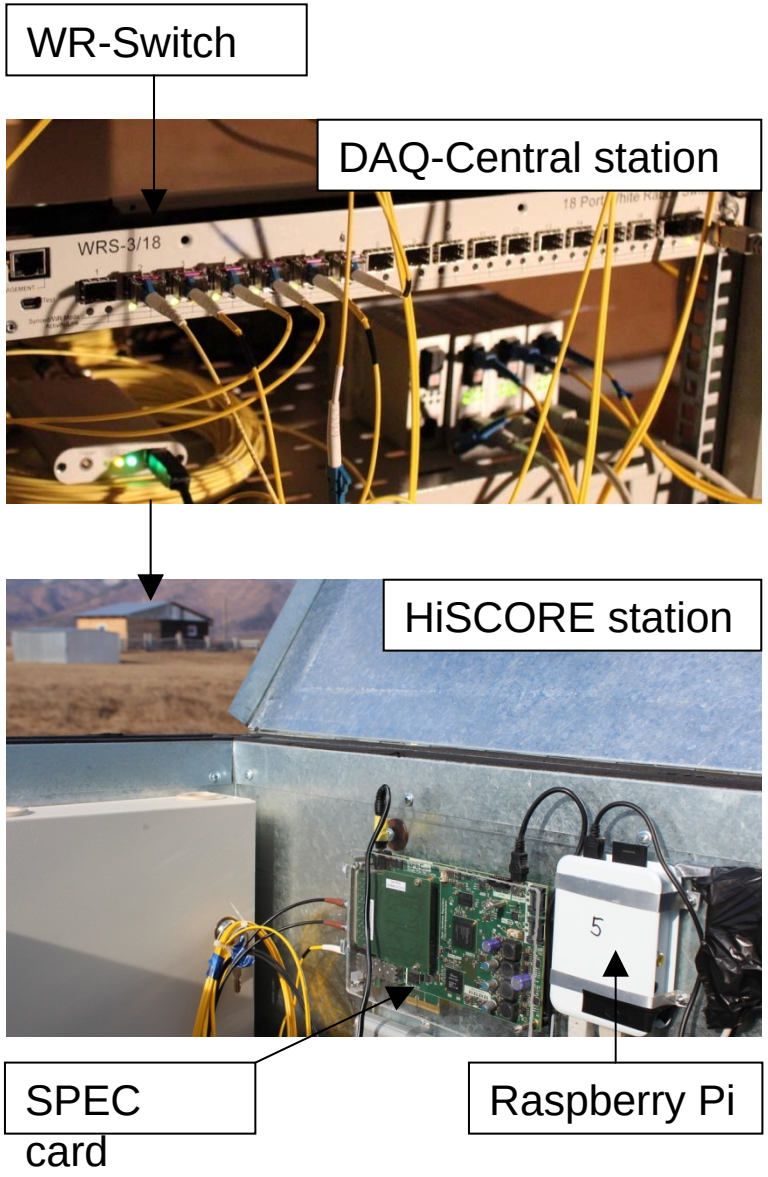
Tunka & HiSCORE prototype setup

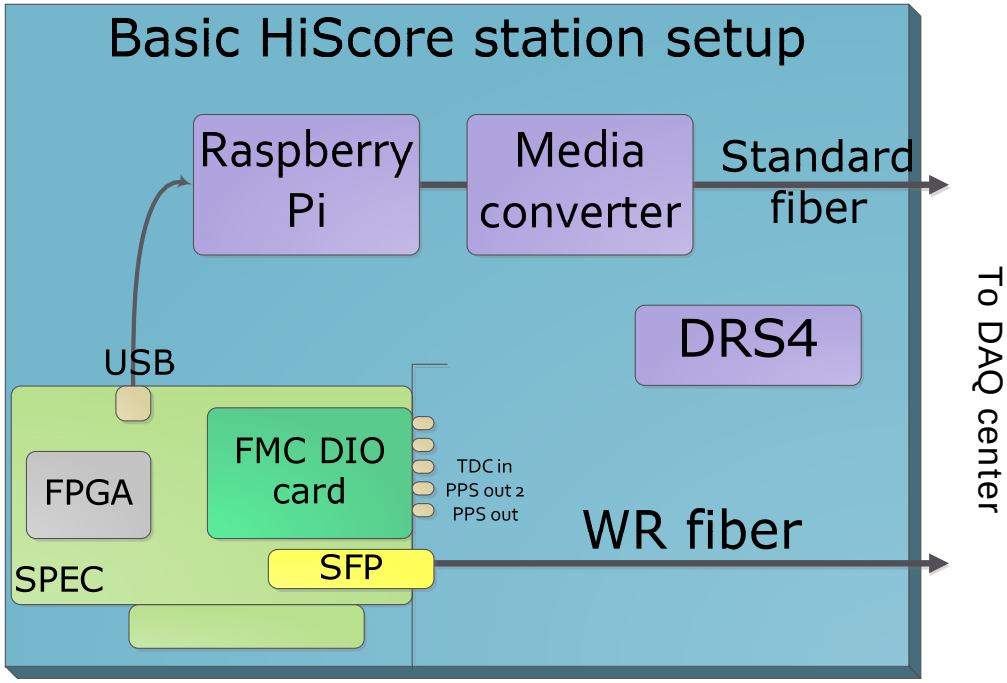
> Three HiSCORE Prototype Stations deployed in Oct.2012





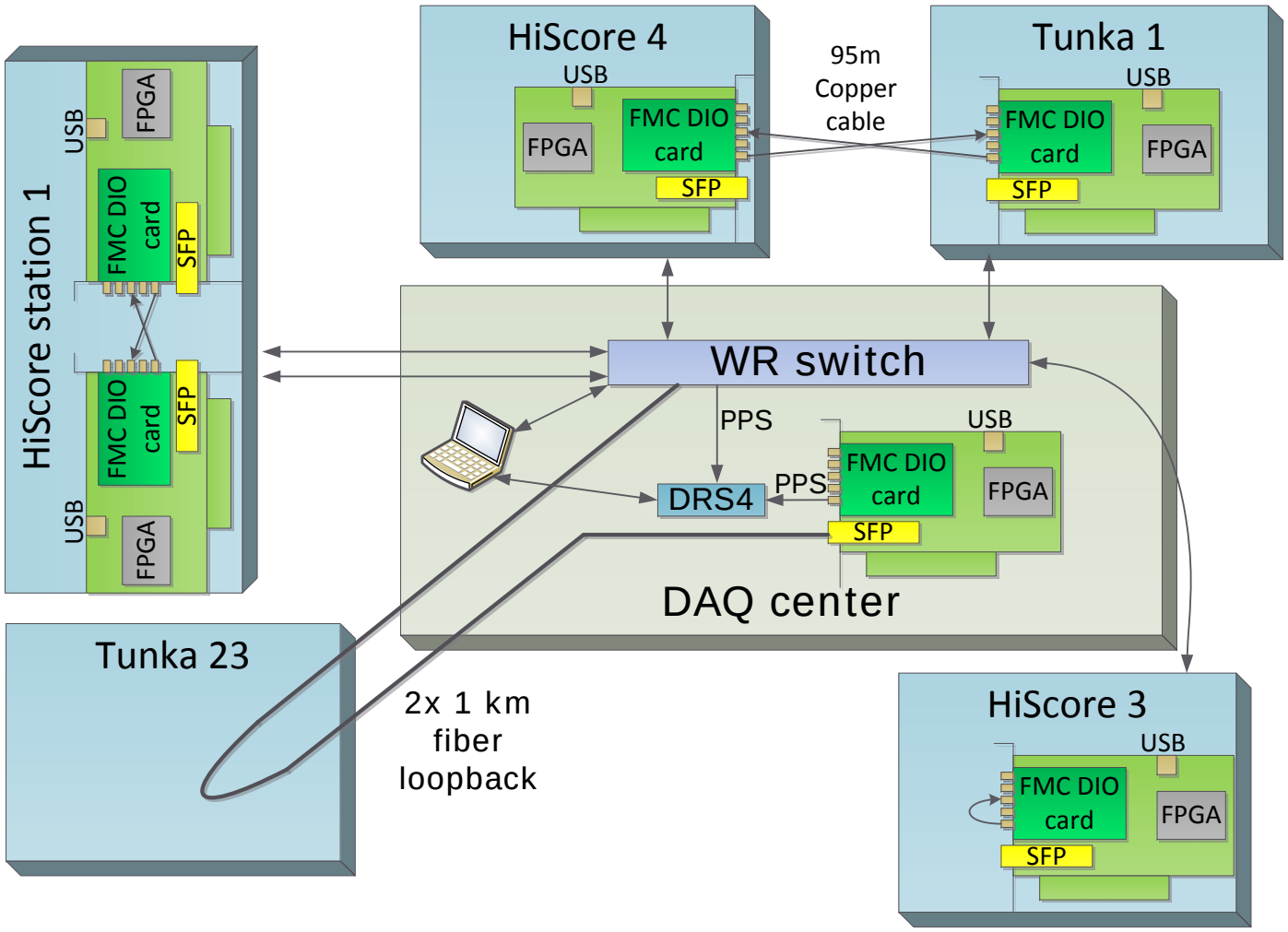
HiSCORE setup overview





- DRS4 as 5 GHz “digital scope”
- Raspberry Pi transports
  - USB Terminal
  - DRS4 (Domino Ring Sampler)
  - Temperature sensor
  - …

HiSCORE setup



- PPS signals (DIO output 1) connected to TDC-inputs (DIO input 3)

HiSCORE setup: measurements

Installed a number of redundant cross-calibration options :

> 2km loopback fiber cable connected to DRS4 to measure and test WhiteRabbit PPS signal (Laboratory located)

> Loopback PPS connection to test TDC performance (HiS 3)

> Crosswise PPS->TDC connection to test TDC and WhiteRabbit

- Within 1 station (HiS1)
- Between 2 stations (HiS4 + Tunka-1), connected by 95m copper
- Now: based on 2ns-TDC (SPEC)

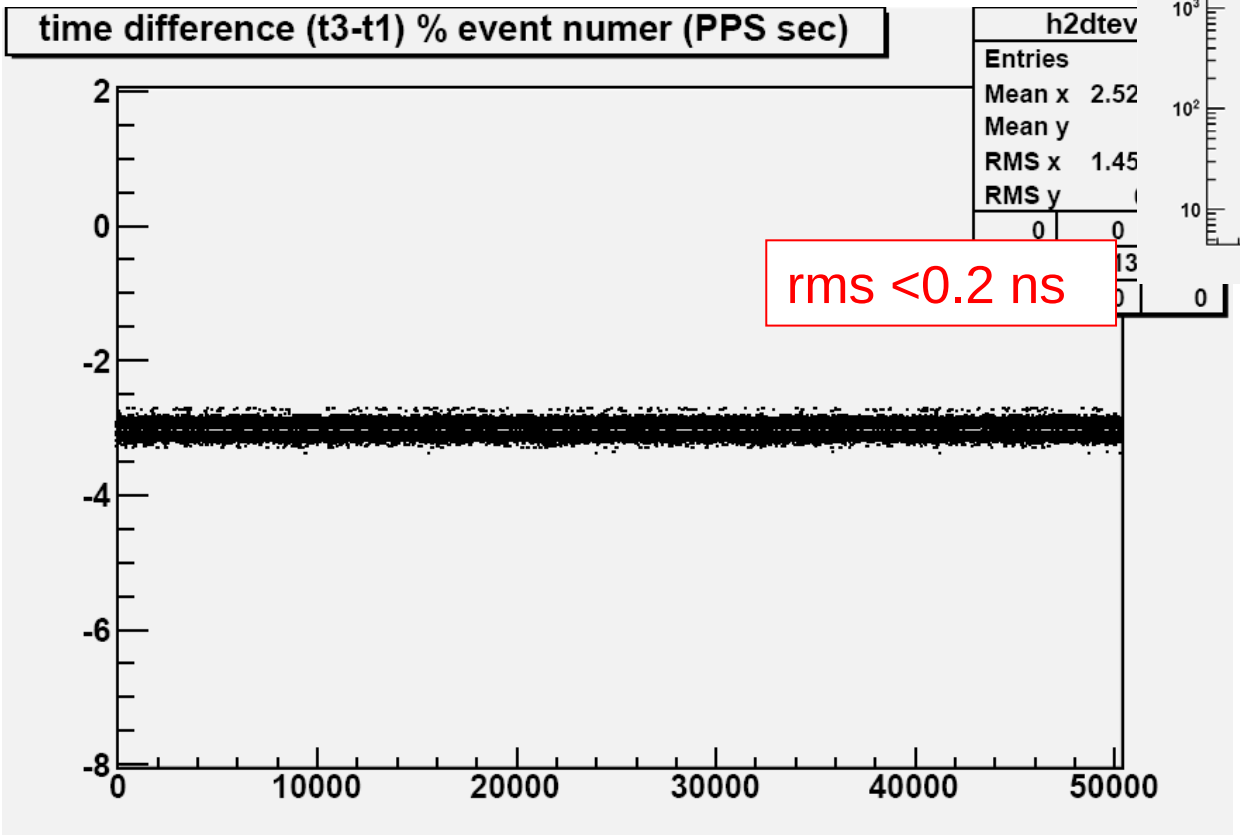
  future: use DRS4 for higher precision (5GHz sampling)
- Future: connect nsec-precision GPS to stations (candidate for a flexible field calibration tool; if GPS reaches nsec-precision)

Results - 2 km fiber loopback with DRS4

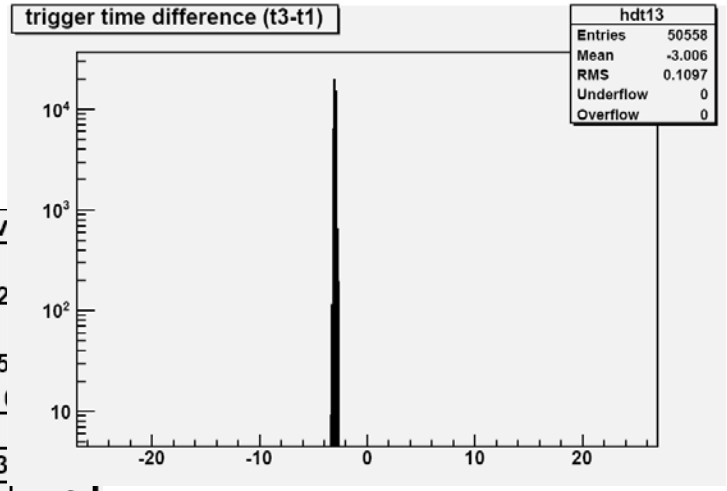
1. Test :

LoopBack Fiber over 2x1km
back to Laboratory

(5GHz DRS4-measurement)



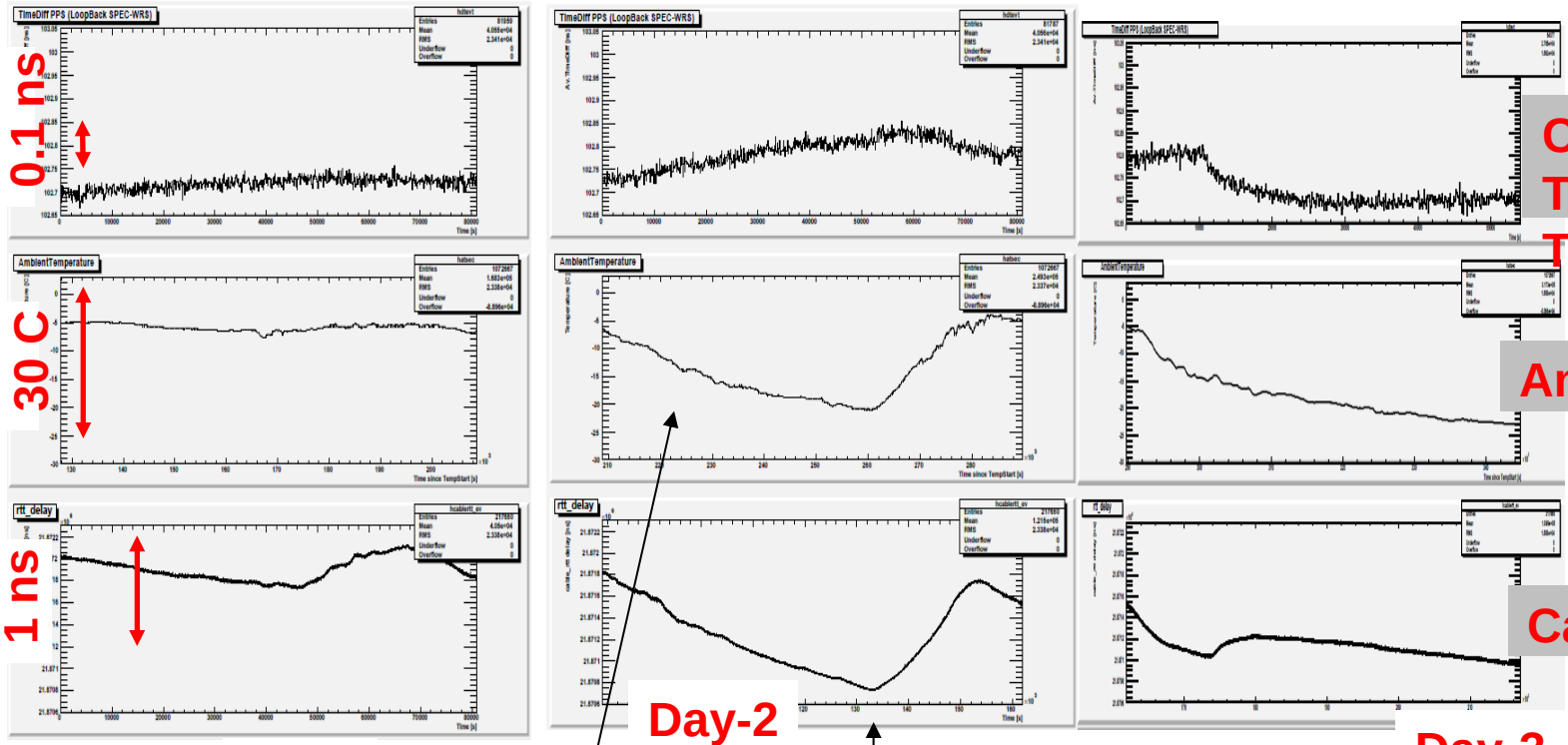
rms <0.2 ns



example:
14hr HiSCORE run

Measurements: 2 km Fiber Loopback

2km Loopback WRS-SPEC (Lab.) : Clock-offset via 1PPS pulses



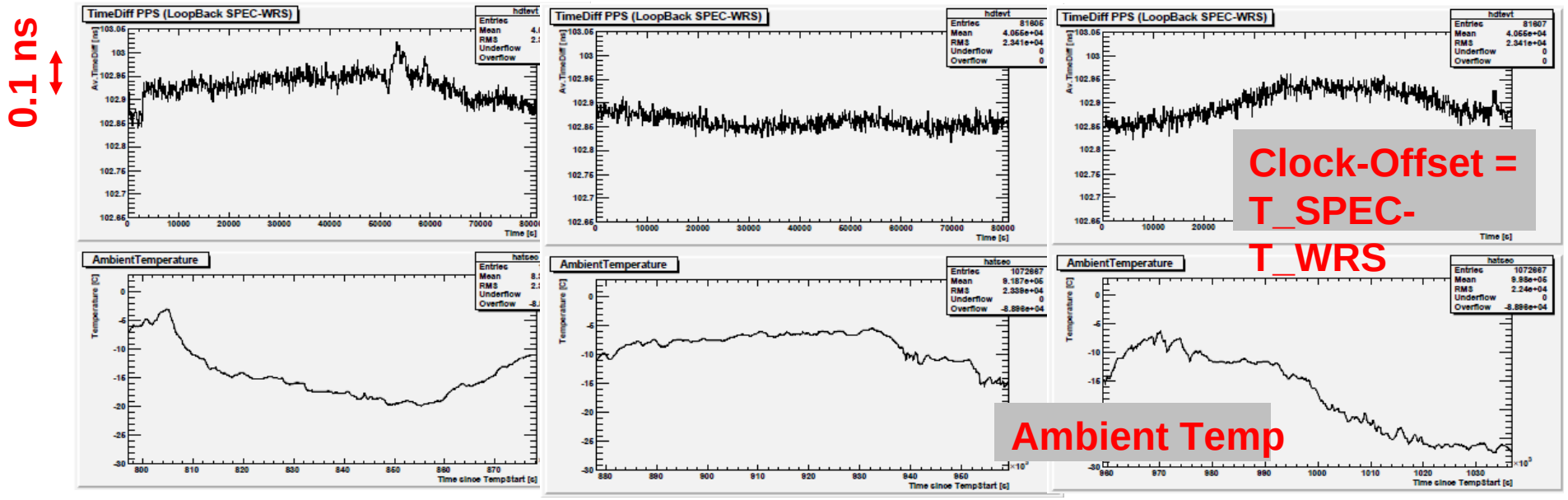
- Delay for 15 C : 4km x 40ps/km/C = 2.4ns > 1 ns

→ AmbientTemp .ne. FiberTemp ?!

Clock-Offset uncorrelated to Ambient Temp

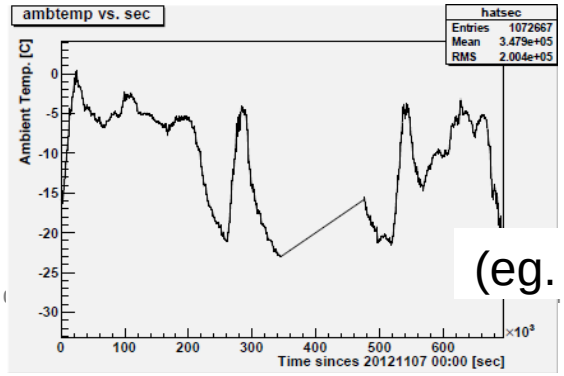
Measurements: 2 km Fiber Loopback (2)

> 2km Loopback WRS-SPEC (Lab.) : Clock-offset via 1PPS pulses



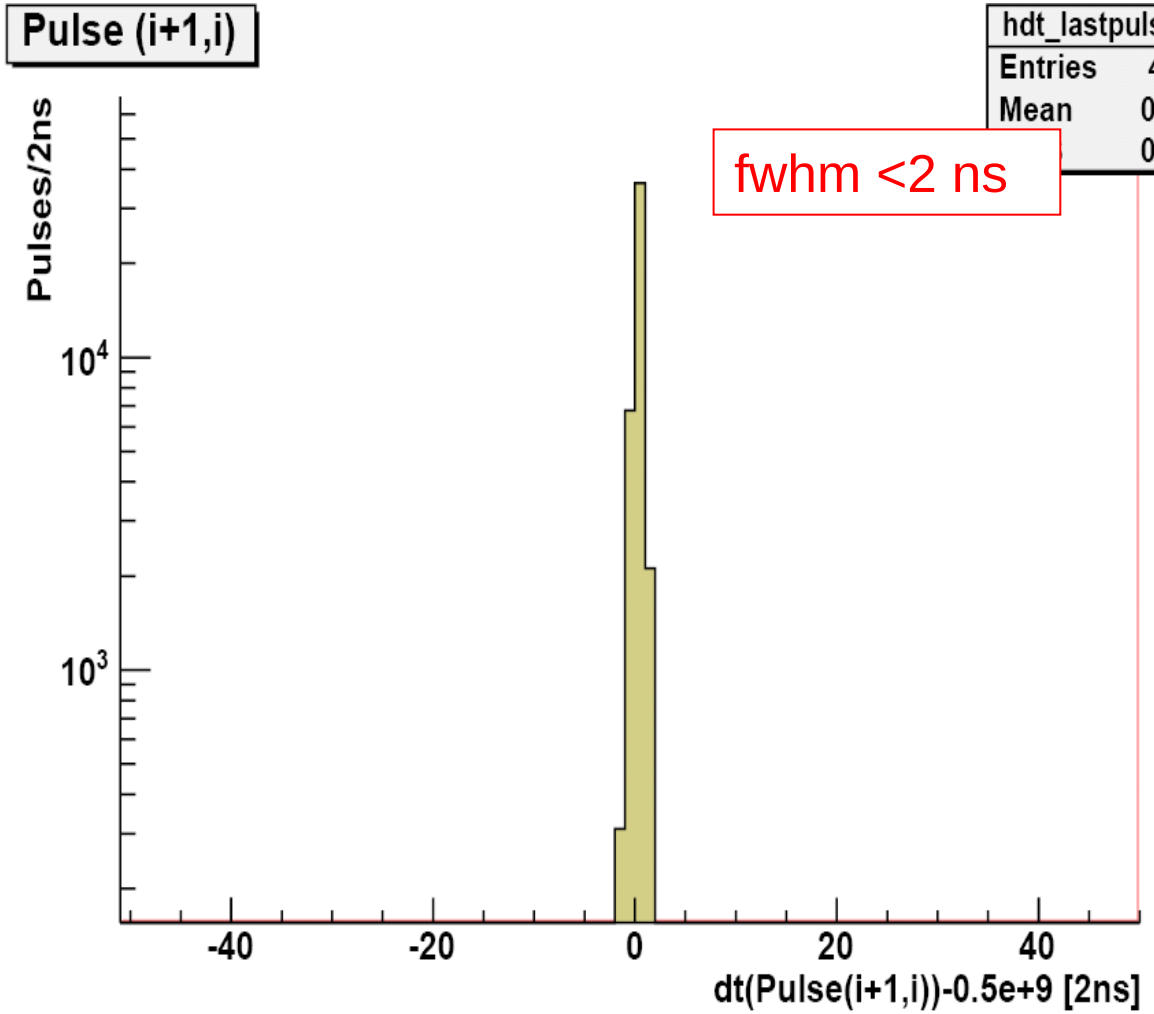
- Clock-Offset: 100s averaged – Clear trends @ 100ps scale
- largely uncorelated with ambient Temp. → Board temperature ?
- New sensors to be installed.

- A wide temp-range covered:



(eg. 8 days)

Results – Timestamping

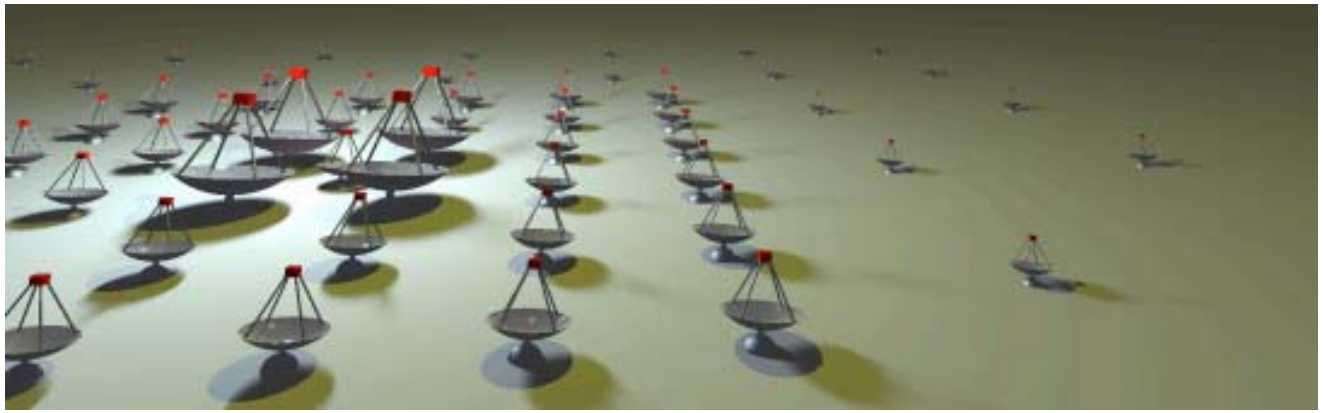


Tunka 1 pulses measured in HiSCORE4 via copper cable (2ns TDC resolution, 12hr run).

2ns/bin; average == 1.00sec

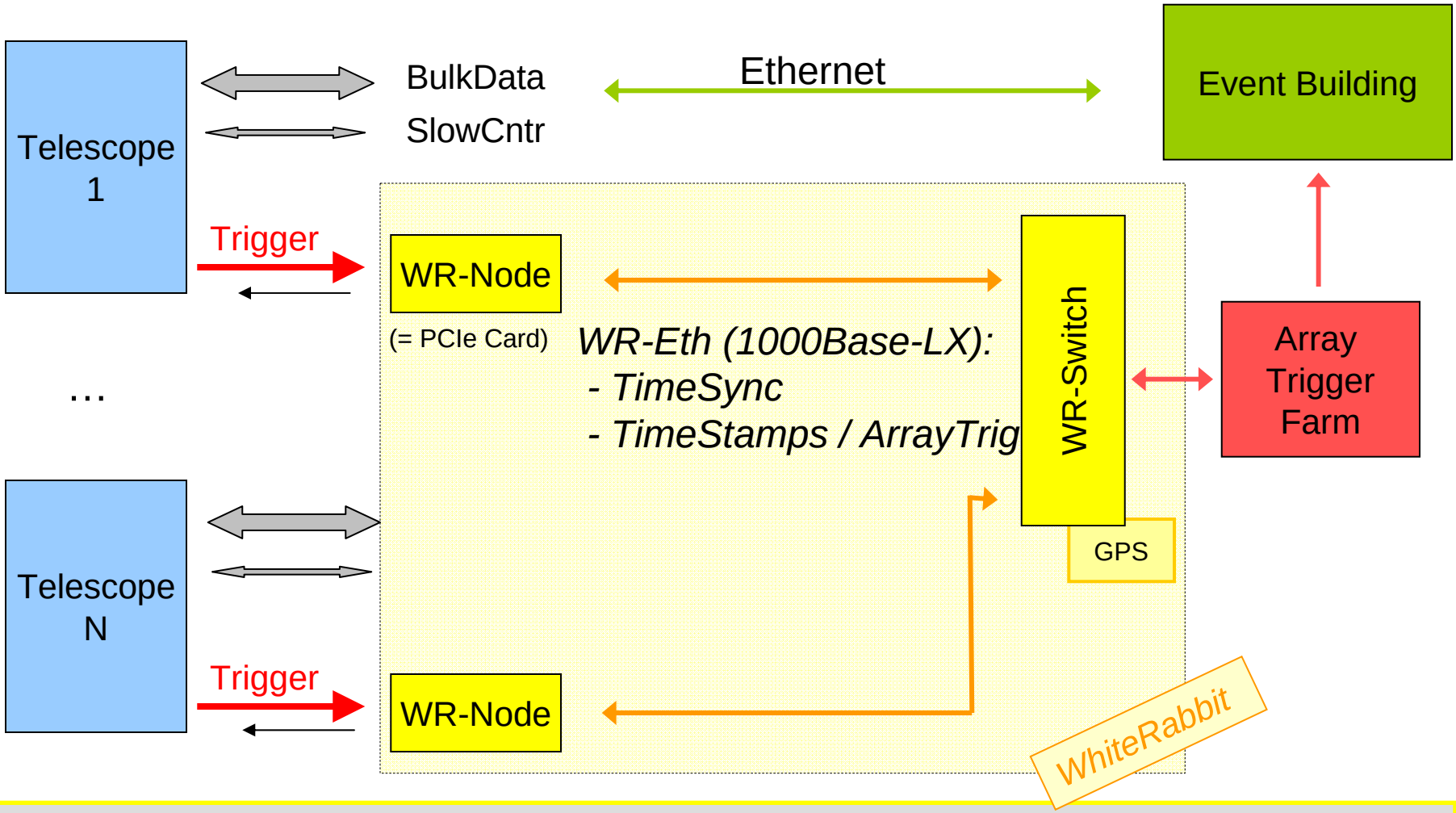
CTA: Discussing Plans for Cherenkov Telescope Array (CTA)

- Array of 50-80 Telescopes over few km2
- Intra-telescope: nsec timing
- Inter-telescopes timing with nsec precision
- “Array trigger” (Stereo) based on fast telescope time-stamps & o(100)nsec window
- WR considered so far for small and medium size telescopes (SST / MST)



White Rabbit for CTA : a candidate layout for Array-Timing, TimeStamping & ArrayTrigger

1st Draft for WR application



Only a few components are needed:

- per telescope : 1 x WhiteRabbit Node (PCIe) + 1 standard fiber (SM;1390/1510nm)
- per array : 1…n WhiteRabbit Switches

Discussion : How do I use WR

FAQ:

“ I have a DAQ/FE-Board. Can I use White Rabbit fro ‘timing’? How ?”

> (1) Simple Case :

Q: My DAQ generates a trigger and reads out. Needs only a time-stamp for the trigger-time; all R/O data (FADC,TDC, …) are relative to that trigger time.

A: Take a setup like HiSCORE/DESY or CTA/DESY – and you are done.

> (2) More complex

Q: My DAQ/FE-boards does not generate a trigger, but reads out “permanently”, or triggers internally (FPGA), without an external trigger signal.

A1: If you have a GPS-interface for synchronization – good. Need to adapt WR/SPEC to GPS-SerialIF. PPS is there. Done.

A2: Otherwise: You need to think about a “clock – information transfer”.

Conclusion : General

- White Rabbit is an excellent choice for sub-nsec time-synchronization in astroparticle experiments. For laboratory scale to large field experimental setups. Phase stability of <0.2ns, precision <1ns.

- Main advantages:
  - Real standard, commercial support, open source HW & SW
  - Reliability, easy maintenance, cost effective, scalability, …
  - Soon a big user-community. Eg. HiSCORE, LHAASO, CERN, CTA …

- In HiSCORE: WR is used for the prototype array.
- In CTA, White Rabbit is a candidate for SST / MST (LST) for :
  - Time-synchronization: local clocks - specs are fulfilled
  - Array trigger : favourable network architecture for time-stamp based coincidences fast coincidences (Level-2 trigger)

Conclusion : General (2)

HAP / Astroparticle related:

- Building up a minimal AP (HAP) ‘user community’ will lower the threshold for small groups to join;
  - minimal funding for a few FPGA-designs would allow for a few standard use-cases
  - GSI: strong WR-group, might also join
- Discussion item

Conclusion : WR @DESY & HiSCORE

- WR at DESY/HumboldtUnivBerlin started in February 2012
- Initial SPEC-SPEC tests at HiSCORE site in April
- First work w/ WR-Switch (vs.3.2) started in July 2012
- Installed HiSCORE setup in October and started routine measurements in field
  - TDC , Trigger Latching & Fiber Readout, Standalone SPEC operation
- First results:
  - all components work as expected, no failures
  - <200 ps Jitter WhiteRabbit switch ← 2km fiber in field → SPEC card

    Residual drift at 100ps level.
  - FWHM < 2ns TDC time stamping jitter (more precise measurements soon)
  - Information from HiSCORE as a first reference setup is valuable for WR.
- Collaboration with other AP (HAP) groups interested in WR is welcome.

Outlook

- Advanced cross calibration tools:
  - NEED for a “nsec-GPS clock”
  - radio-phase alignment
- Improve TDC-resolution: 1 ns TDC (or better)
- Collecting more field-measurement data
- In collaboration with other WR-teams ?
  - Welcome are suggestions from WR-community ? Sharing the data ? ….

End

> Thank you