HAP Workshop Topic 4, Advanced Technologies at KIT, CN

Summary parallel session #1:

“Digitizing analog signals at high sampling rate and bandwidth”

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General discussion

Options for digitization:

- traditional FADCs, also possible for up to 5 GHz
  - continuous sampling, full information, standard for low # of channels
- interleaved sampling
  - factor 2-4 higher rate, but also higher effort; good timing needed
- use of Switched Capacitor Arrays (SCA)
  - good solution for high # of channels with low rate of triggers
  - low power, low cost, variety of chips, sampling rates in GHz range

    → interesting of many applications and groups
  - focused discussion on DRS4 chip and future trends

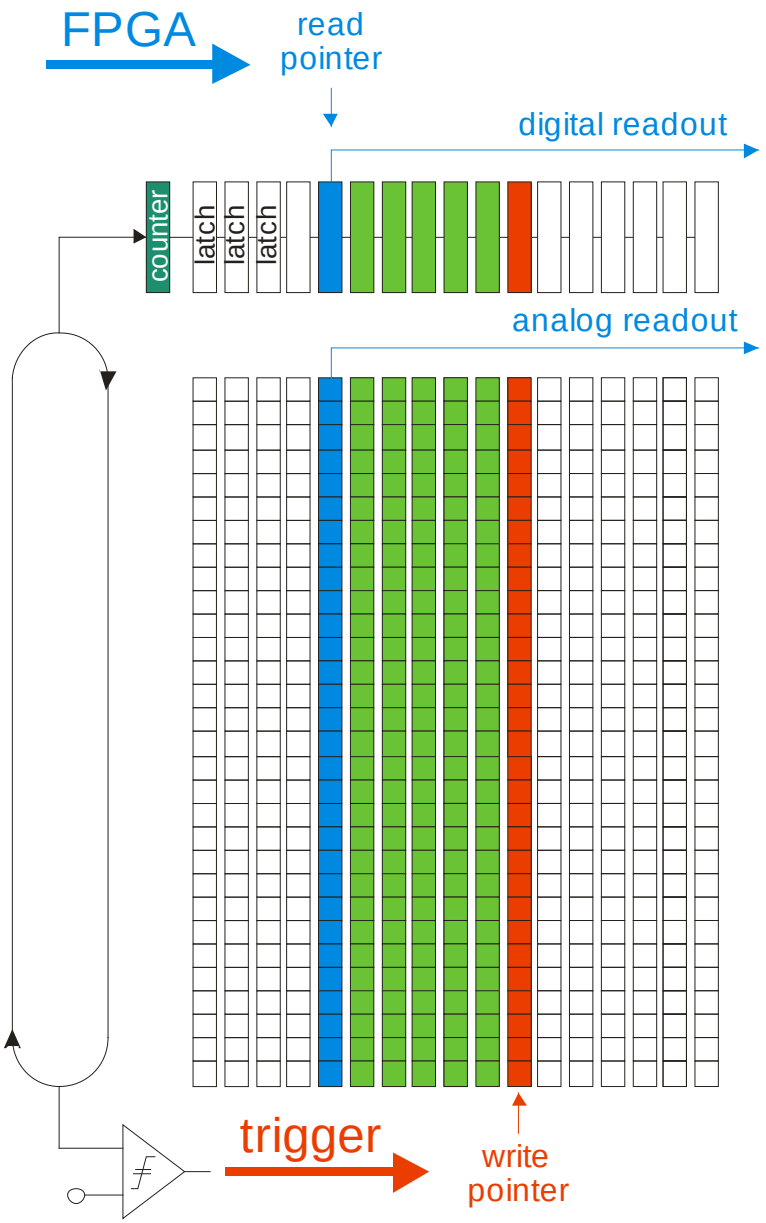
Plans

DRS5 (PSI)

- Self-trigger writing of 128 short 32-bin segments (4096 bins total)
- Storage of 128 events
  - Accommodate long trigger latencies
  - Quasi dead time-free up to a few MHz,
  - Possibility to skip segments
    → second level trigger
- Attractive replacement for CFG+TDC
- First version planned for 2014

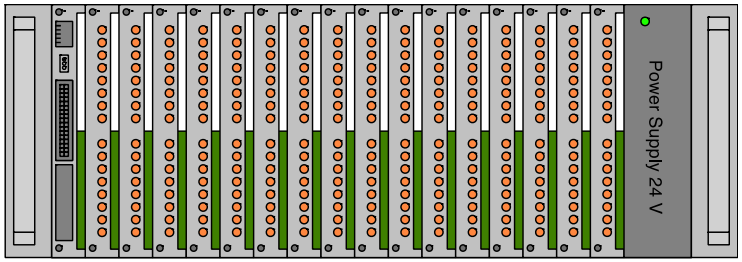
CEA/Saclay

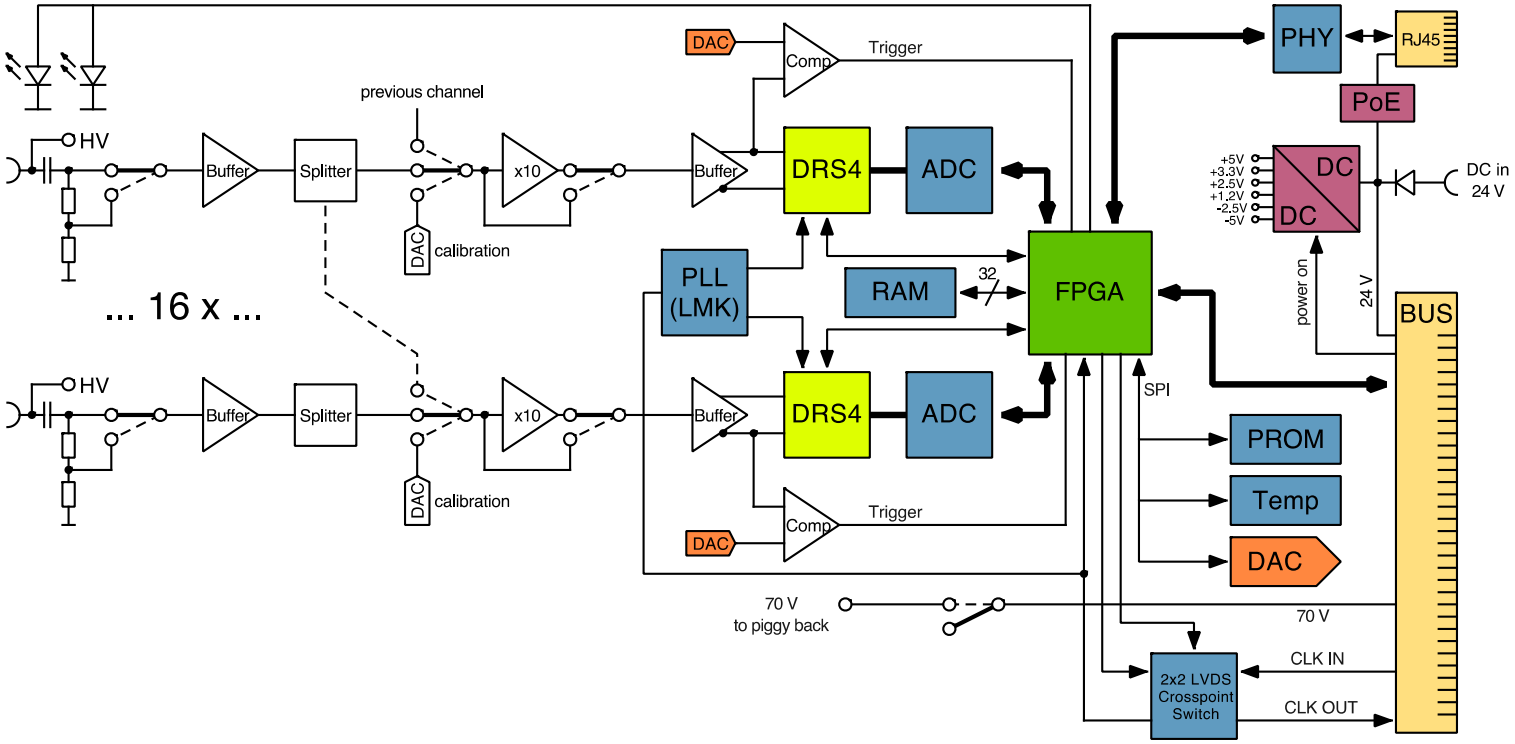
- Dual gain channels
- Dynamic power management (Read/Write parts)
- Region-of-interest readout



WaveDREAM board

- 16 channels standalone (GBit Ethernet) or 3HE crate (256 channels)
- Variable gain 0.1/1/10 or 1/10/100
- Flexible integrated triggering
- Global clock synchronization
- Integrated SiPM biasing (up to 200V)
- Currently under development at PSI





Conclusion:

Switched capacitor arrays are good solutions for many cases. They are especially attractive for:

- systems with many channels
- sampling of rare events with high time resolution
- low power applications
- low chip counts and low price

Points to take into account:

- designs for low /no dead time
- where to procure the chips
- wait for new design family with more flexibility