Backend Design of the Read-Out System for Cryogenic Particle Sensors

HIRSAP Workshop 2021 - Karlsruhe, Germany

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UNSAM Director:
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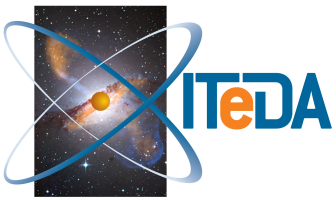
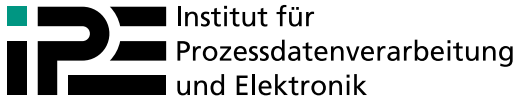
Scientific Supervisor:
PD. Dr. Oliver Sander

KIT Director:
Prof. Dr. Marc Weber

ITeDA - Instituto de Tecnologías en Detección y Astropartículas, Buenos Aires, Argentina
UNSAM - Universidad Nacional de San Martín, Buenos Aires, Argentina
KIT - Karlsruher Institut für Technologie
IPE - Institut für Prozessdatenverarbeitung und Elektronik, Karlsruhe, Germany



UNSAM
UNIVERSIDAD
NACIONAL DE
SAN MARTÍN



Introduction

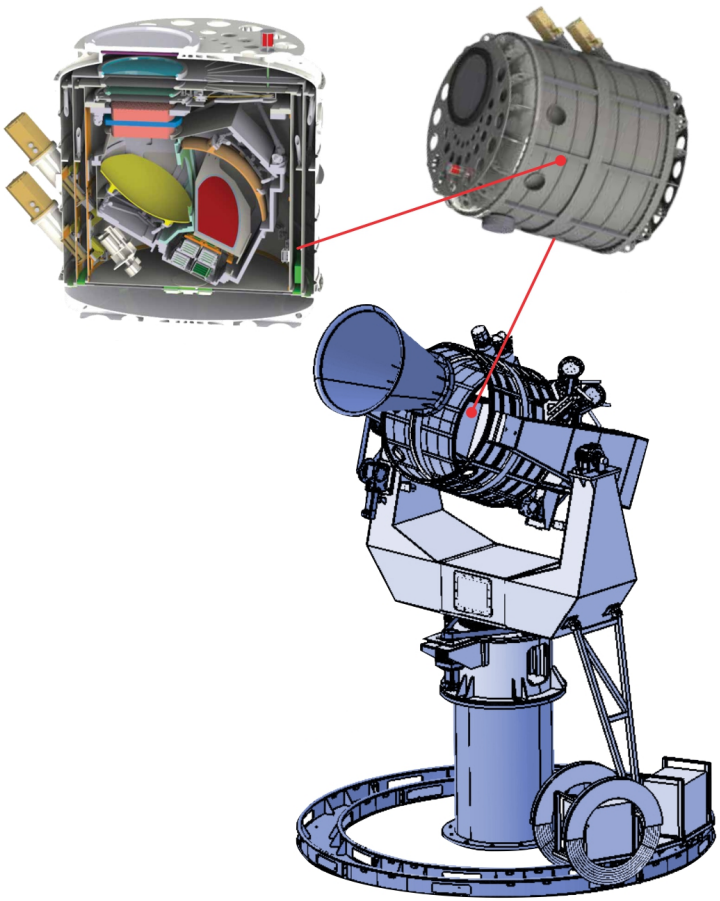
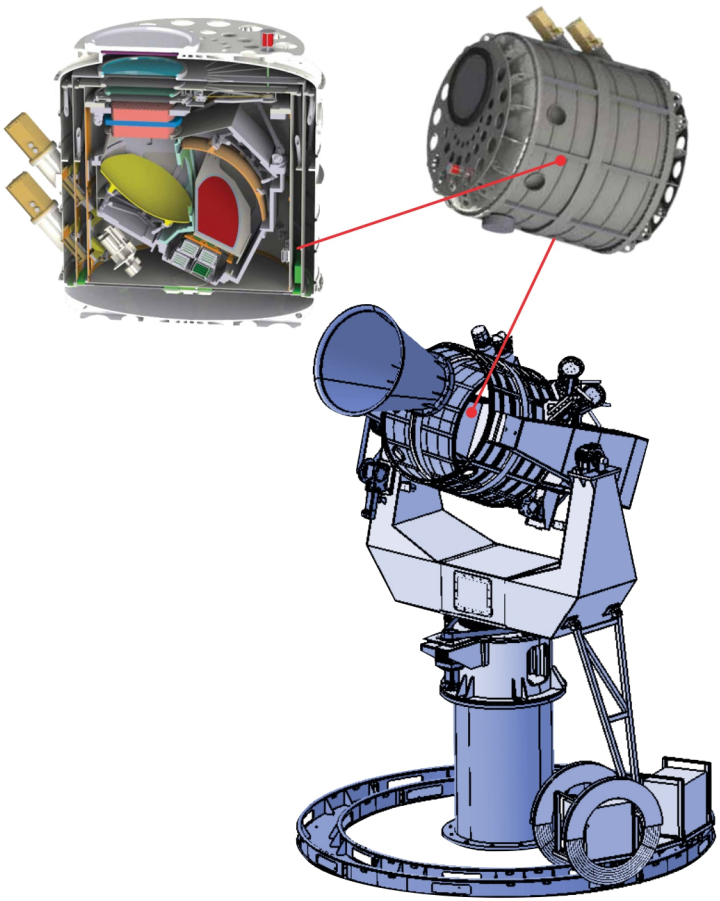


Figure: The QUBIC Instrument [1]



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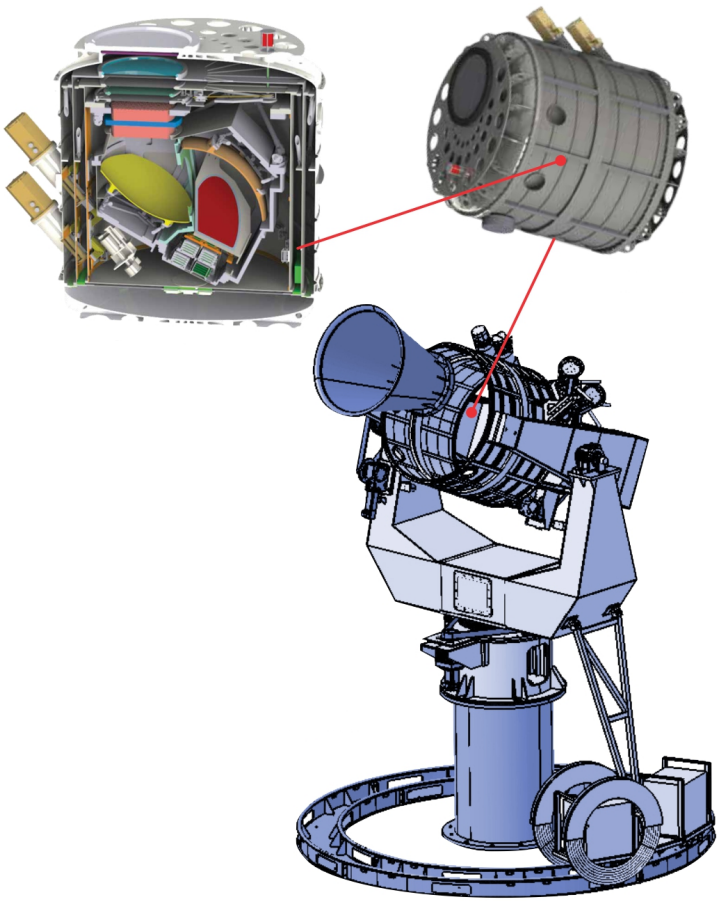
- 130 Collaborators, 22 Laboratories, 6 countries: France, Argentina, Italy, Ireland, USA and UK,



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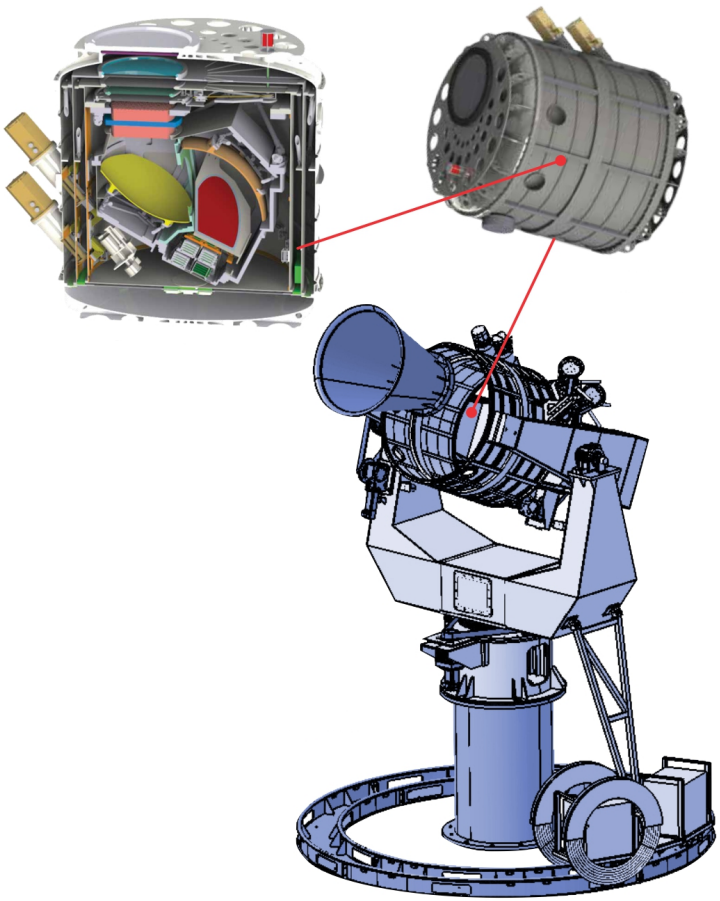

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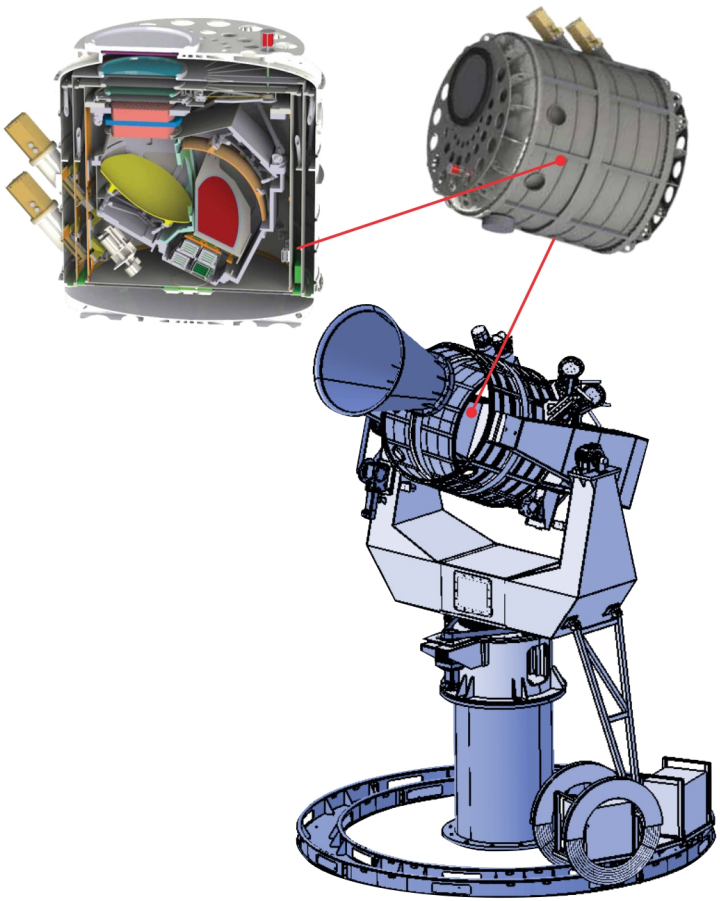

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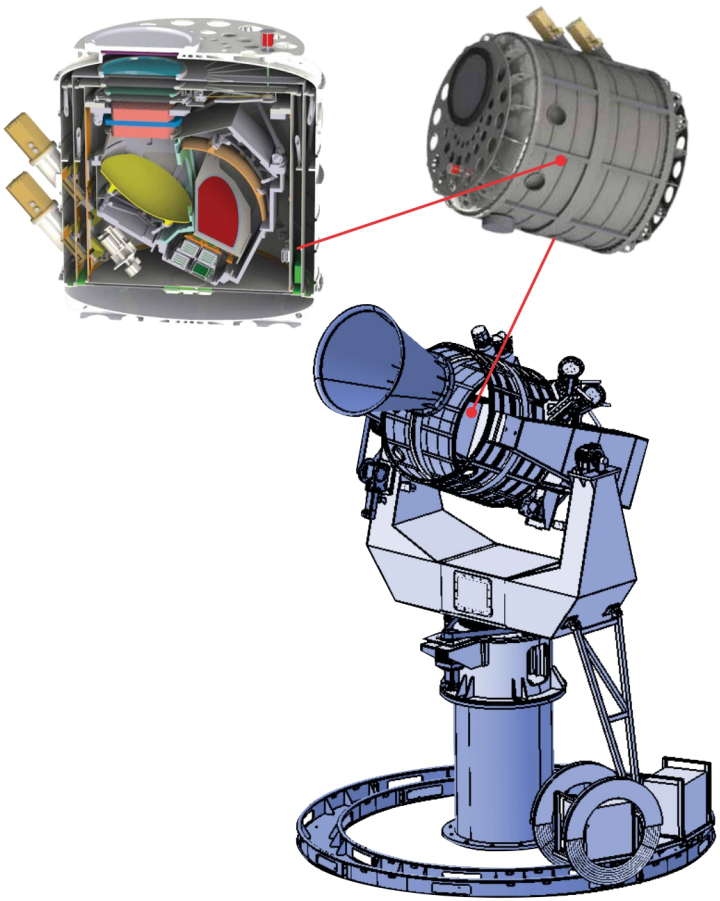

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- Combines 2 techniques: bolometric (sensitivity) and interferometric (control of systematic erros),
- Working range: 150 GHz y 220 GHz bands.

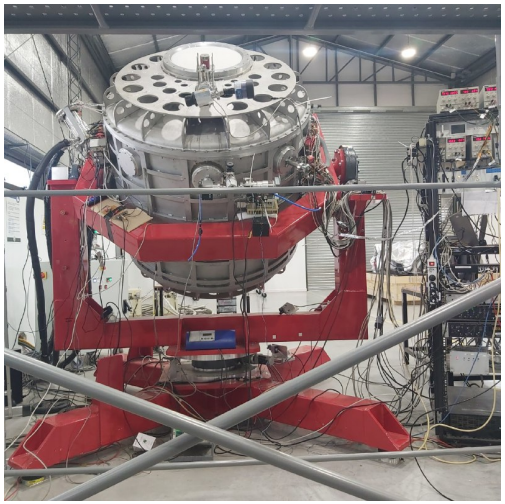

Figure: QUBIC Technical Demonstrator

Thesis goals

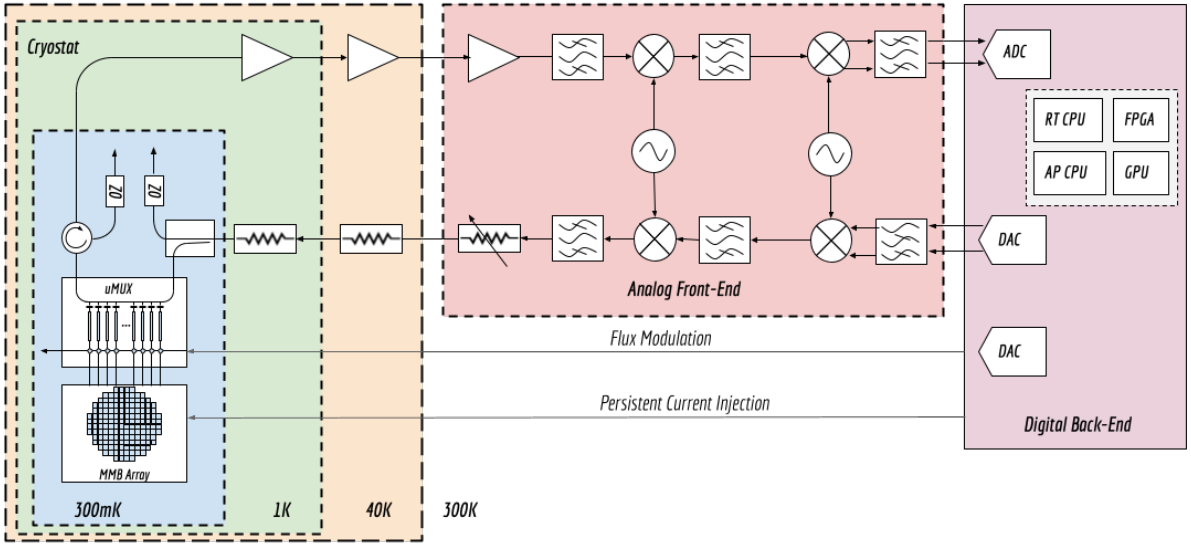

Figure: Proposed Read-Out Electronics for CMB Experiments

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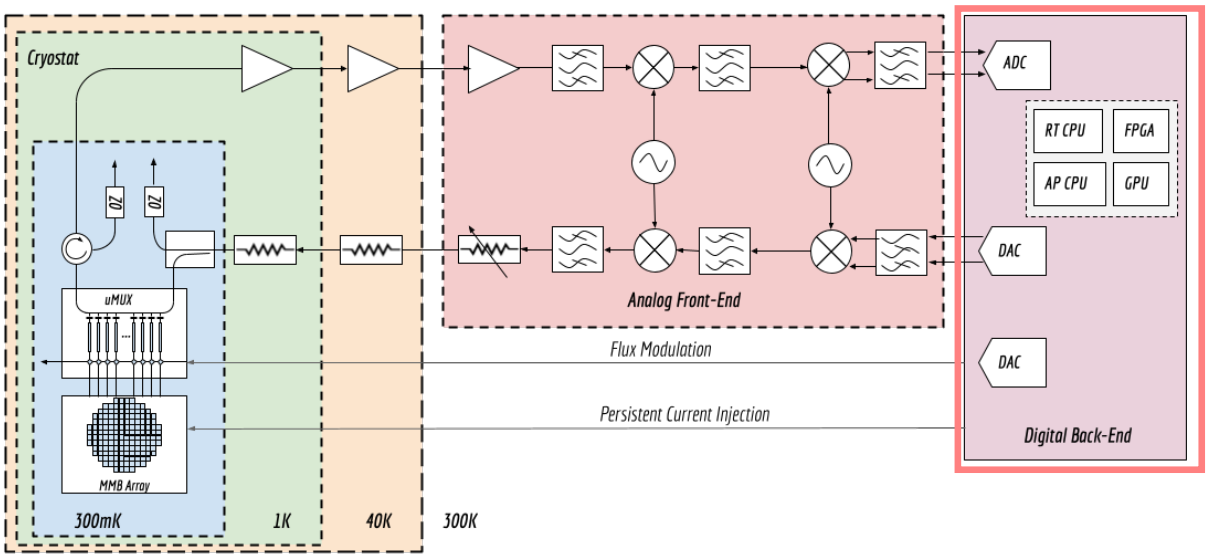


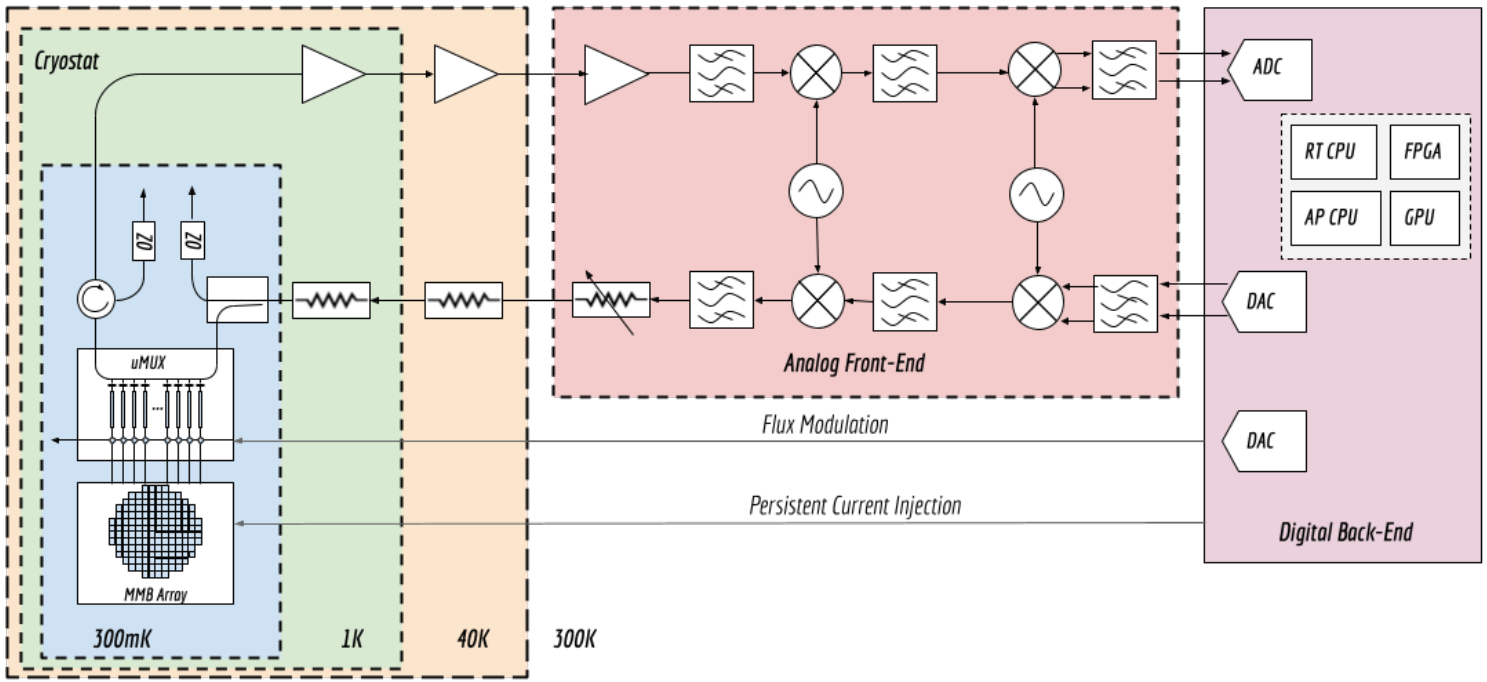
Figure: Proposed Read-Out Electronics for CMB Experiments

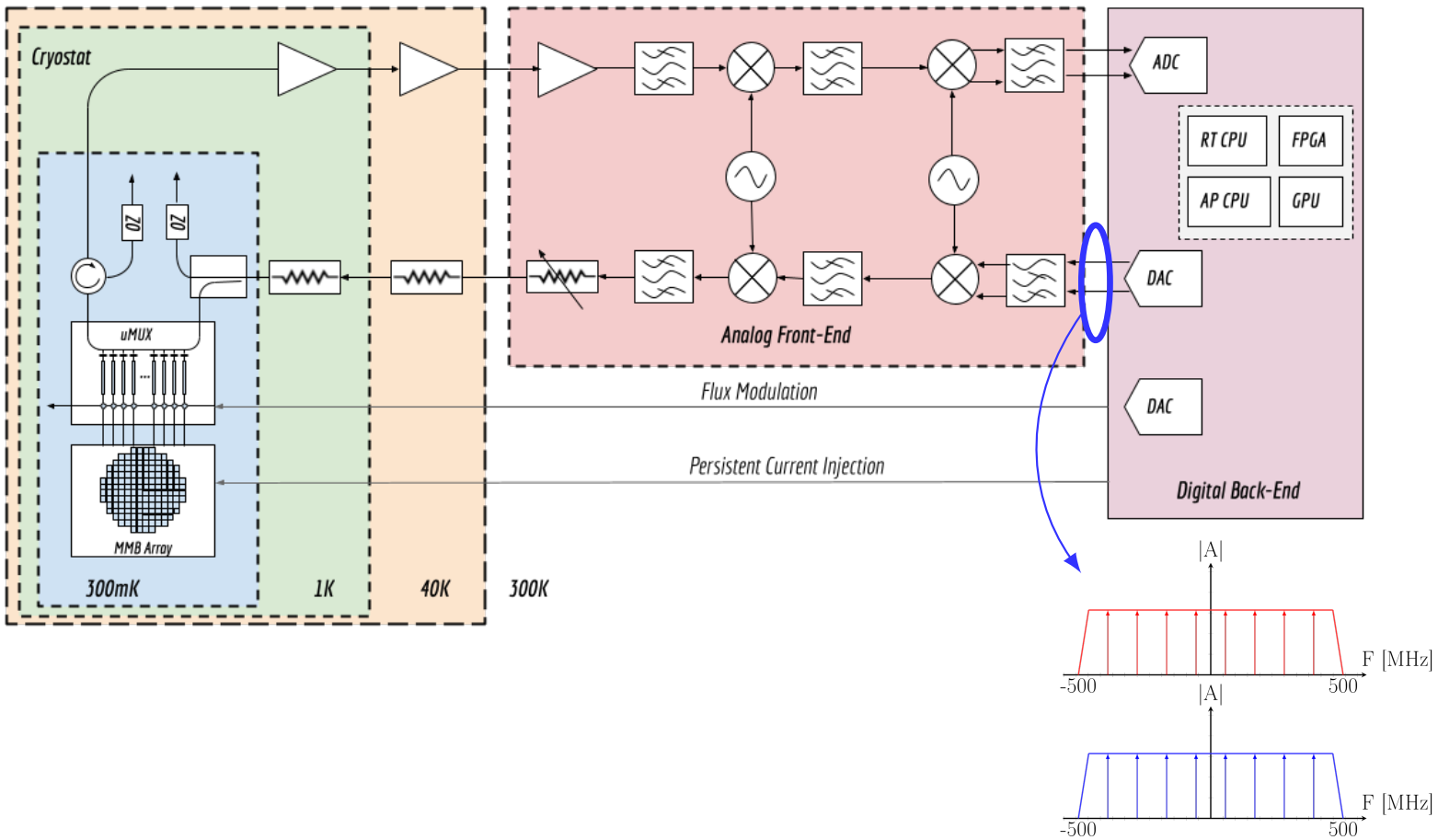
This thesis proposes a real-time processing backend for the read-out electronics of cryogenic particle detectors, aiming to process a high number of frequency tones for a FDM scheme ($\approx$ 1000). It's focused in the design and development of a high performance processing and high scalabity approach, minimizing the used resources.

Projects I'm involved

- QUBIC, for CMB observation (**ITeDA**),
- ECHo, neutrino mass determination (**IPE**)

The Read-Out System


Cryostat
ADC
RT CPU
FPGA
AP CPU
GPU
DAC
DAC
Analog Front-End
Flux Modulation
Persistent Current Injection
Digital Back-End
uMUX
MMB Array
300mK
1K
40K
300K


Cryostat
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300mK
1K
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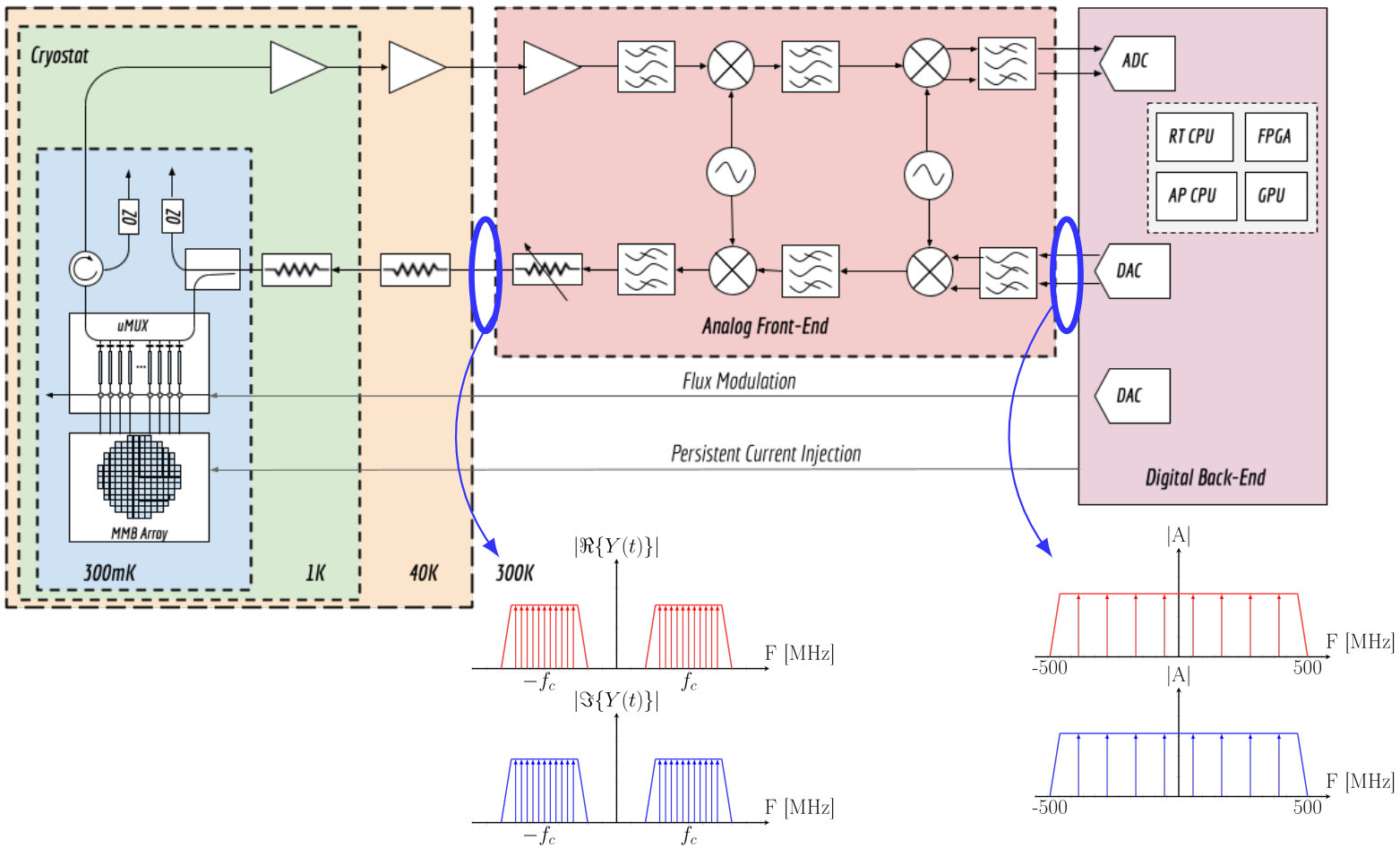
300K
Analog Front-End
ADC
RT CPU
FPGA
AP CPU
GPU
DAC
DAC
Digital Back-End
Flux Modulation
Persistent Current Injection
|A|
F [MHz]
-500
500
|A|
F [MHz]
-500
500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$|\Re\{Y(t)\}|$
F [MHz]
$-f_c$
f_c
$|\Im\{Y(t)\}|$
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F [MHz]
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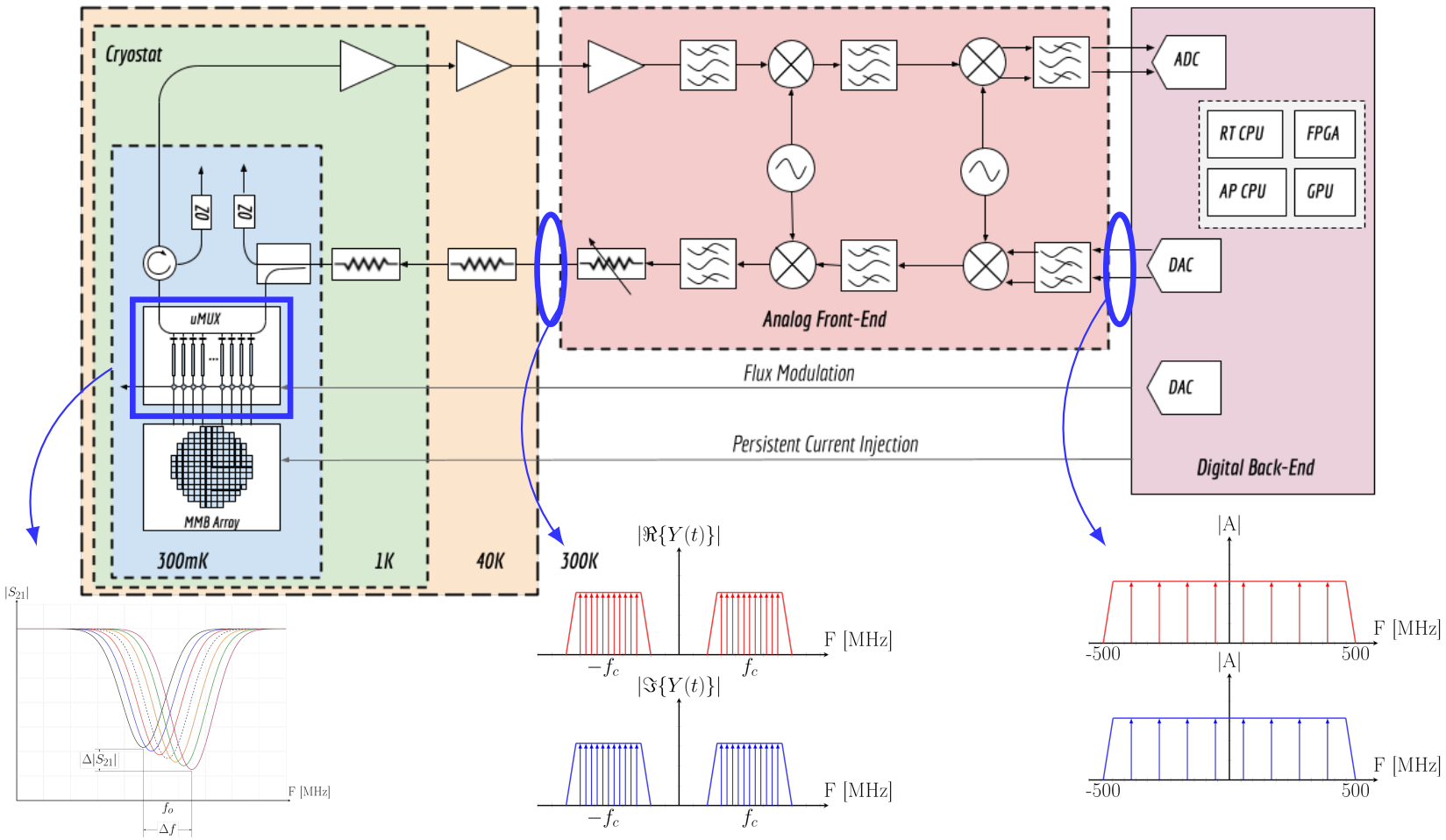
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AP CPU
GPU
DAC
DAC
Flux Modulation
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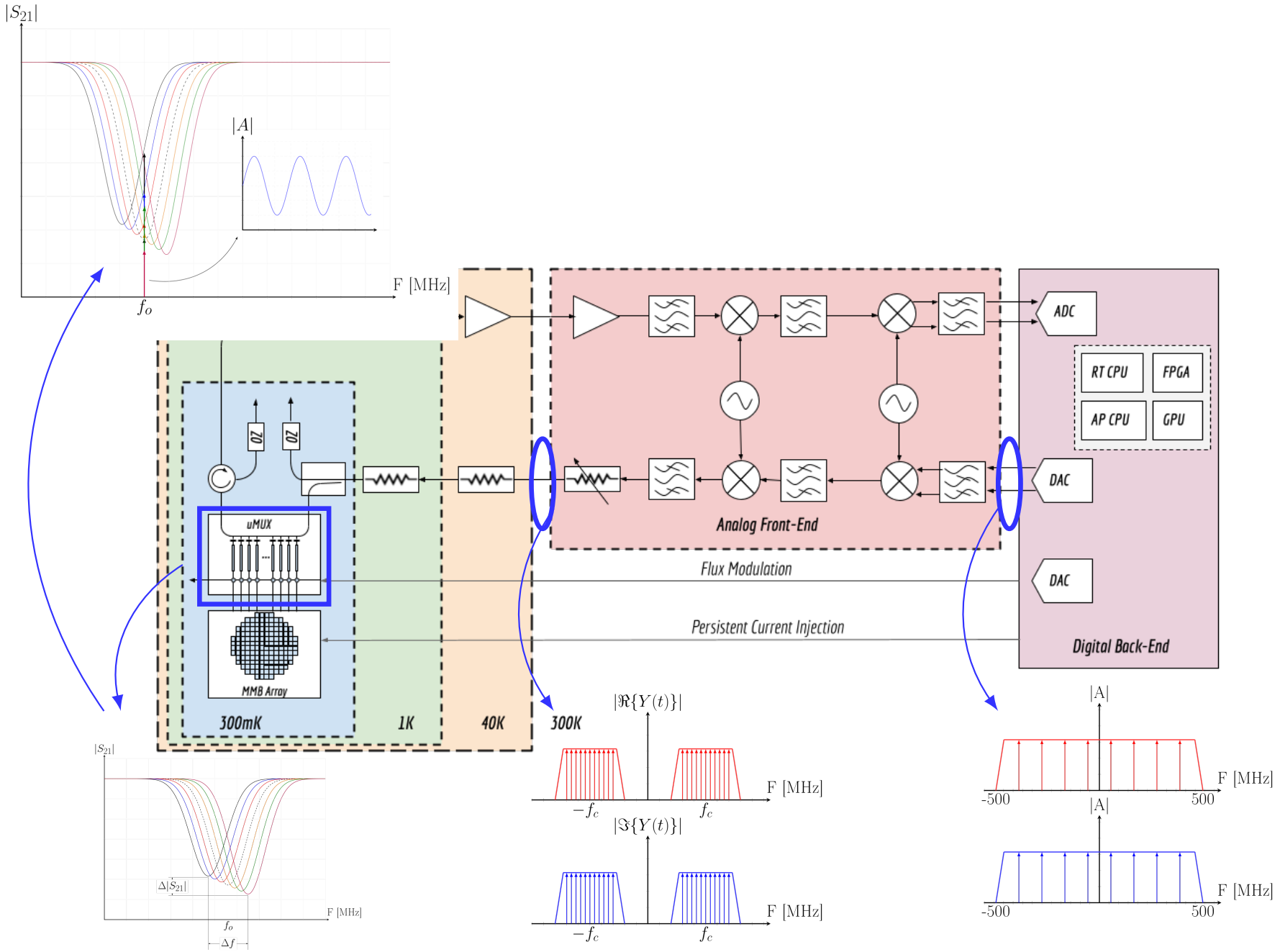
Digital Back-End
$|S_{21}|$
$\Delta|S_{21}|$
F [MHz]
f_o
Δf
$|\Re\{Y(t)\}|$
F [MHz]
$-f_c$
f_c
$|\Im\{Y(t)\}|$
F [MHz]
$-f_c$
f_c
|A|
F [MHz]
-500
500
|A|
F [MHz]
-500
500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$|A|$
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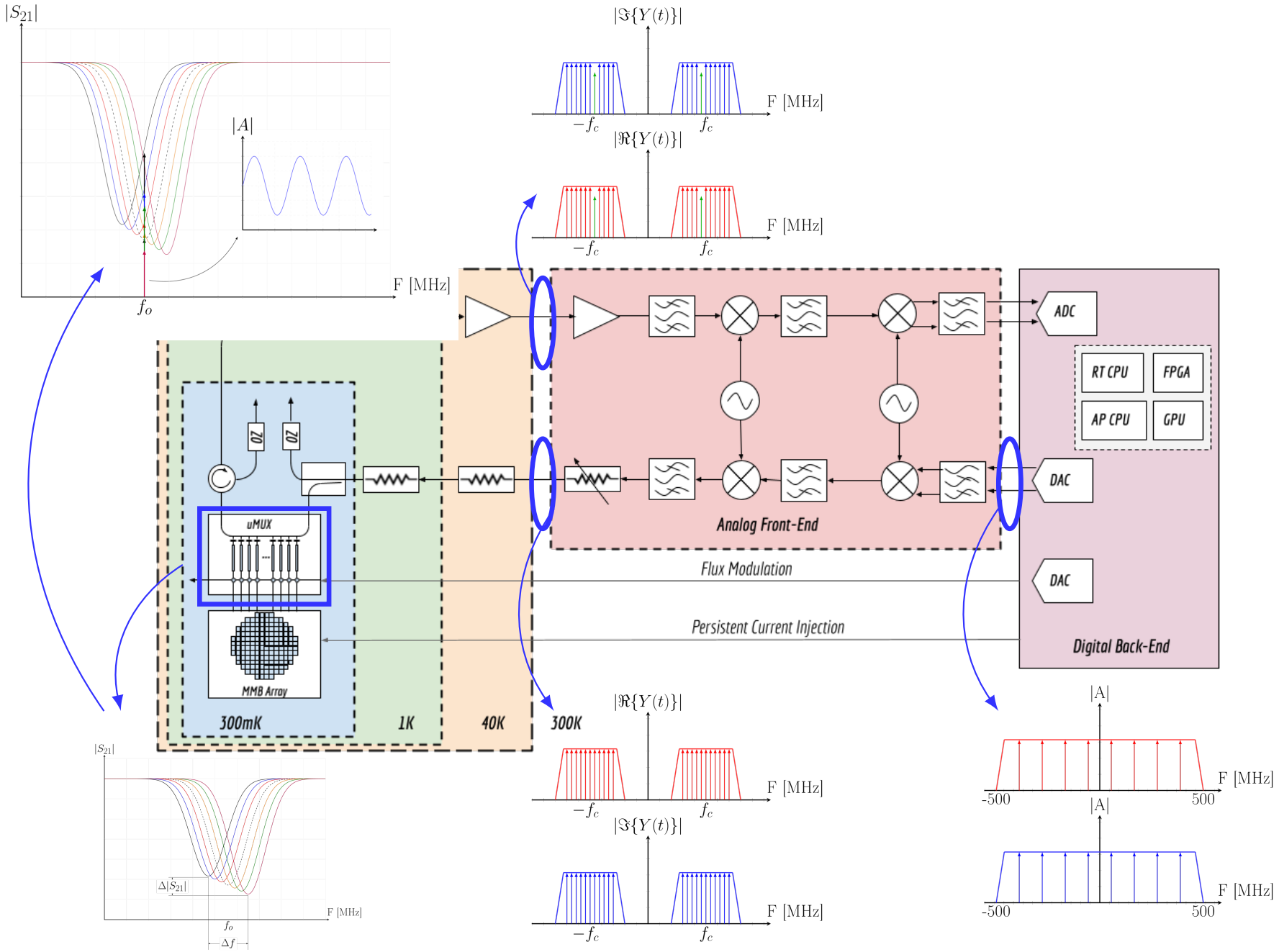
$\Delta|S_{21}|$
Δf
-500
500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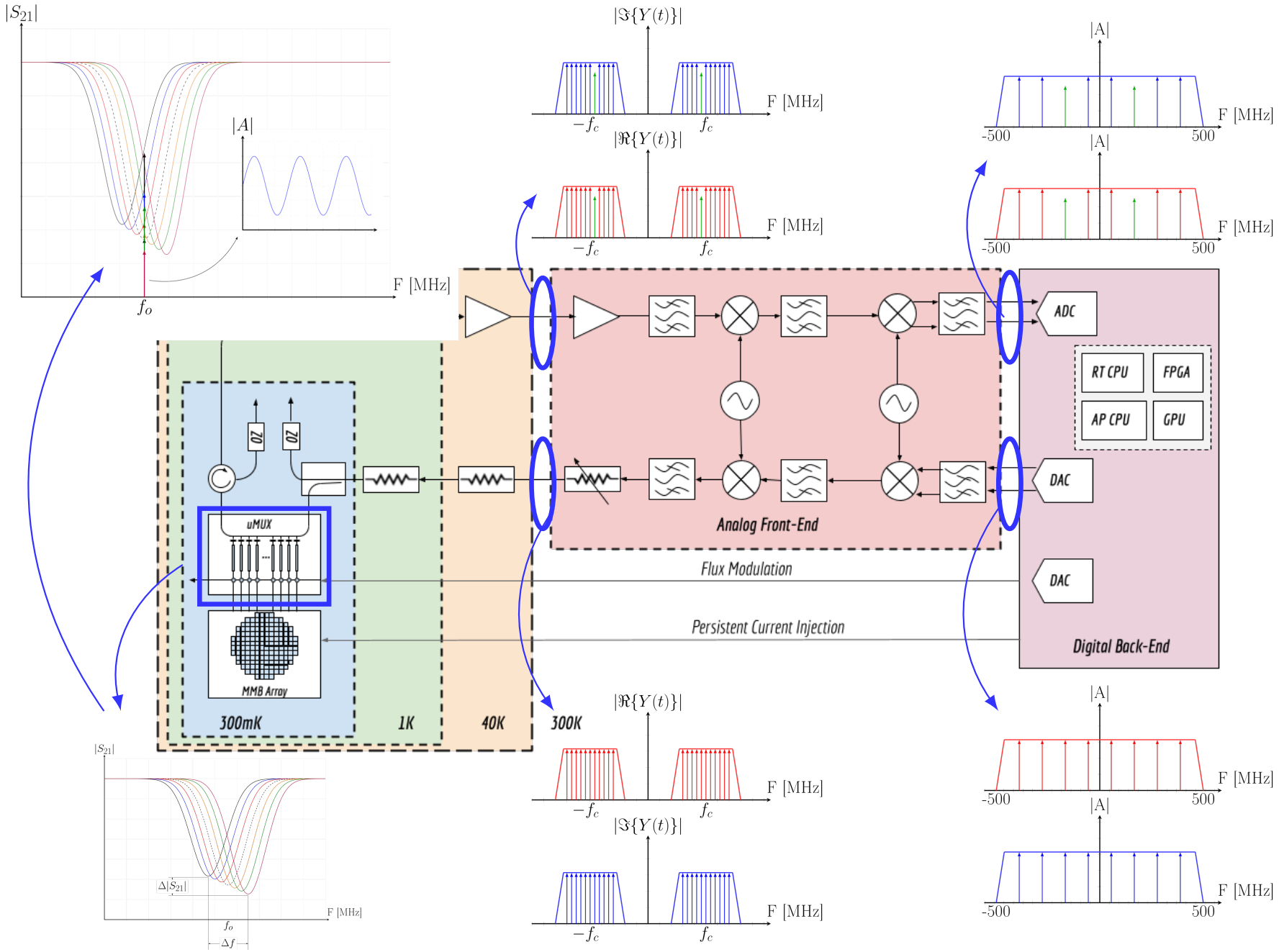
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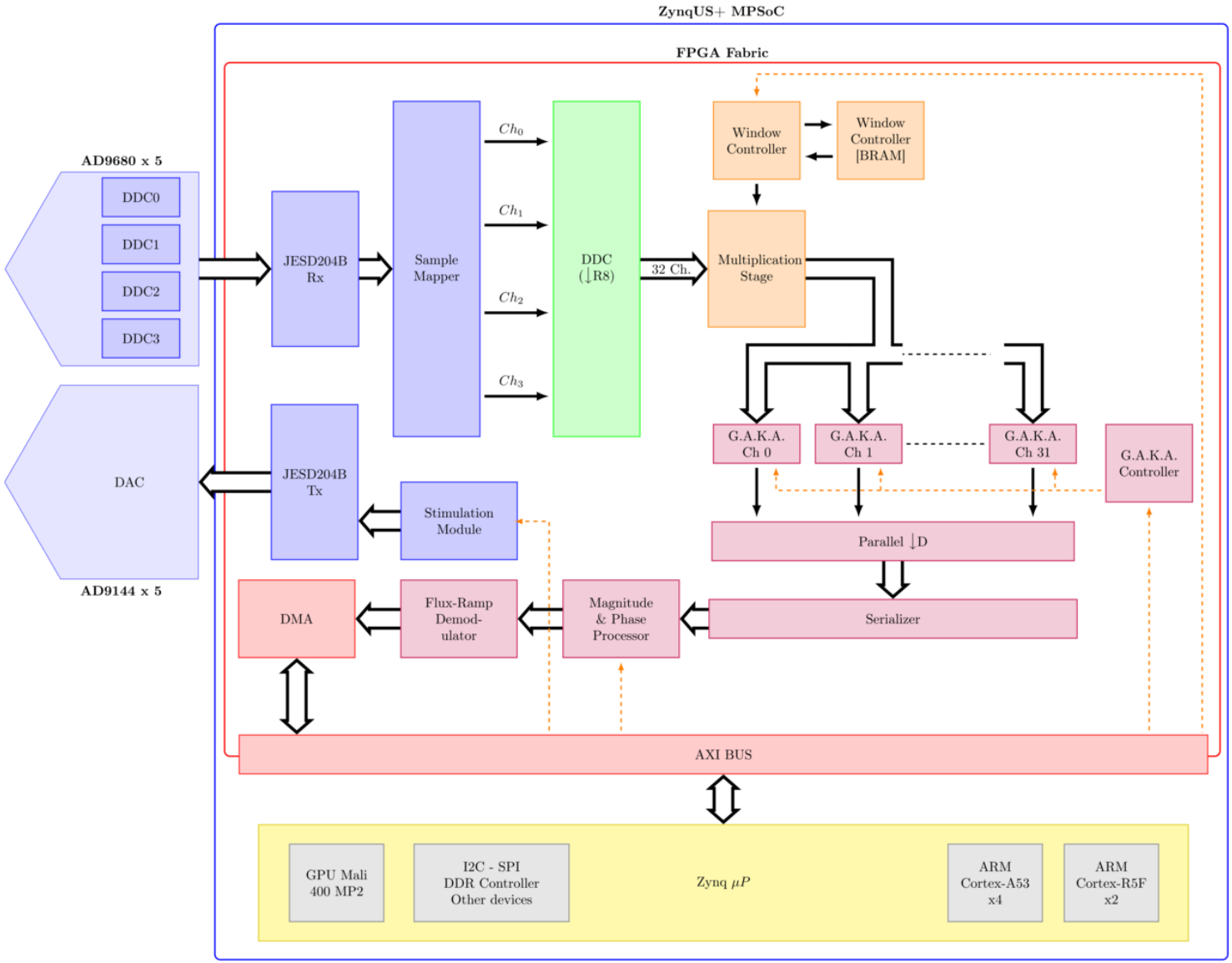
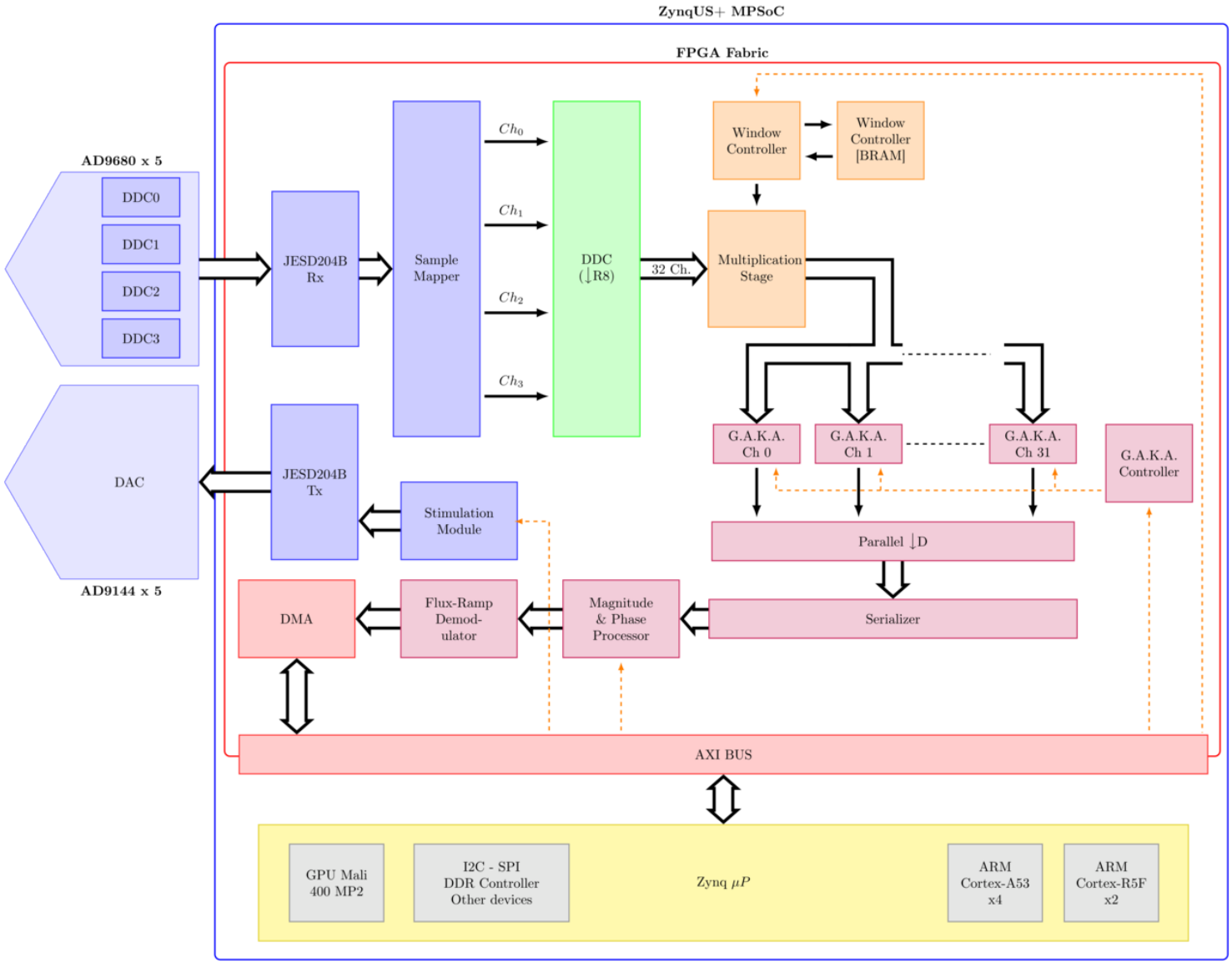
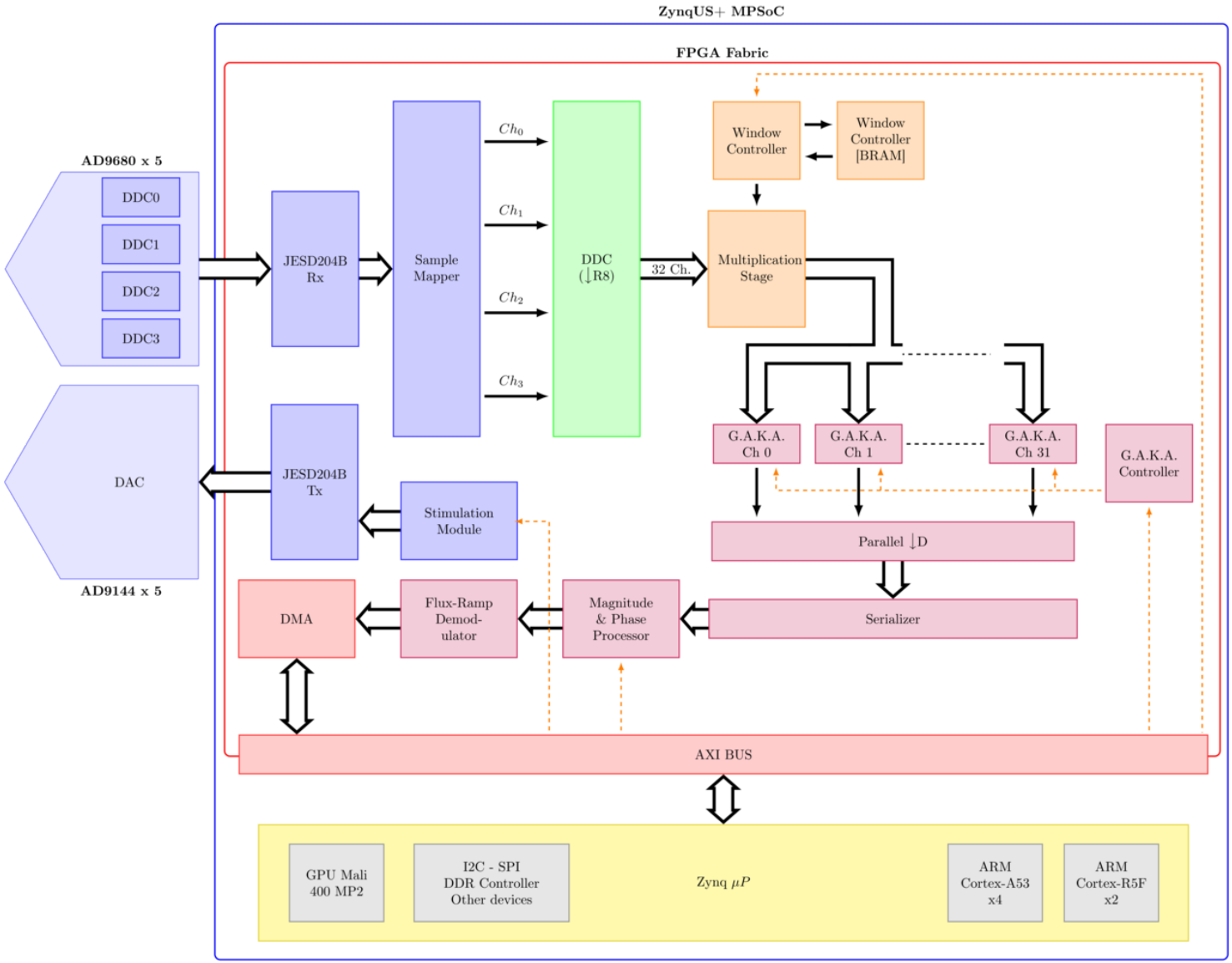

ZynqUS+ MPSoC
FPGA Fabric
AD9680 x 5
DDC0
DDC1
DDC2
DDC3
DAC
AD9144 x 5
JESD204B Rx
JESD204B Tx
Sample Mapper
Ch_0
Ch_1
Ch_2
Ch_3
DDC (↓R8)
32 Ch.
Window Controller
Window Controller [BRAM]
Multiplication Stage
G.A.K.A. Ch 0
G.A.K.A. Ch 1
G.A.K.A. Ch 31
G.A.K.A. Controller
Parallel ↓D
Serializer
Magnitude & Phase Processor
Flux-Ramp Demod-ulator
Stimulation Module
DMA
AXI BUS
GPU Mali 400 MP2
I2C - SPI DDR Controller Other devices
Zynq μP
ARM Cortex-A53 x4
ARM Cortex-R5F x2

- Process 1024 sensors per focal plane,



- Process 1024 sensors per focal plane,
- RF bandwidth: 4 GHz (from 4GHz to 8 GHz),



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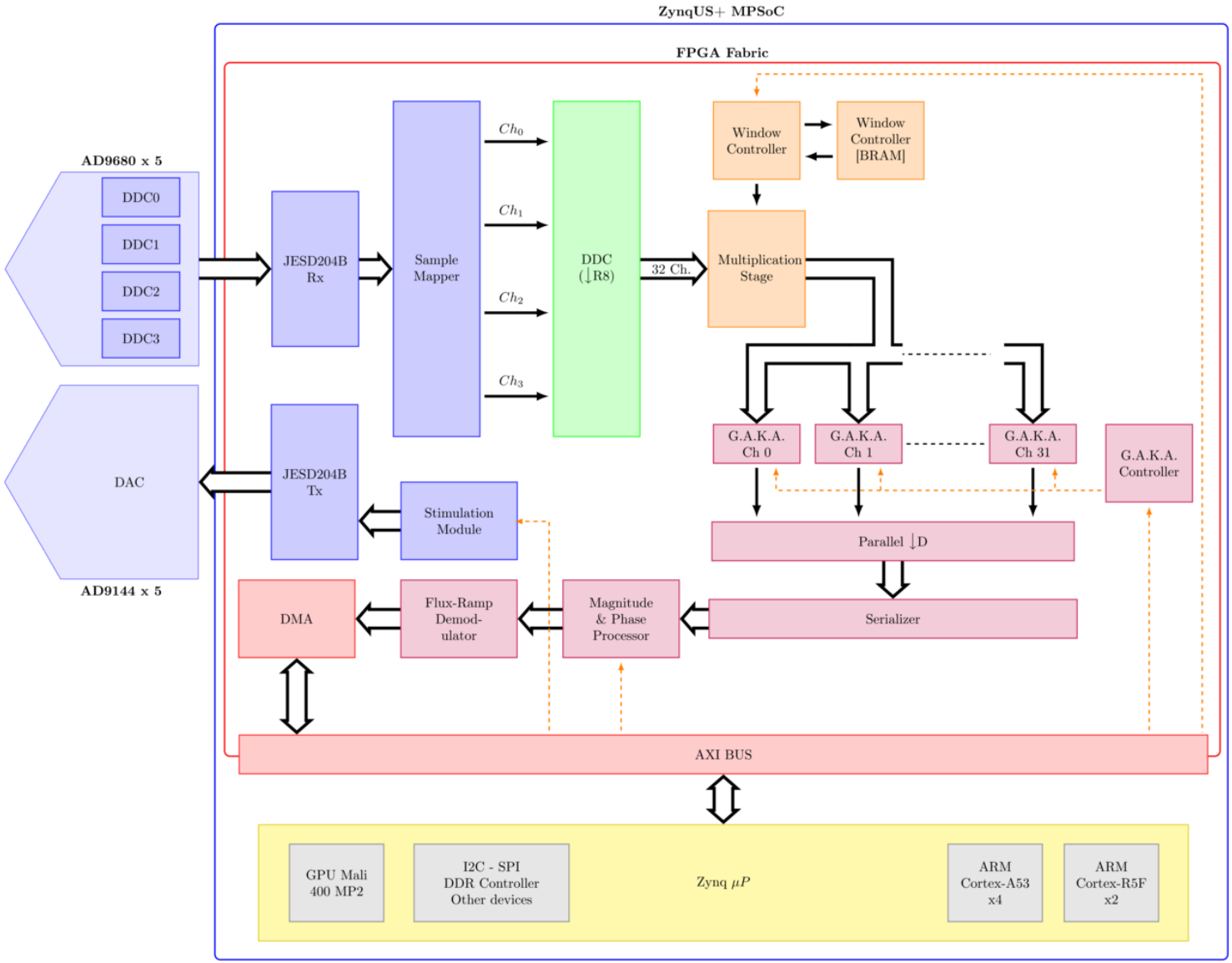
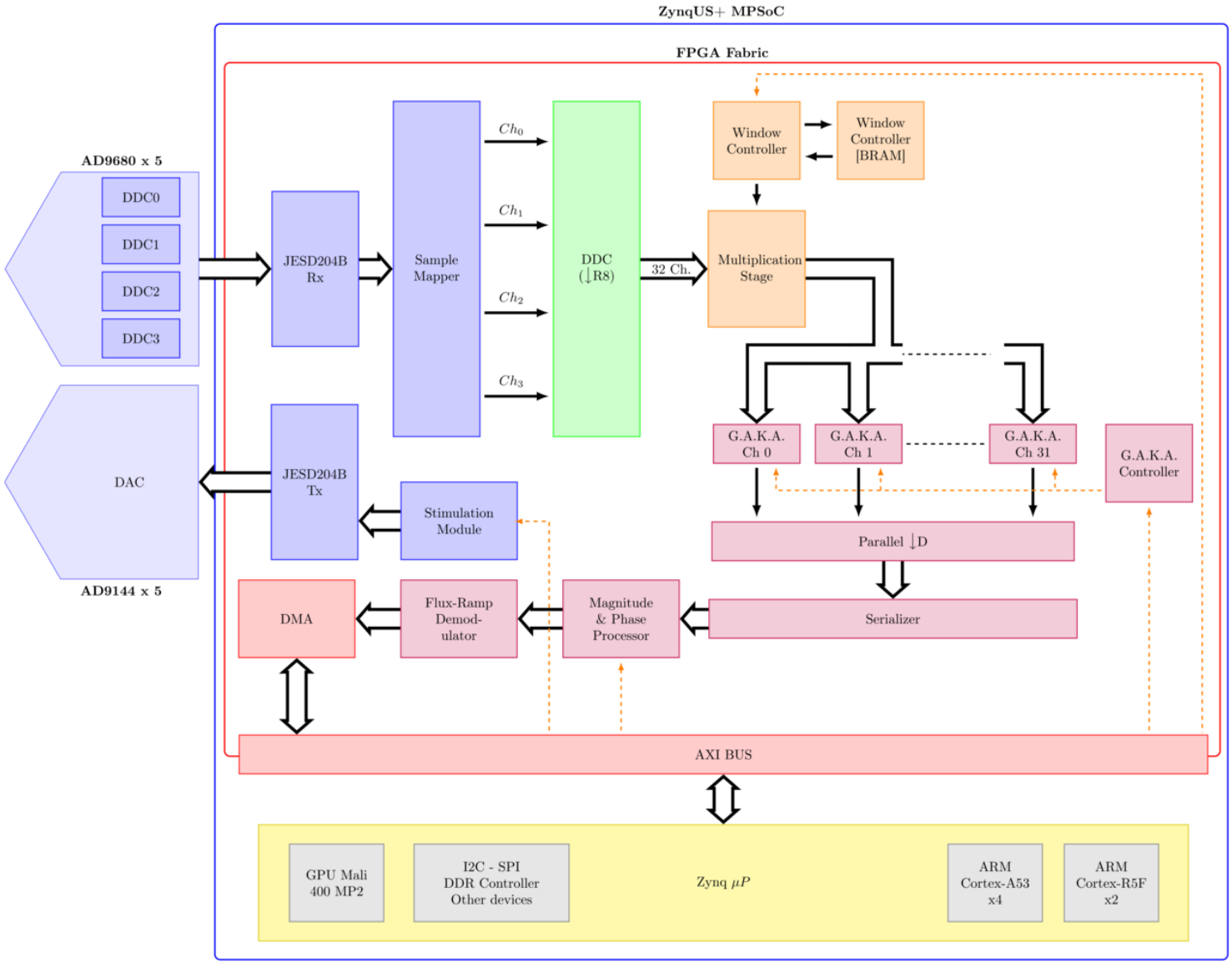
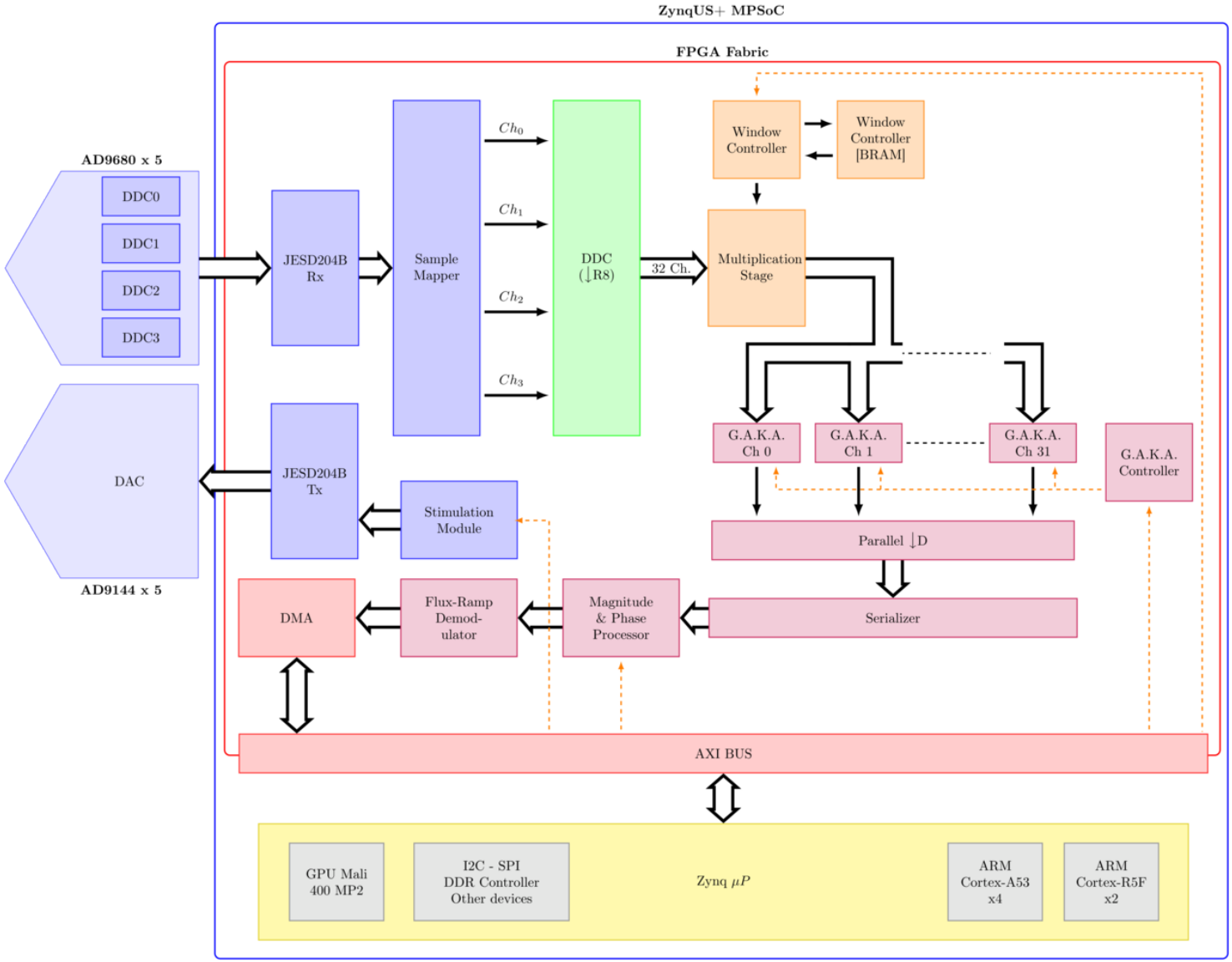


- Process 1024 sensors per focal plane,
- RF bandwidth: 4 GHz (from 4GHz to 8 GHz),
- Baseband bandwidth: 4 GHz (from $\approx$ 0 Hz to 4 GHz),
- ADC effective BW: 800 MHz.

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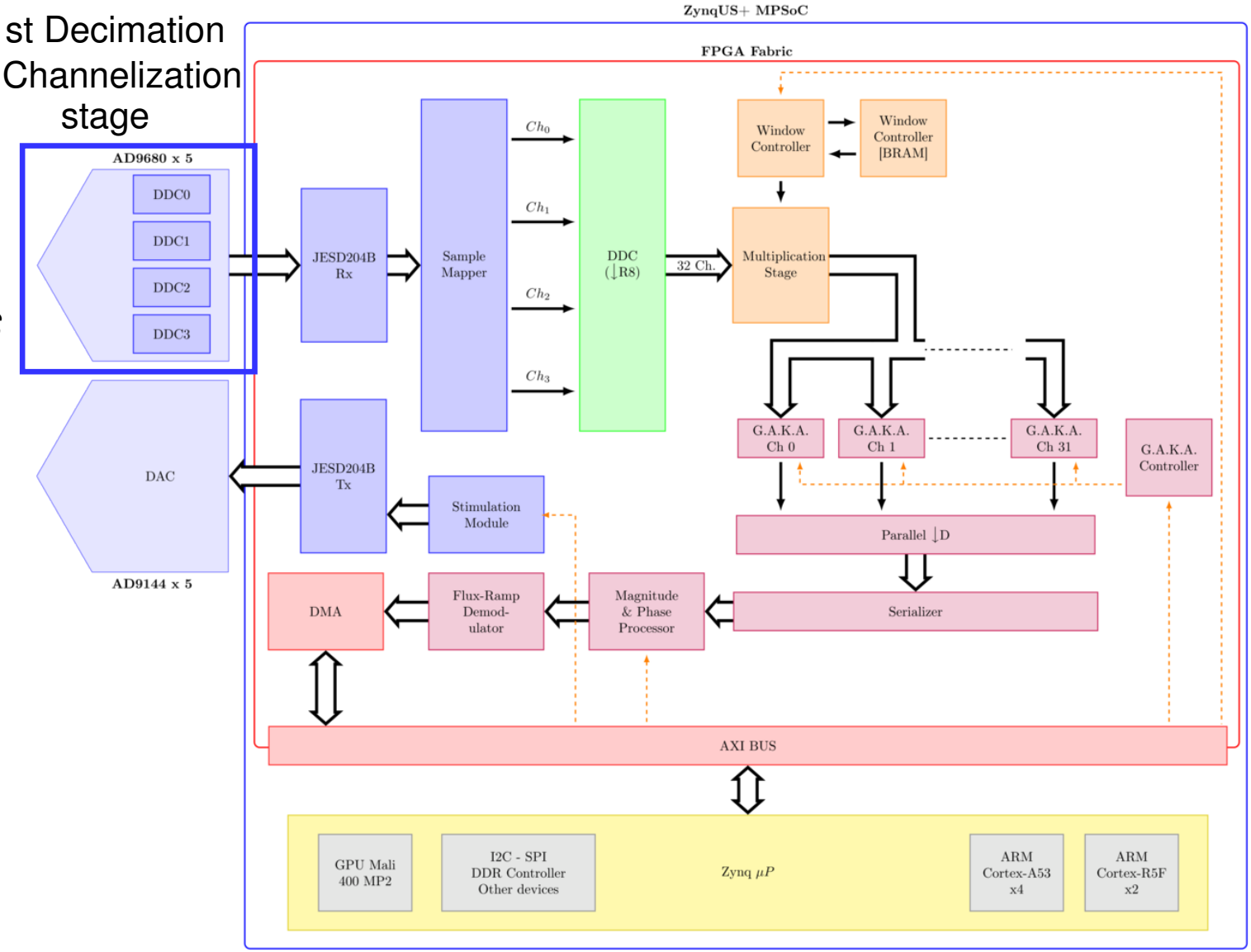
I2C - SPI DDR Controller Other devices
Zynq μP
ARM Cortex-A53 x4
ARM Cortex-R5F x2

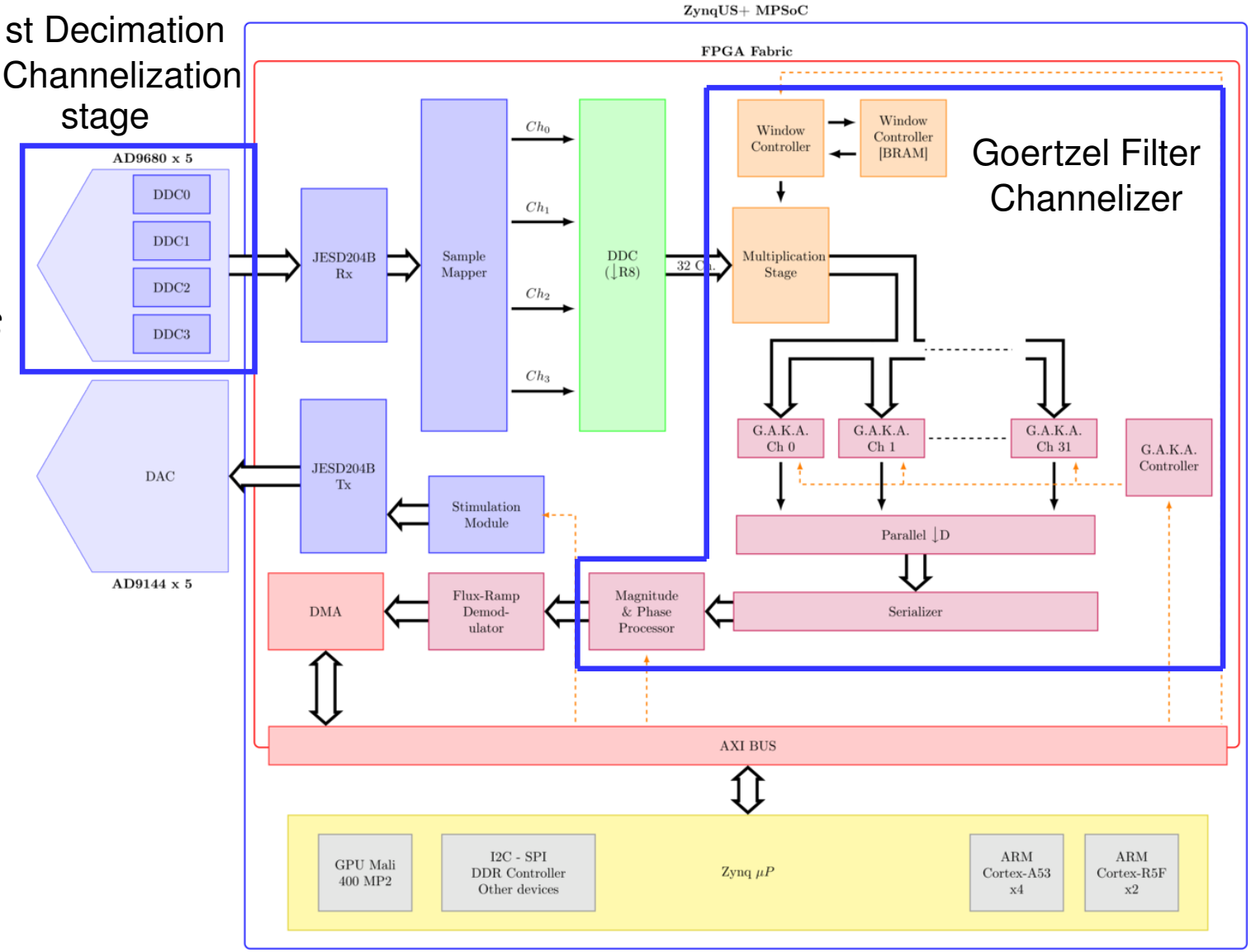
4 Ch.
$Fs = 250MSPS$

1st Decimation & Channelization stage



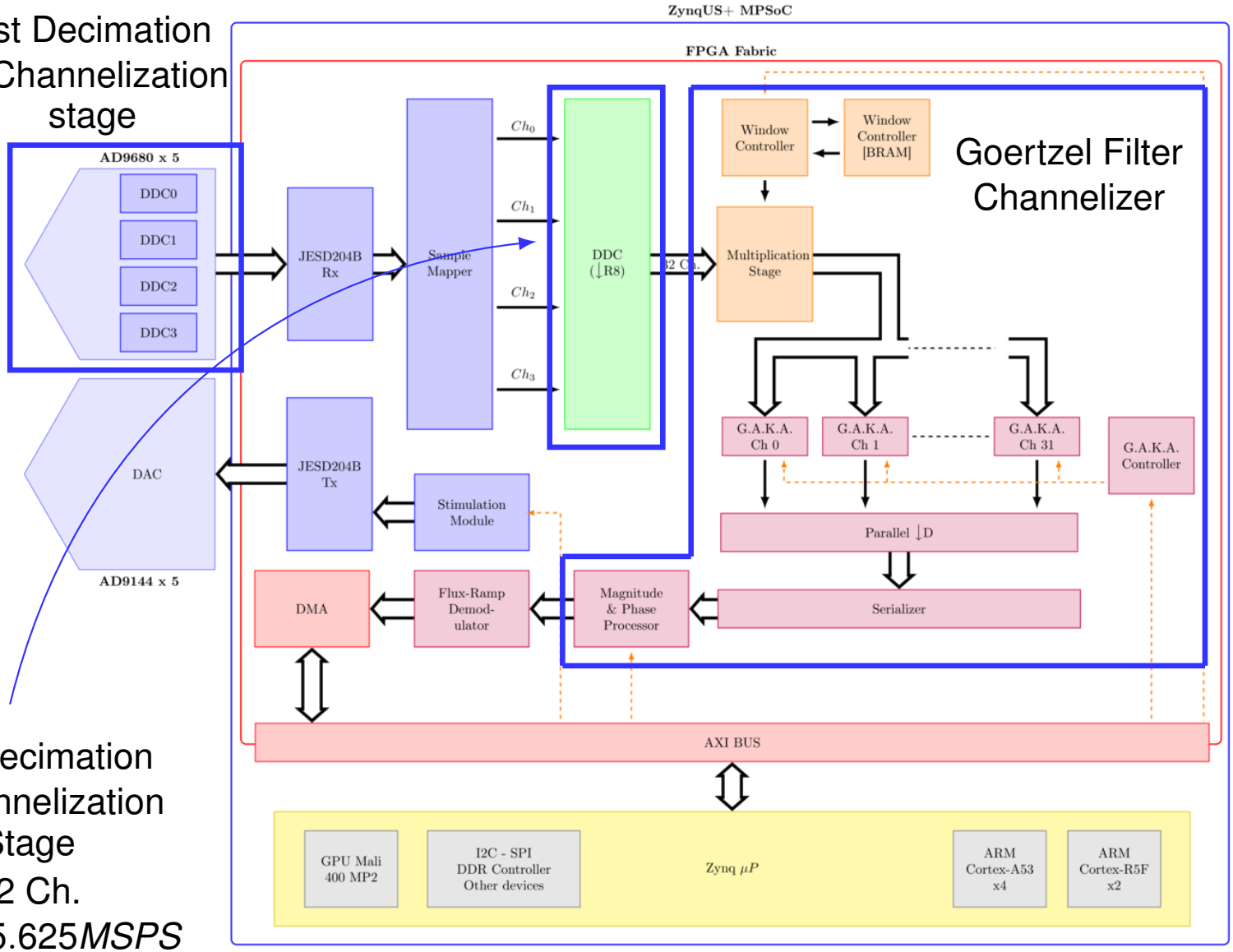
4 Ch.
$Fs = 250MSPS$

1st Decimation & Channelization stage

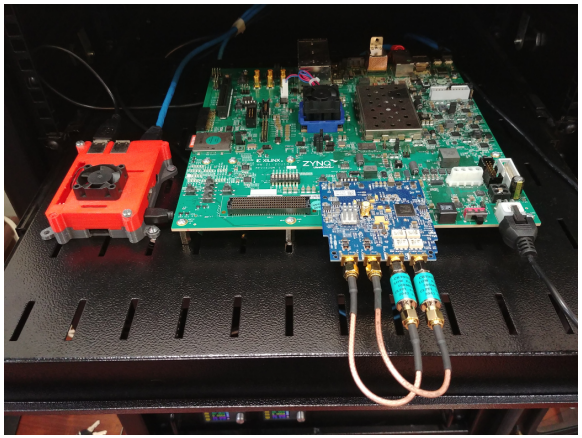


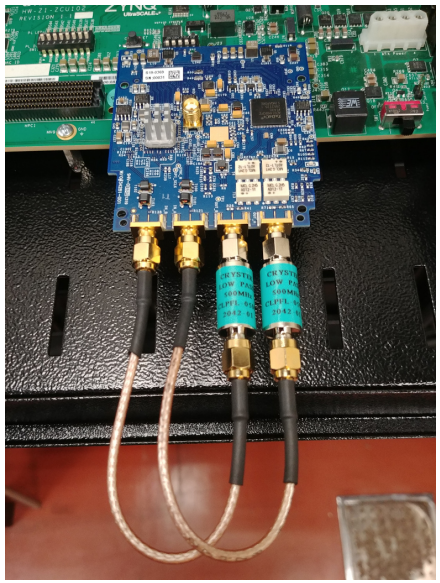
1st Decimation & Channelization stage

4 Ch.
$Fs = 250MSPS$



2nd Decimation & Channelization Stage
32 Ch.
$Fs = 15.625MSPS$





- Left top: Zynq UltraScale+ ZCU102 + RPi 3 + AD-FMCDAQ2-EBZ,
- Left bottom: AD-FMCDAQ2-EBZ (ADC: AD9680@1GSPS and DAC:AD9144@1GSPS),
- Right: setup for hardware testing.

IQ Generation Test

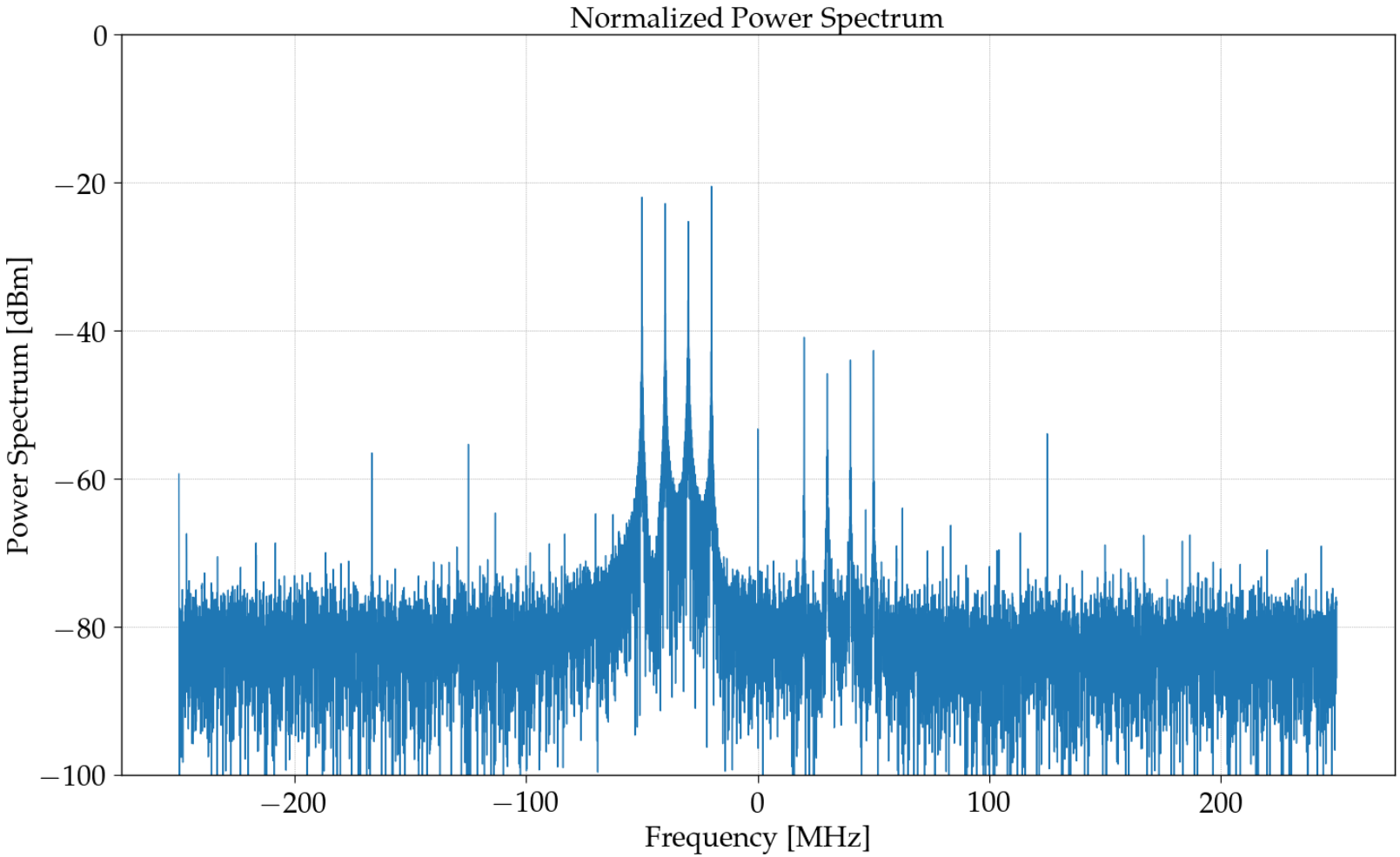


Figure: 4 IQ tones: $-20MHz, -30MHz, -40MHz$ and $-50MHz$

Future Work and related PhD tasks

Future work

- Validate the Direct Down Conversion stage,
- Finish the adjustments for compatibility between the new structure and the rest of the design,
- Merge everything and start with validation measurements for the whole design,
- Perform tests on a resonator emulator.

Language courses

- Deutsch A1.1 - **Approved**,
- Deutsch A1.2 - *In progress*.

KSETA Topical Courses - 1 course remaining

1. Observational Cosmology - March 2021 **(accredited)**,
2. Statistical methods in particle physics data analysis - March 2021 **(accredited)**,
3. Low-Temperature (Superconductive) Detectors - October 2021 **(done)**,
4. Introduction to quantum physics - October 2021 **(done)**,
5. Introduction to Machine Learning and Deep Learning - October 2021 **(done)**.

Obligations with UNSAM - 1 credit remaining

- 19 credits of the 19 requested:
  - Historical Introduction to Science's Philosophy ***[doesn't give credits]***,
  - Economics for Technologists ***[doesn't give credits]***,
  - Automatic Learning ***[4/4 given credits]***,
  - Statistics in Experimental Physics ***[5/5 given credits]***,
  - Astroparticles Physics ***[5/5 given credits]***,
  - Techniques in Particles Detection ***[5/5 given credits]***.

Presentations

- 7th Meeting Helmholtz Detectors Technology and Systems - February 2021.

References


J.-C. Hamilton, S. Torchinsky, *et al.*, "QUBIC I: Overview and Science Program,"

Vielen Dank!

Backup

Signal Generation

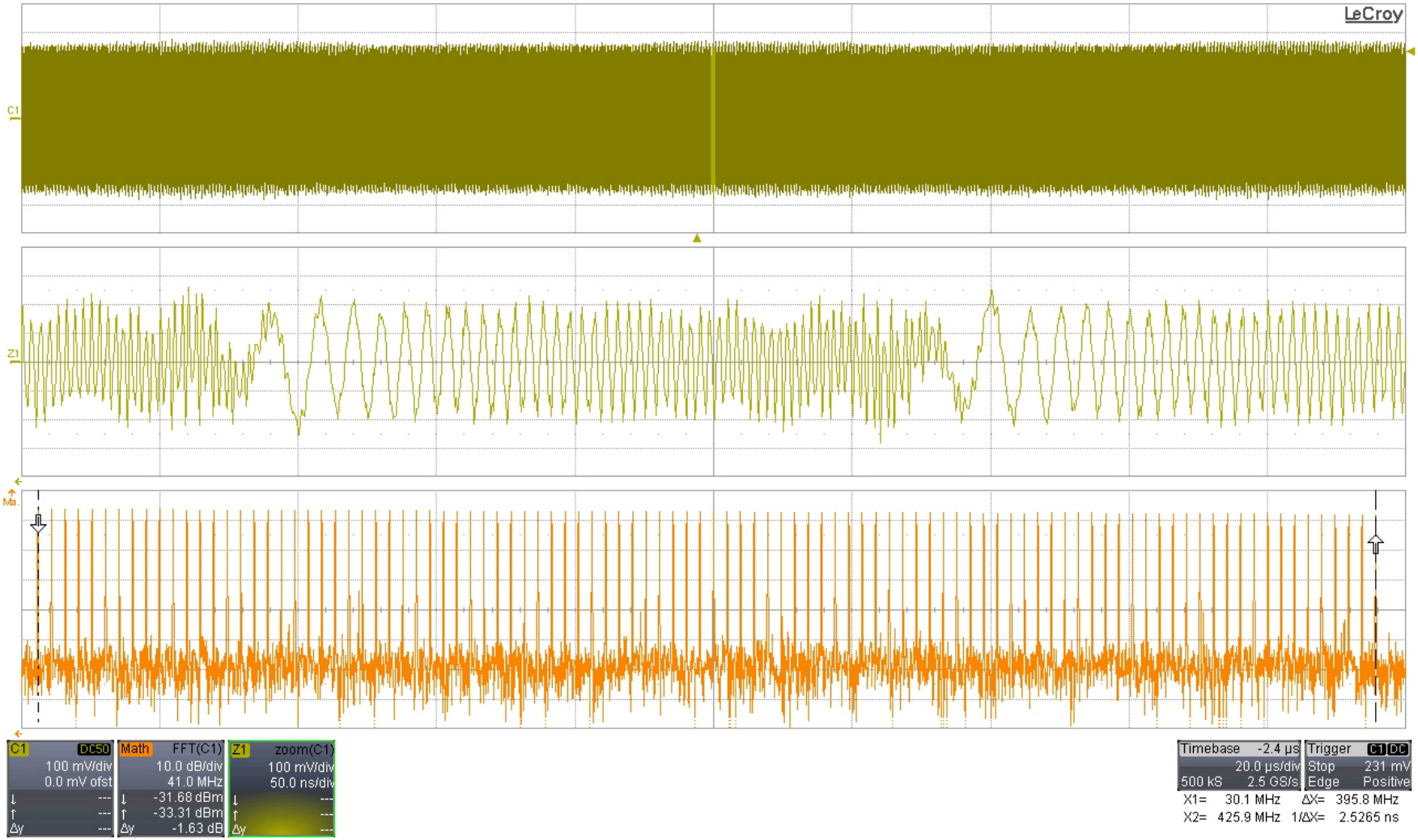
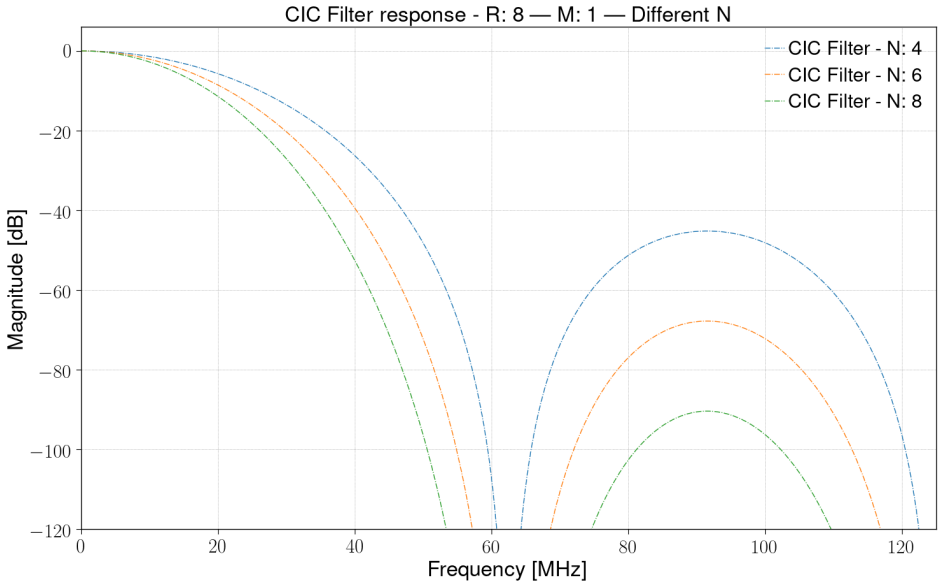
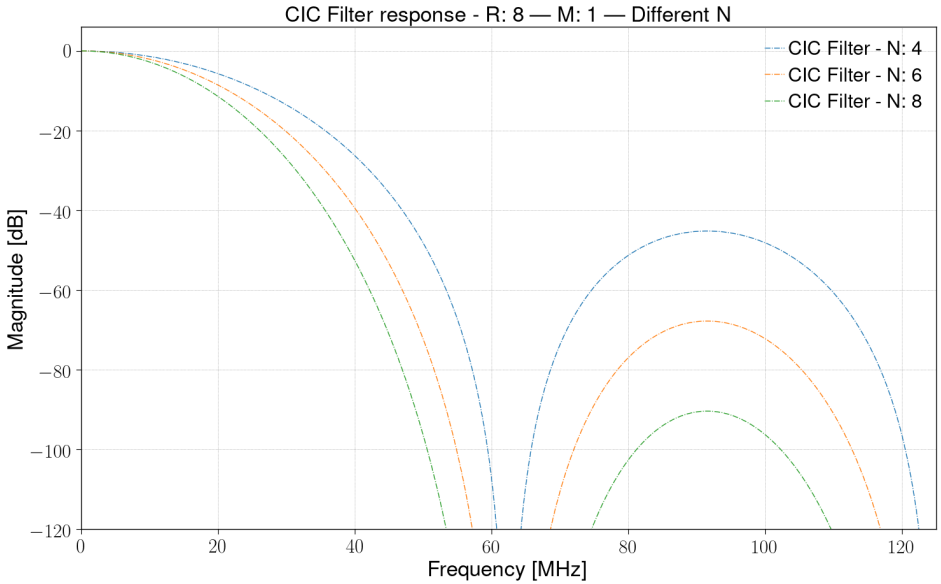


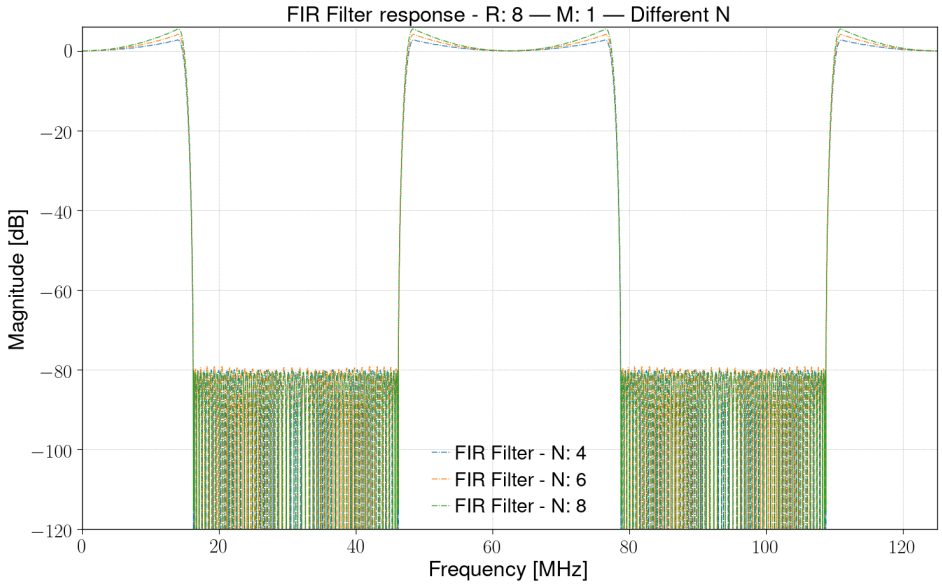
Figure: 100 Tones from 30 MHz to 426 MHz ($\Delta f = 4$ MHz)

Design Analysis

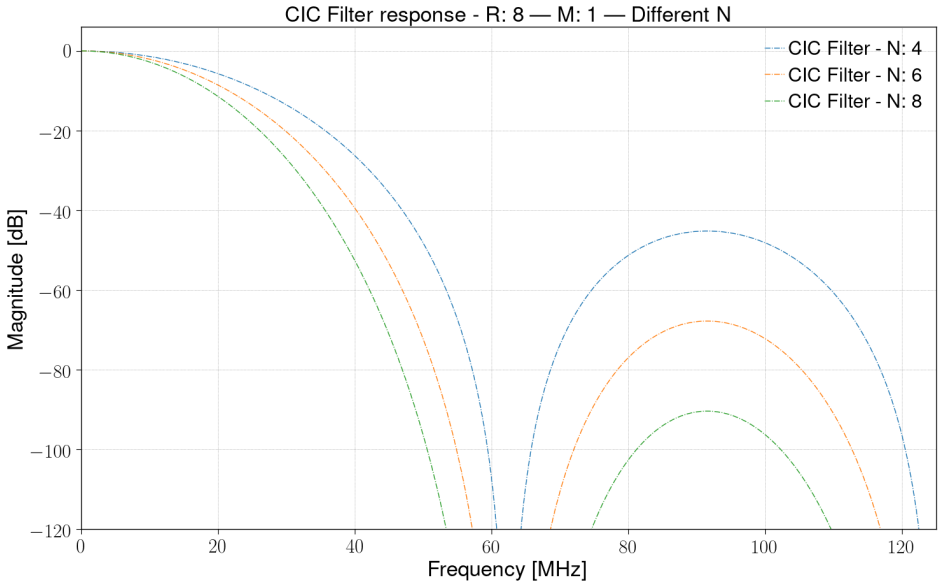


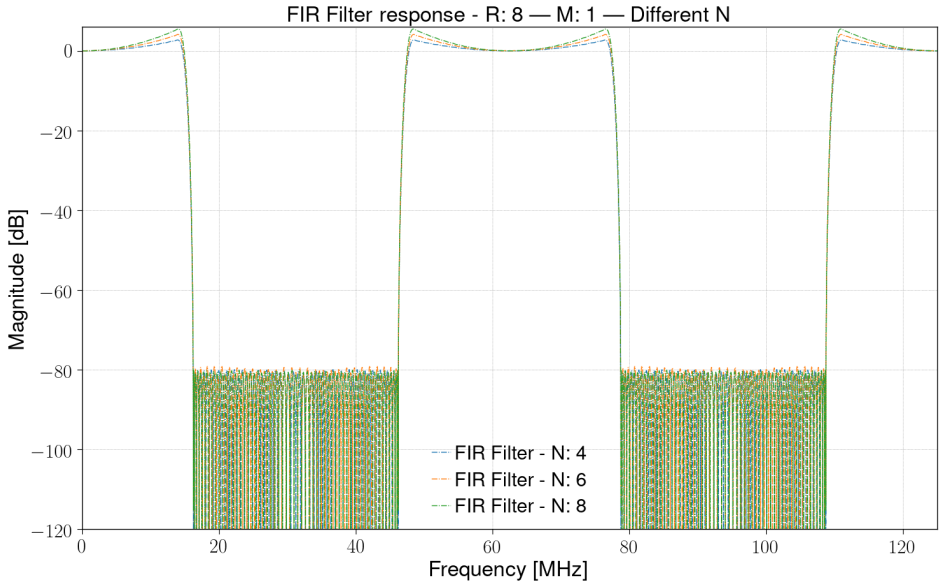
Design Analysis

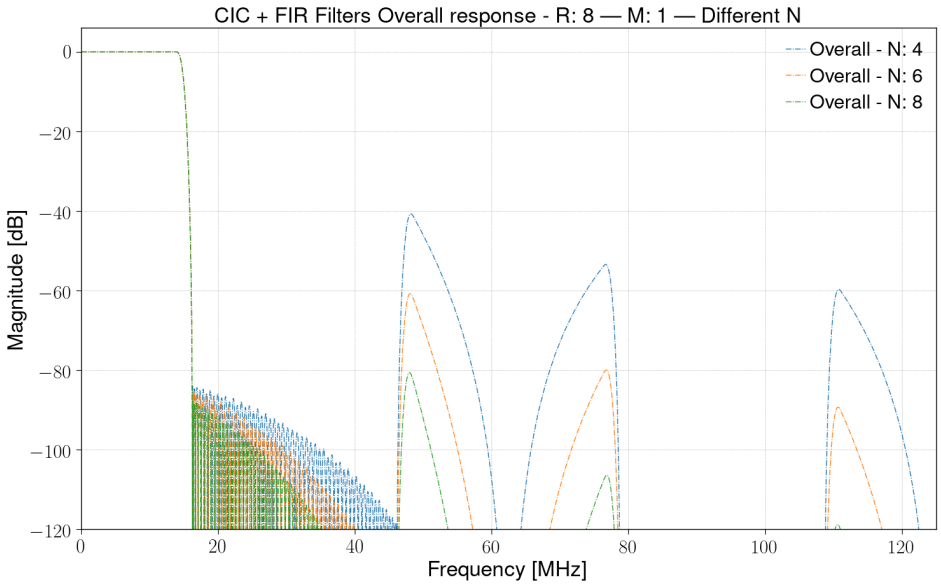


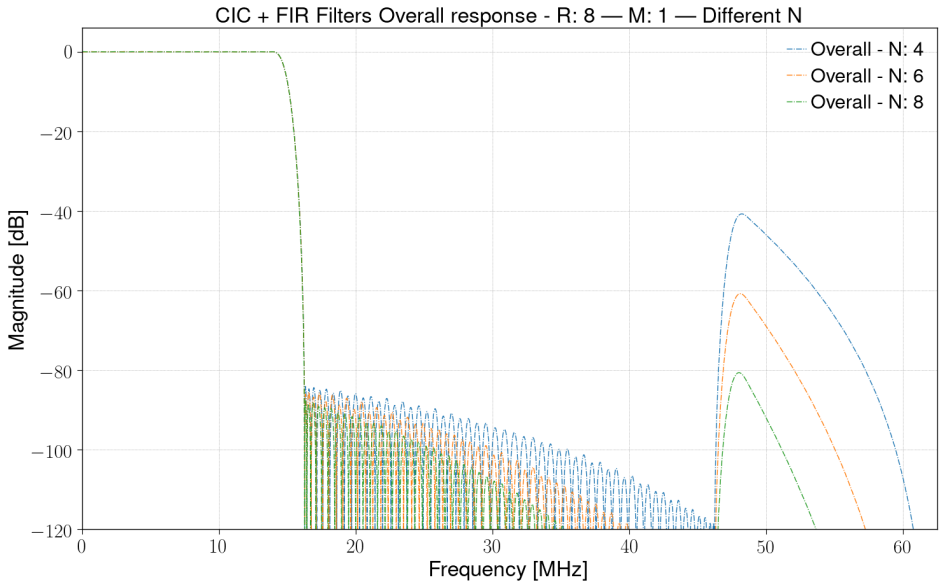


Design Analysis

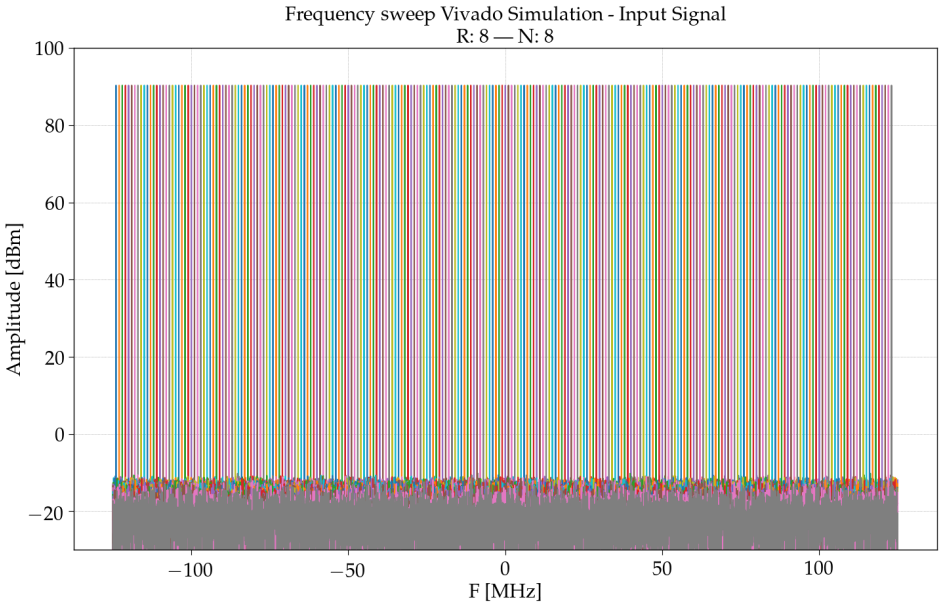




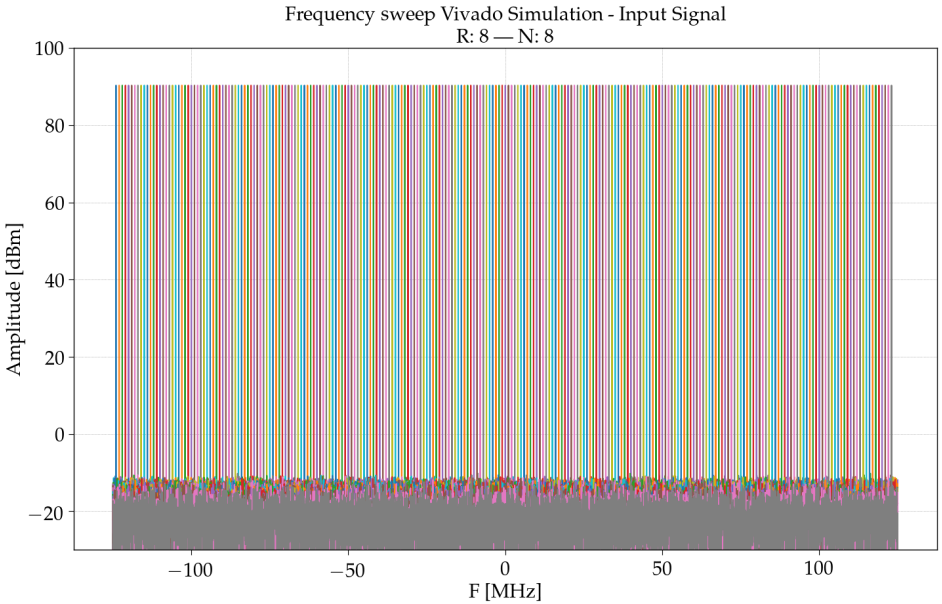


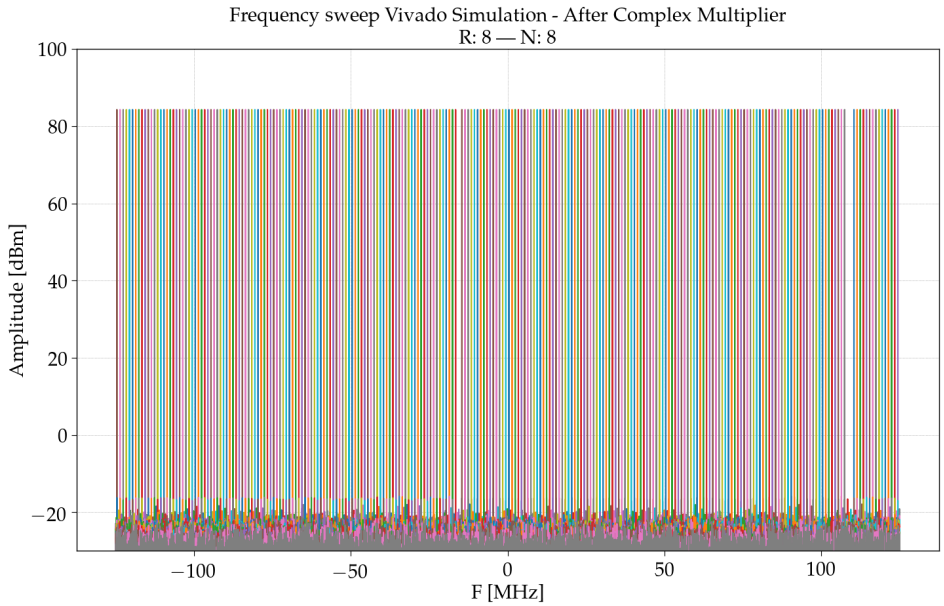


Vivado Simulation (HDL/RTL)

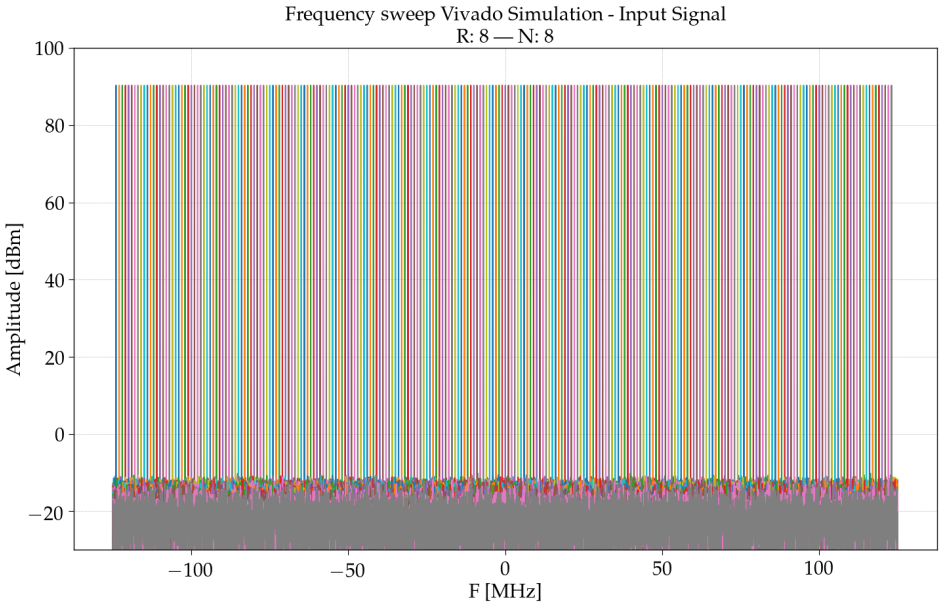


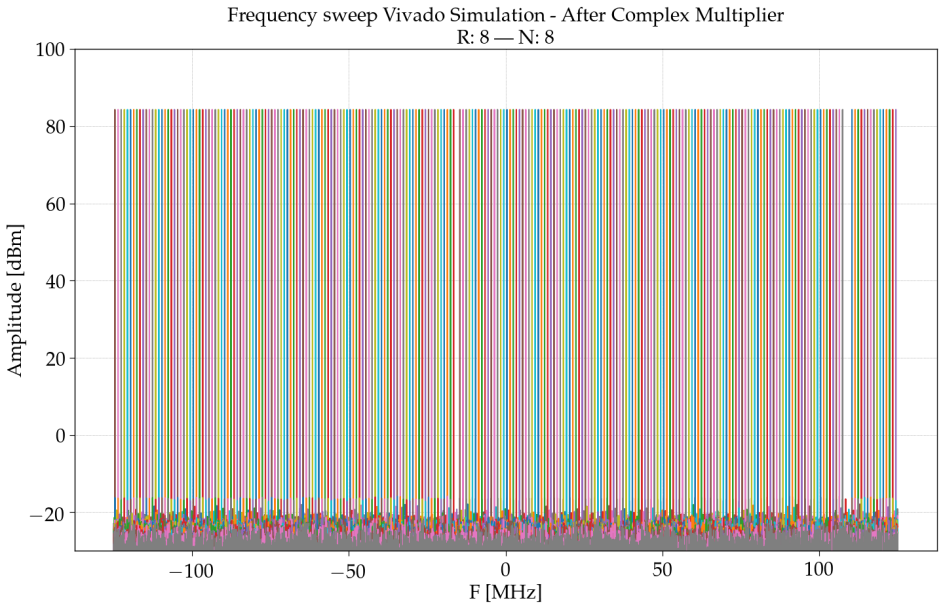
Vivado Simulation (HDL/RTL)

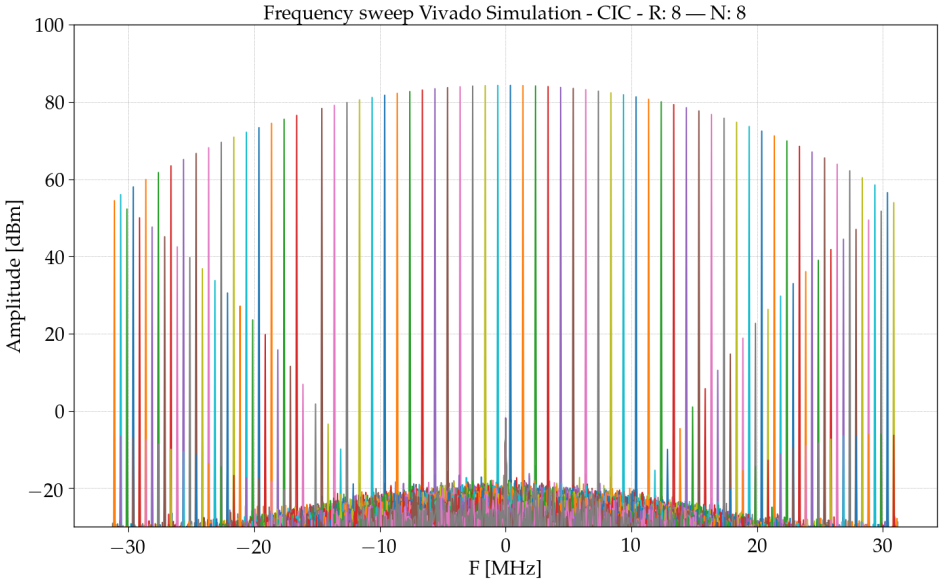




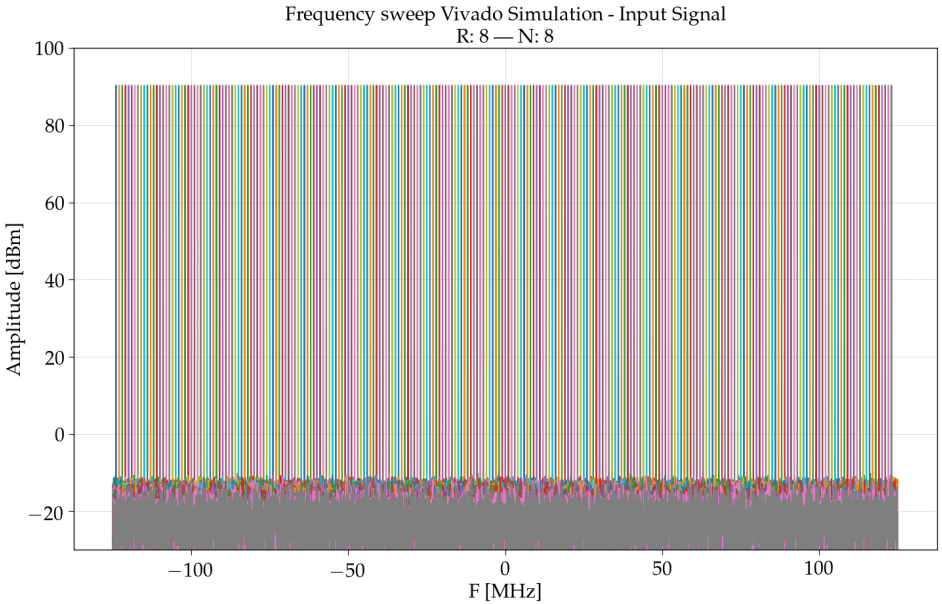
Vivado Simulation (HDL/RTL)

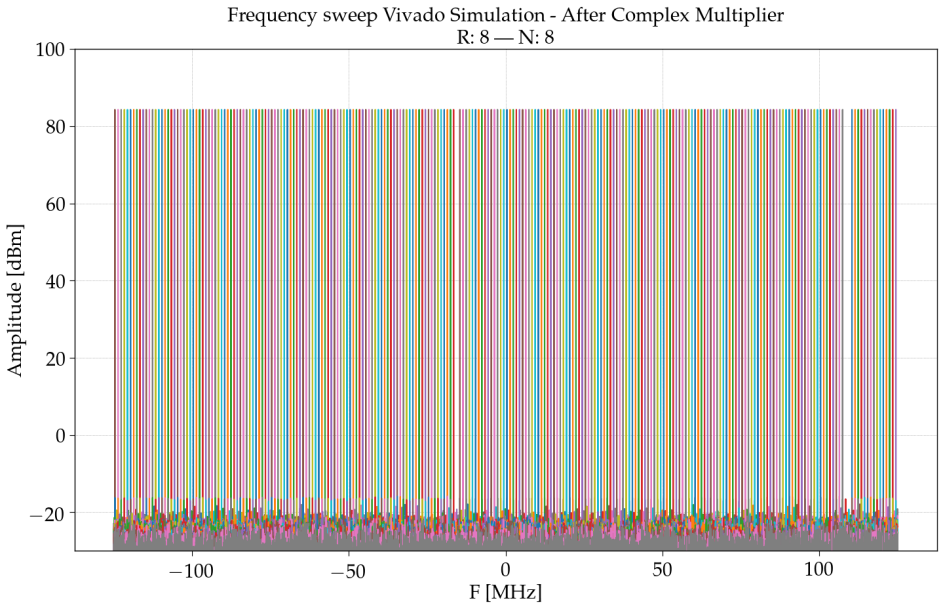


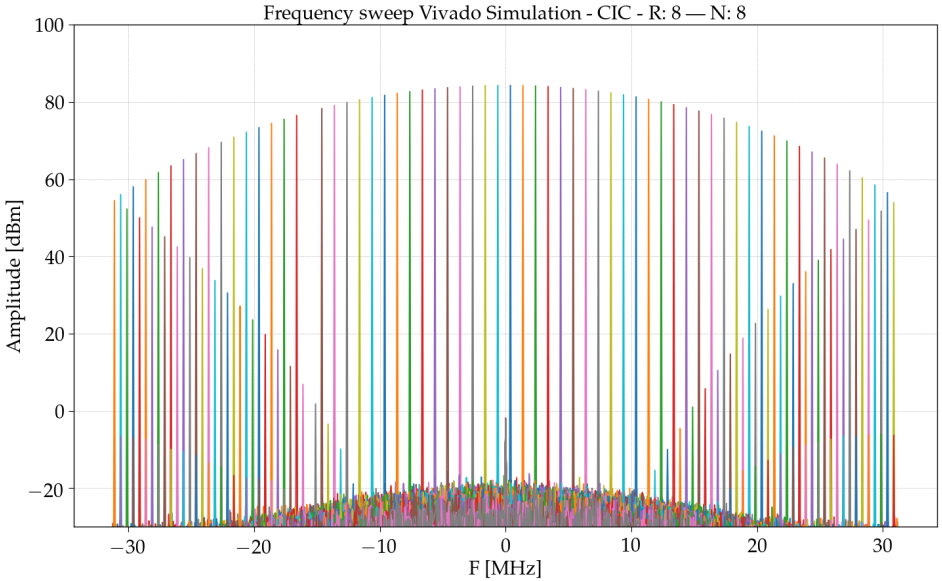


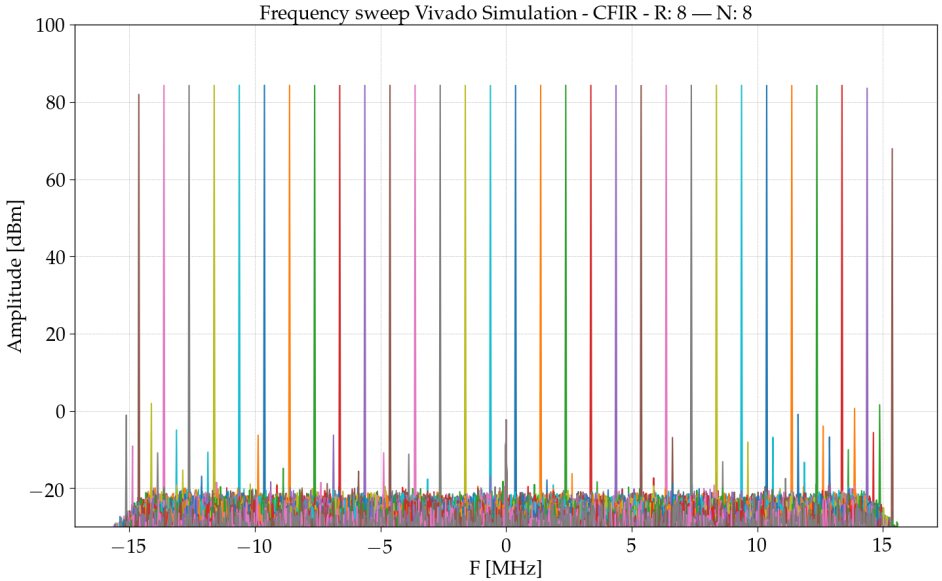


Vivado Simulation (HDL/RTL)









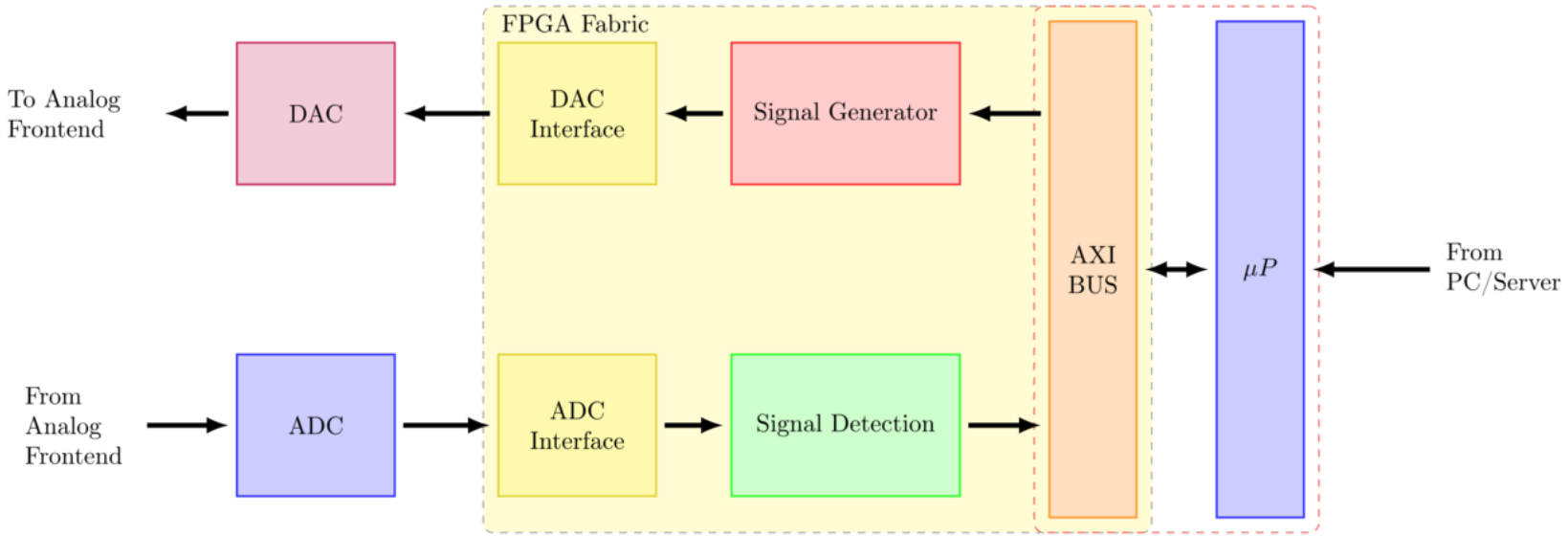


Figure: Firmware general block diagram

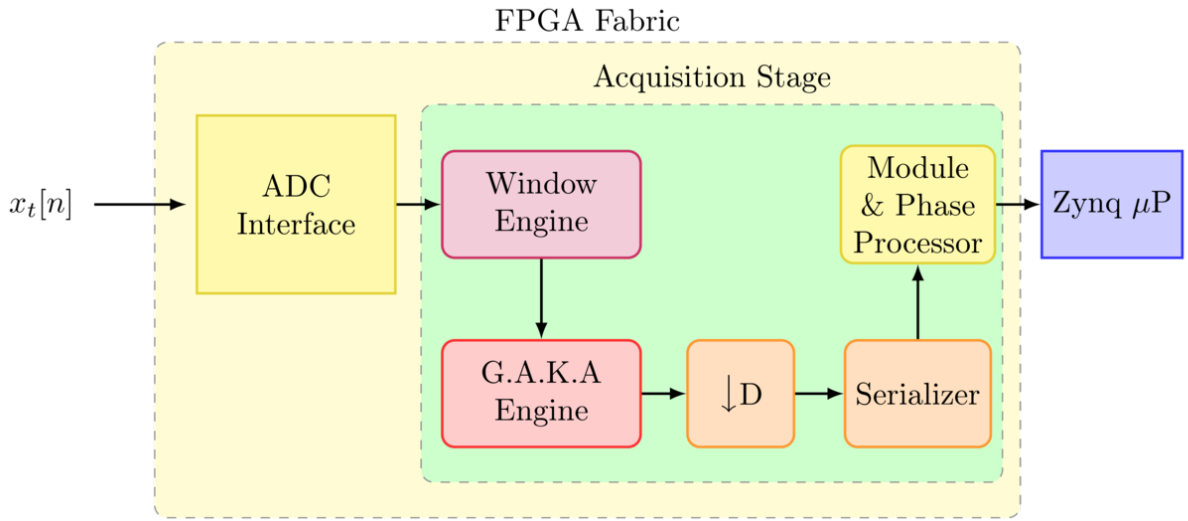


Figure: Old firmware *Signal Detection* block diagram

With this old firmware it was possible to:

- Implement only 100 filters (processing only 50 complex signals) ☹,
- Trying to increase the number of filters led to timing closure issues (not implementable design) ☹,
- The used resources per filter weren't scaling very well in this scenario ☹.

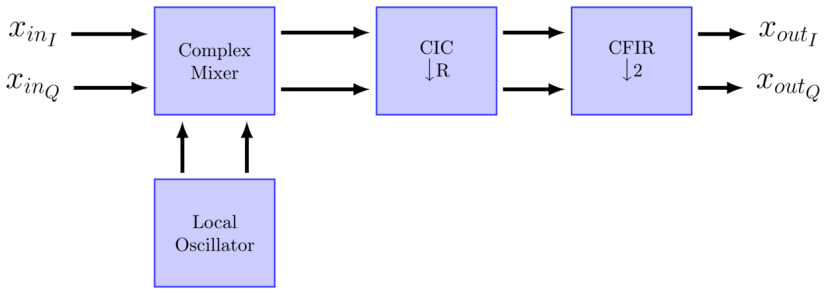


Figure: Basic block diagram of a DDC for complex signals

$$x_{in}(t) = x_{in_I}(t) + jx_{in_Q}(t),$$
$$x_{osc}(t) = \cos(2\pi f_{osc}t) \pm j\sin(2\pi f_{osc}t),$$
$$x_{out}(t) = x_{in}(t) \cdot x_{osc}(t)$$

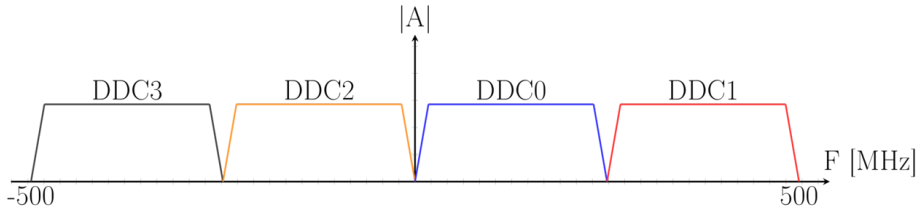


Figure: ADC Channelization - 1st Decimation stage

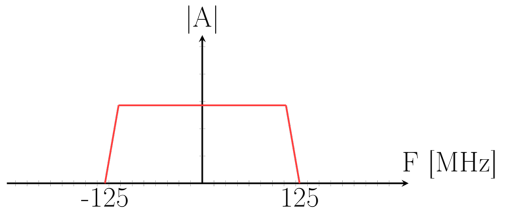


Figure: ADC digital ouput spectrum - $F_s = 250$ MSPS

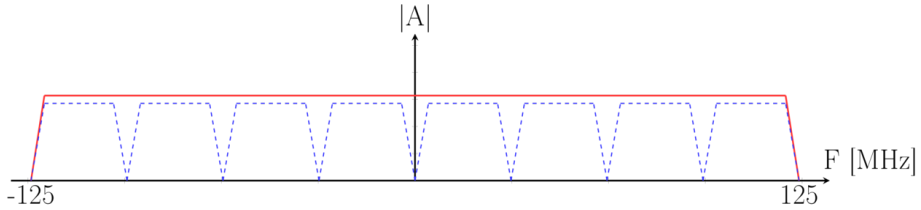


Figure: New DDC stage - 2nd Decimation stage (R = 8)

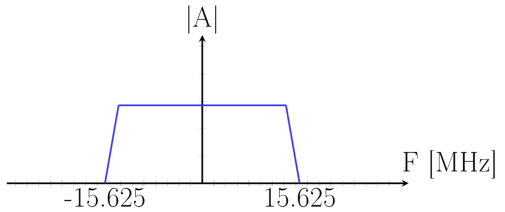
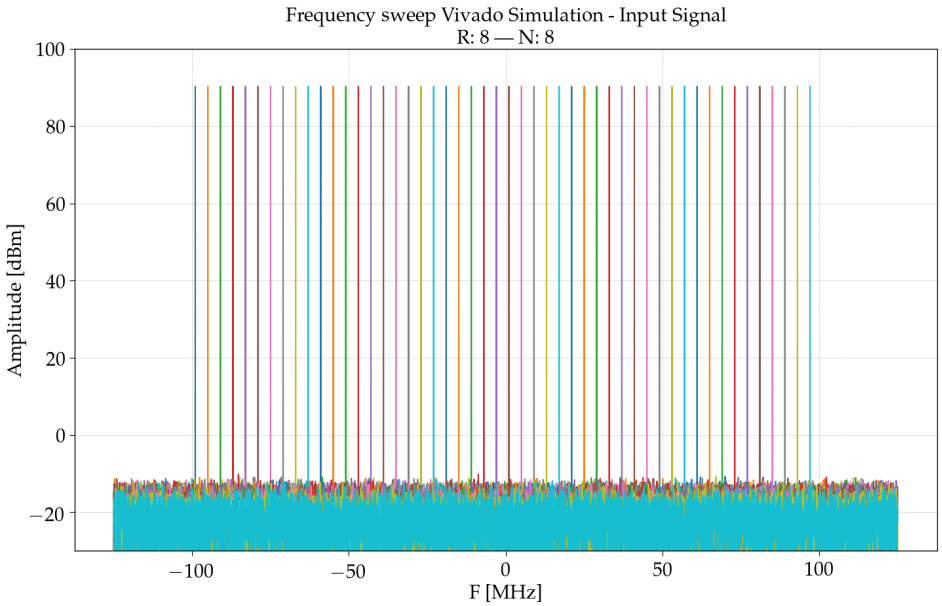
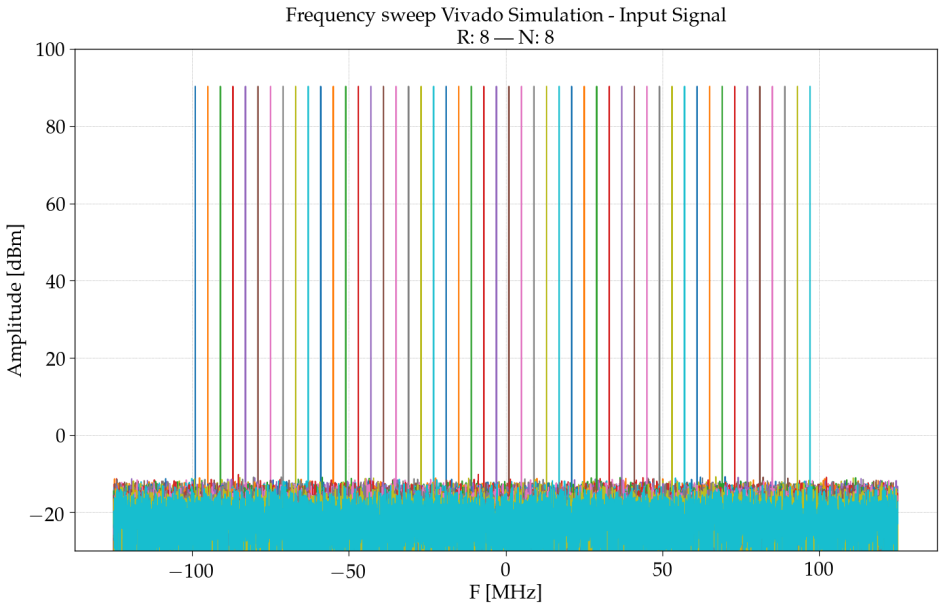


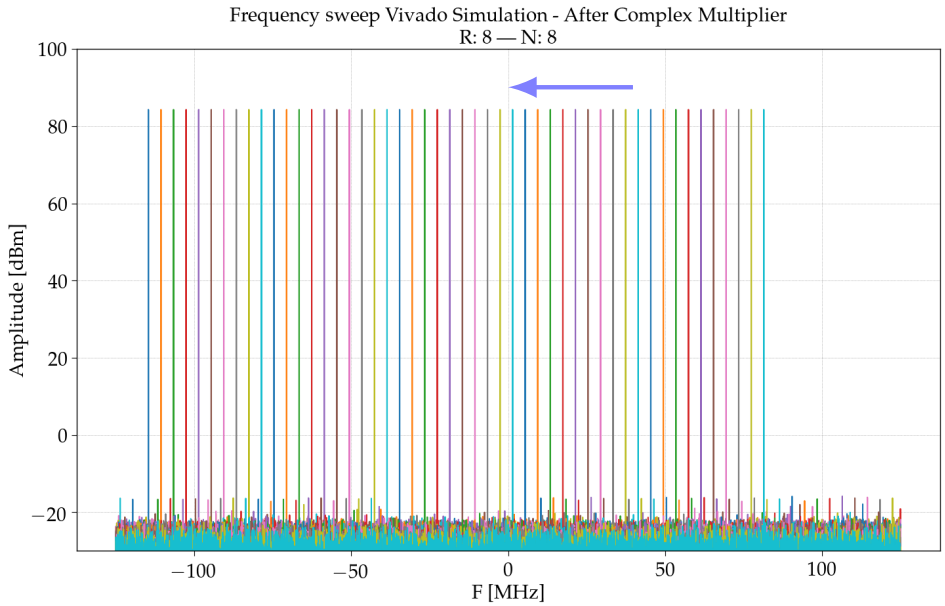
Figure: New DDC stage digital output spectrum - 31.25 MSPS

Vivado Simulation (HDL/RTL)

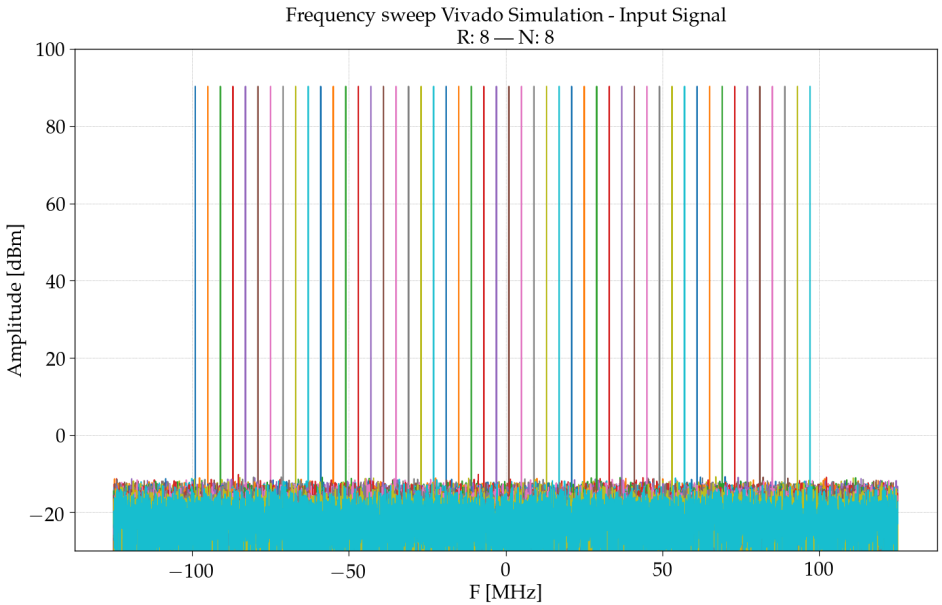


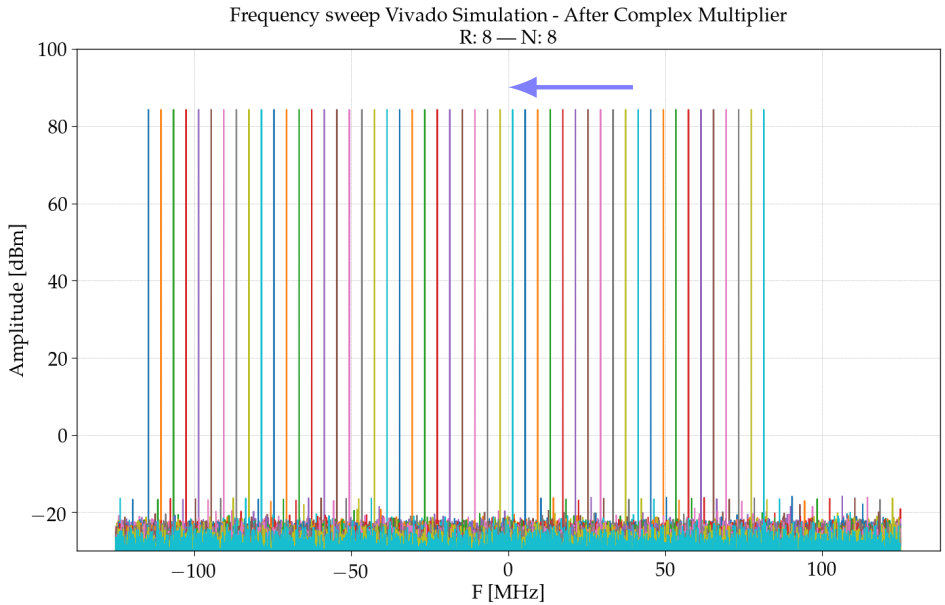
Vivado Simulation (HDL/RTL)

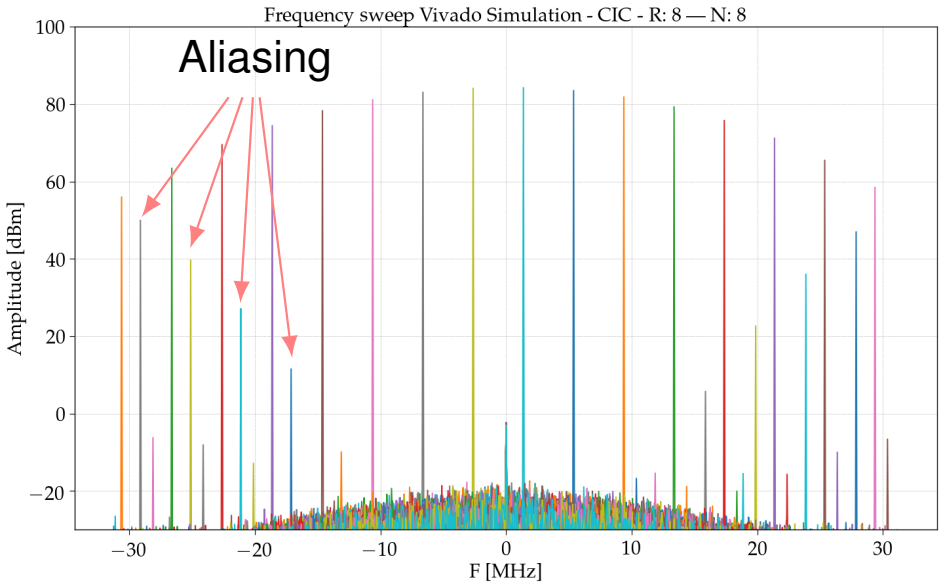


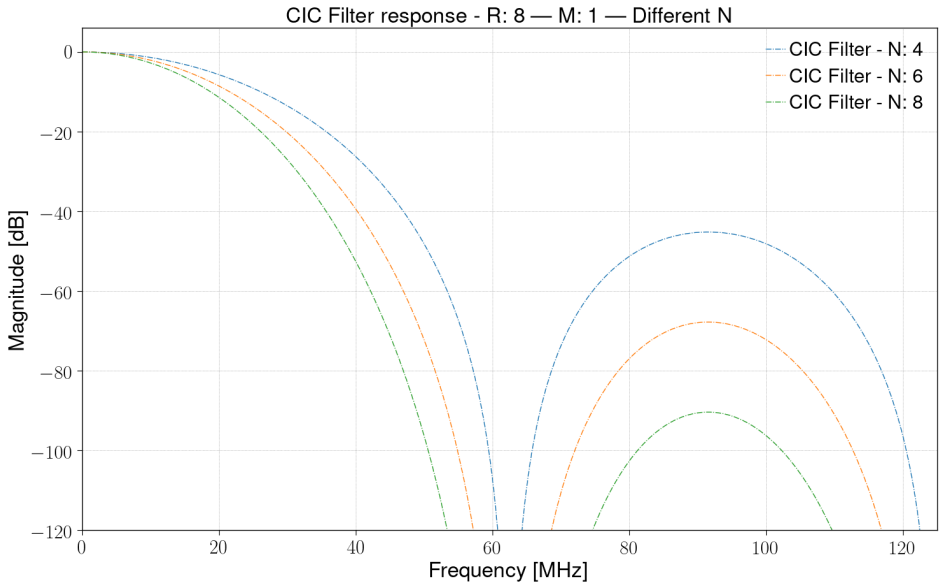


Vivado Simulation (HDL/RTL)

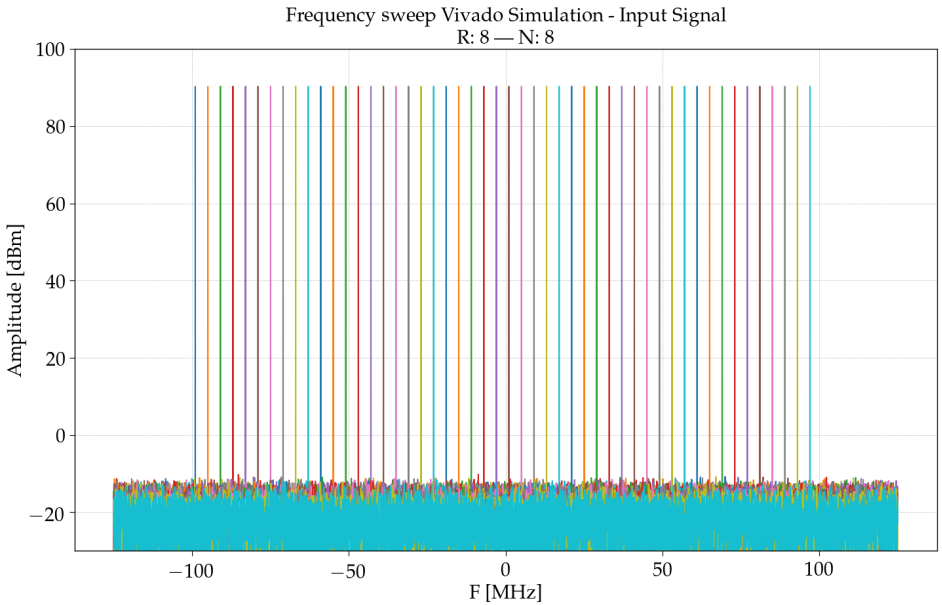


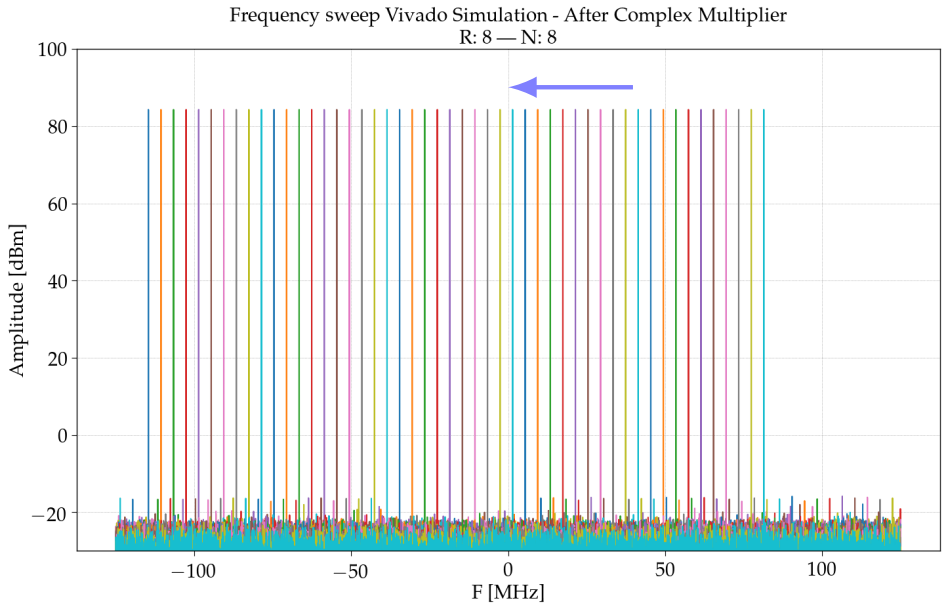


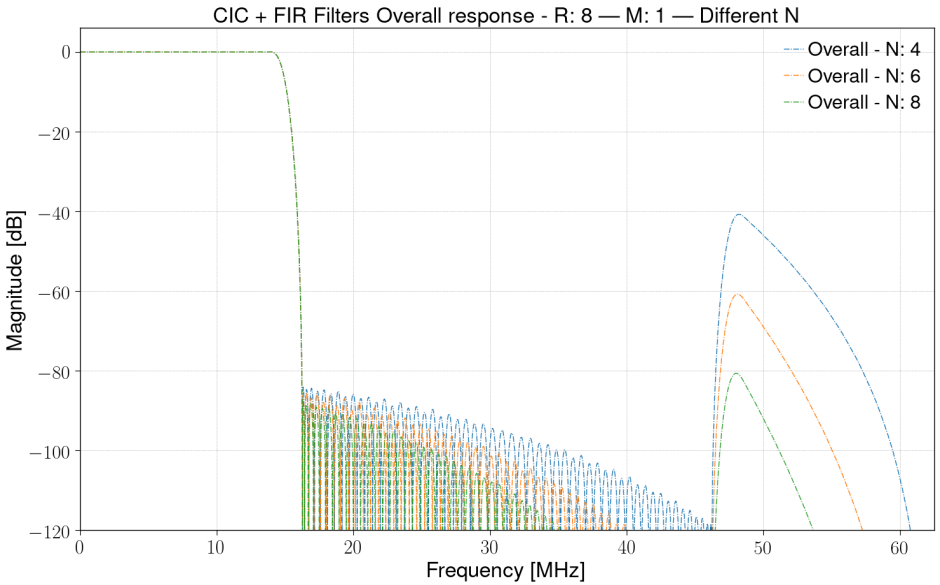


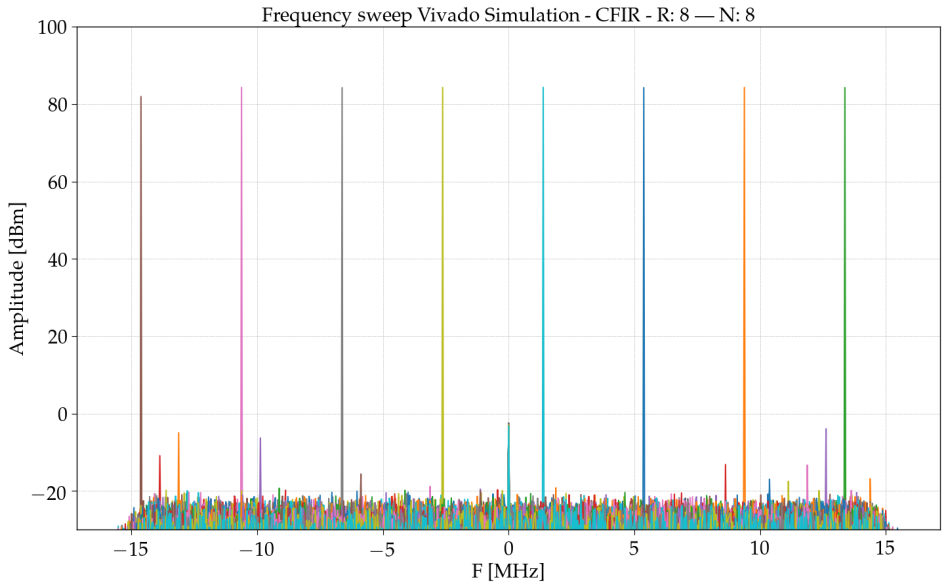


Vivado Simulation (HDL/RTL)

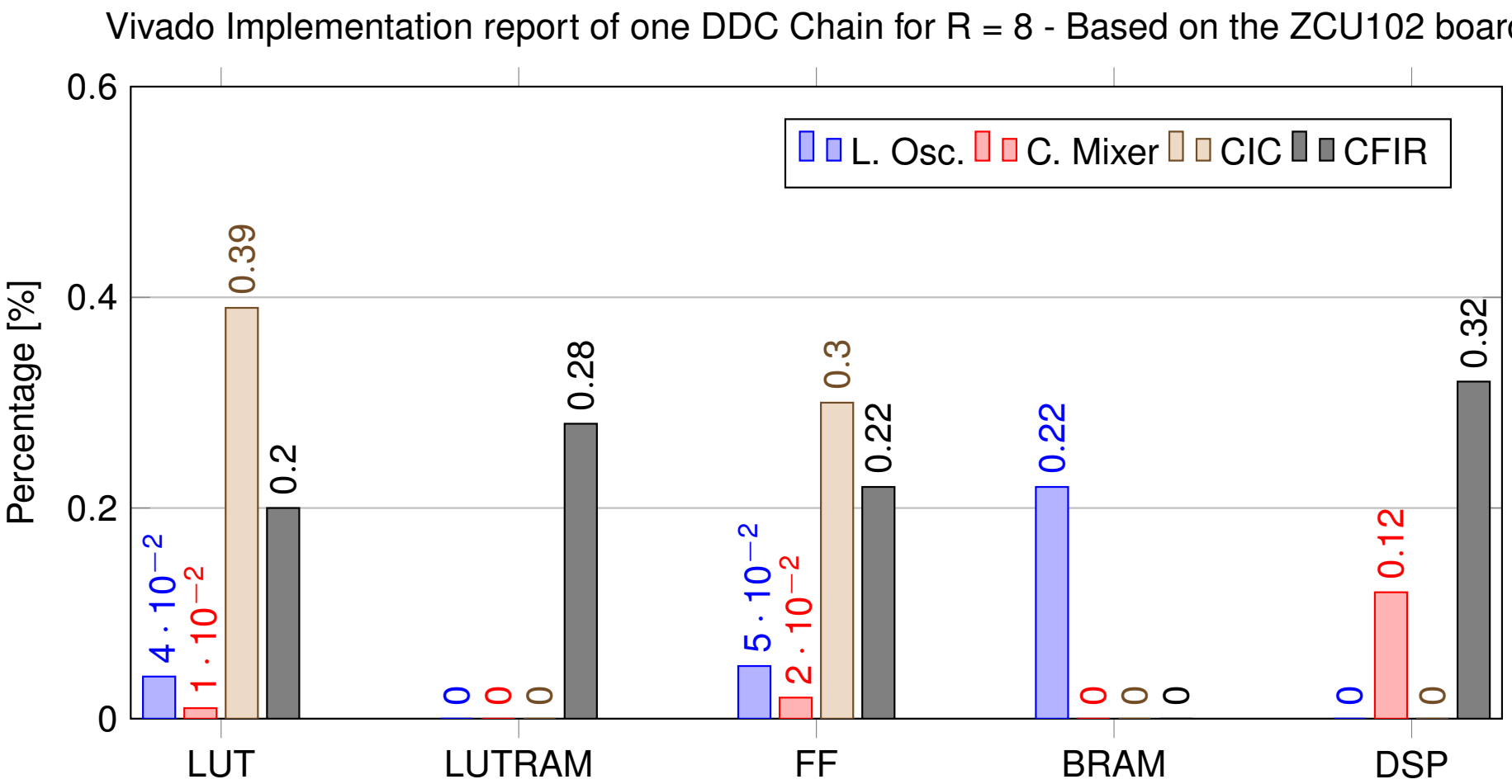








FPGA Resource utilization

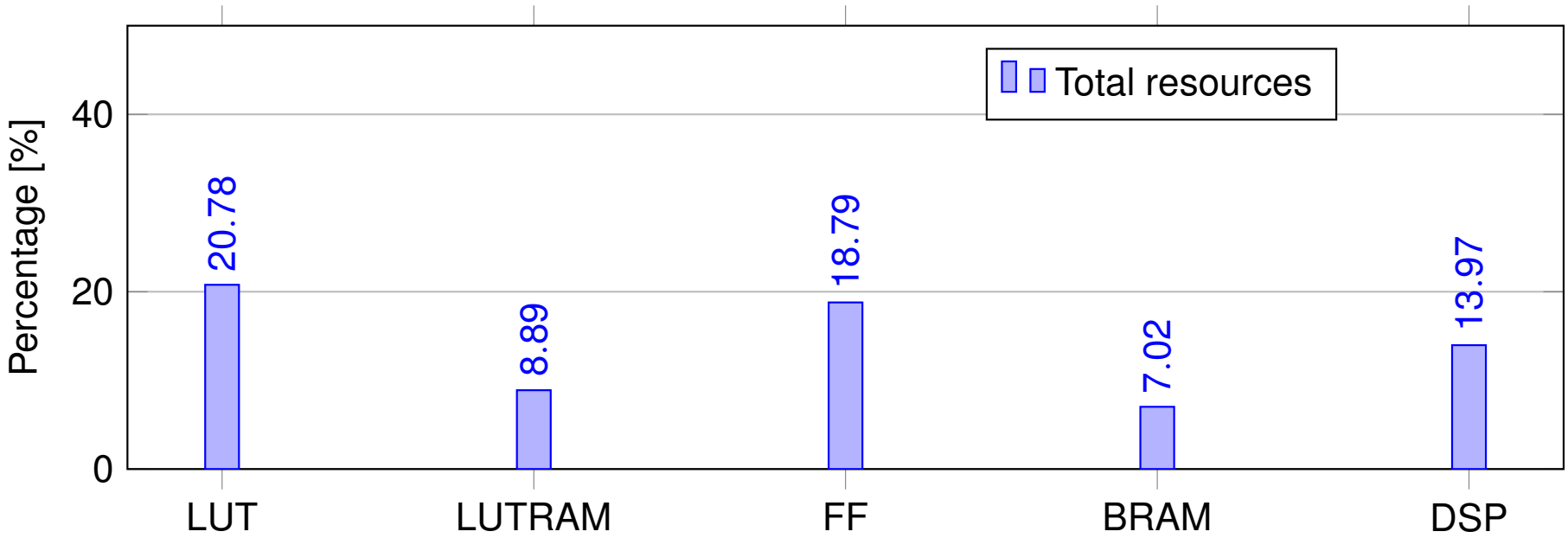


Where: *L. Osc.*: Local Oscillator, *C. Mixer.*: Complex Mixer, *CIC*: Cascaded Integrator-Comb filter, *CFIR*: Compensation Decimation FIR filter.

FPGA Resource utilization

- Decimating by 8 means that per each ADC output channel, there will be 8 subbands,
- 8 subbands means 8 DDC chains per ADC ouput channel,
- Then, 32 channels = 32 DDC chains,
- Finally, the previously enumerated resource have to multiplied by 32

Implementation report of 32 DDC Chains for R = 8 - Based on the ZCU102 board



So.. what about the rest of the acquisition chain?

The estimation for the following modules...

- The following modules in the acquisition chain needed to be adjusted to this new structure,
- The Goertzel Filter (GF) (*Windowing* + *Goertzel Algorithm*(GA)) now works in a mixture of FDM and TDM, where each GF is running 8 times faster (but much slower than in the old firmware version) than the input data sampling rate allowing the process of 4 complex components per GF,
- While each GA needs 2 DSP Slices, the benchmark suggest the use of 0.25 DSP Slice per complex tone: 50 filters for 200 complex tones per ADC (100 DSP Slices),
- After the GF the data rate is considerably slow compared to the logic operation frequency, suggesting that for the *Module & Phase Processor* only 16 DSP Slices are needed. And finally, the *Flux-Ramp Demodulation module* only 28 DSP Slices.

So.. what about the rest of the acquisition chain?