Karlsruhe Institute of Technology

Timing and Fast Control @ ITIV

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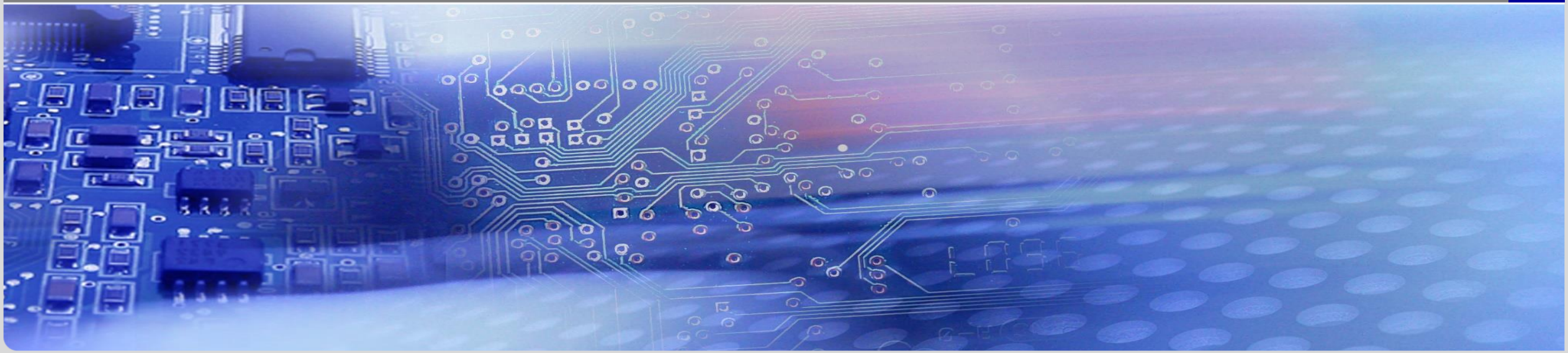
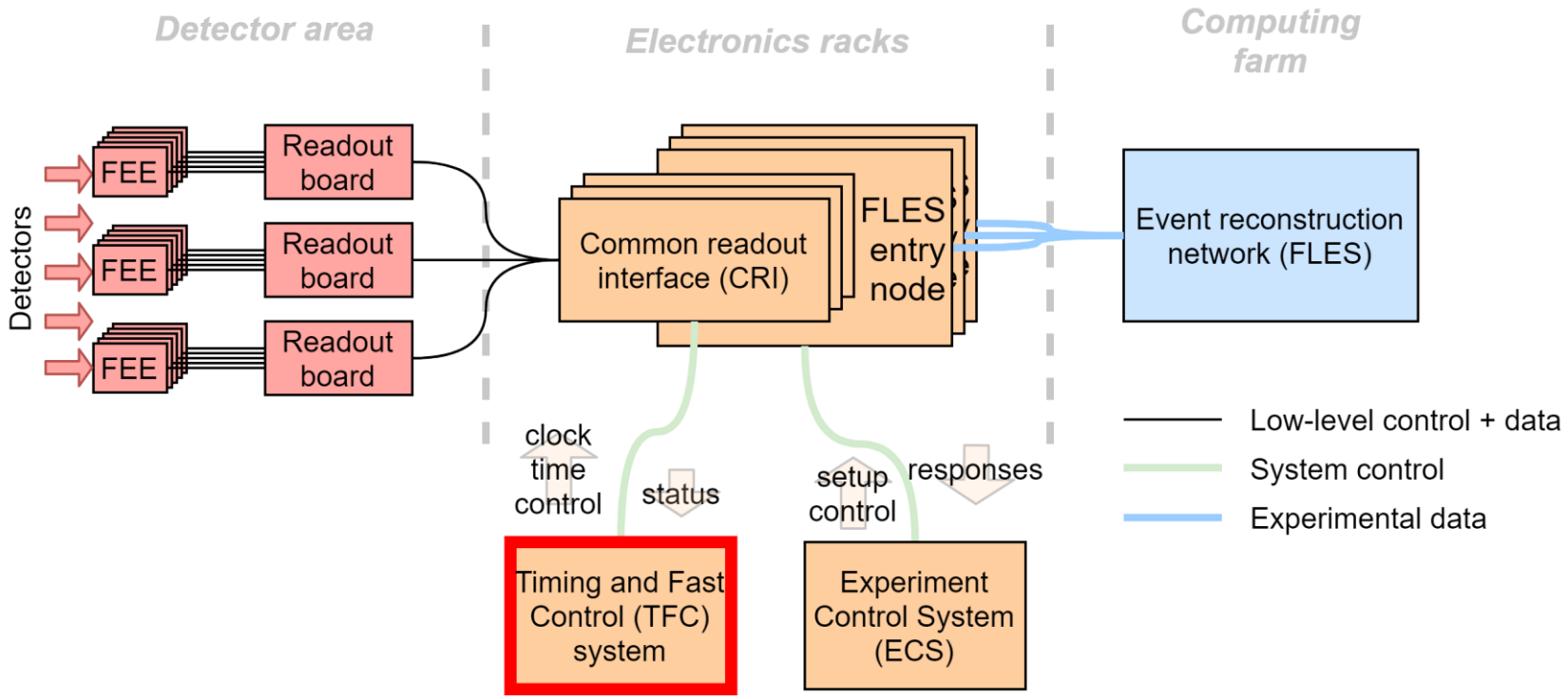
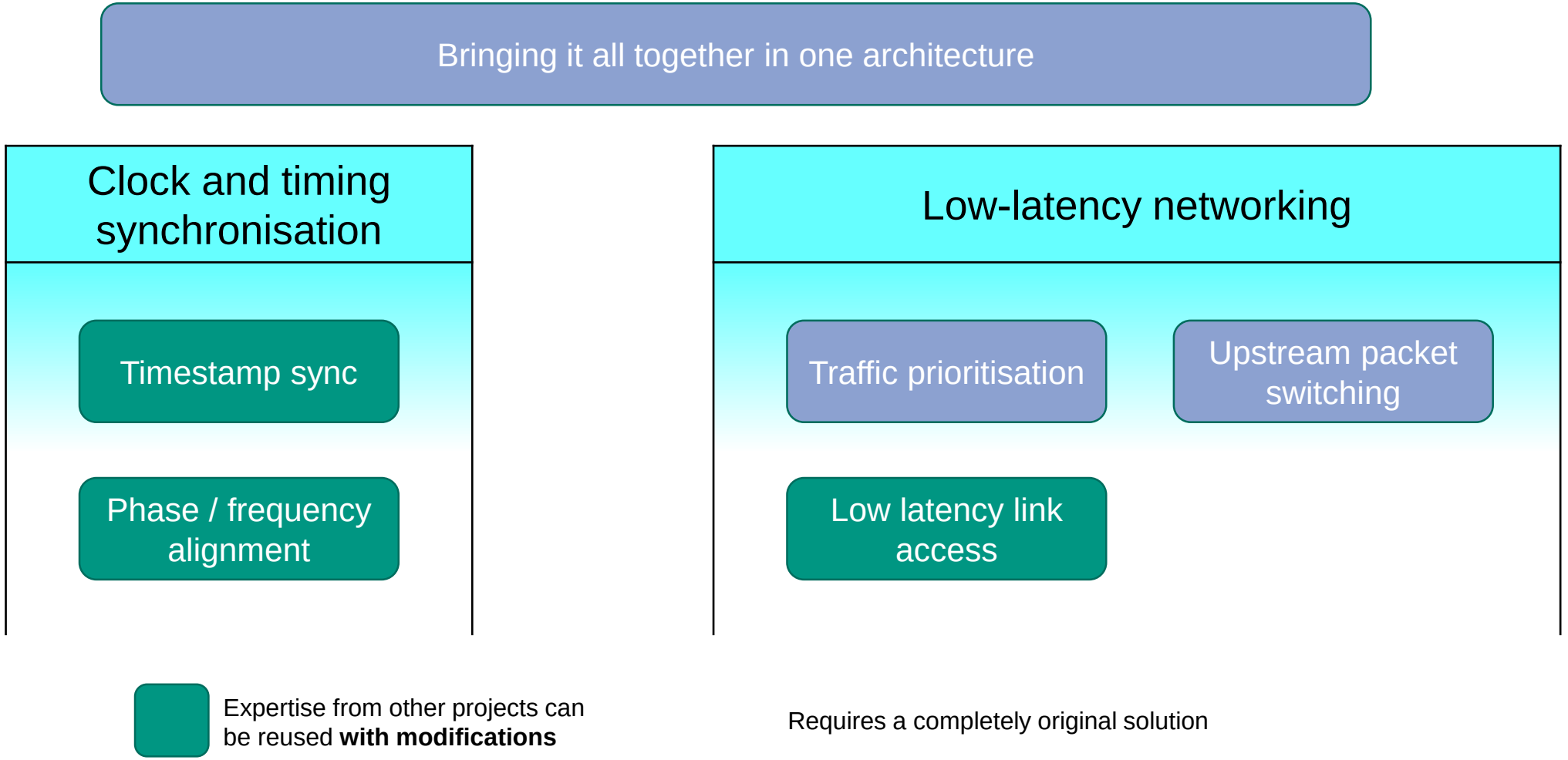


TFC - mission

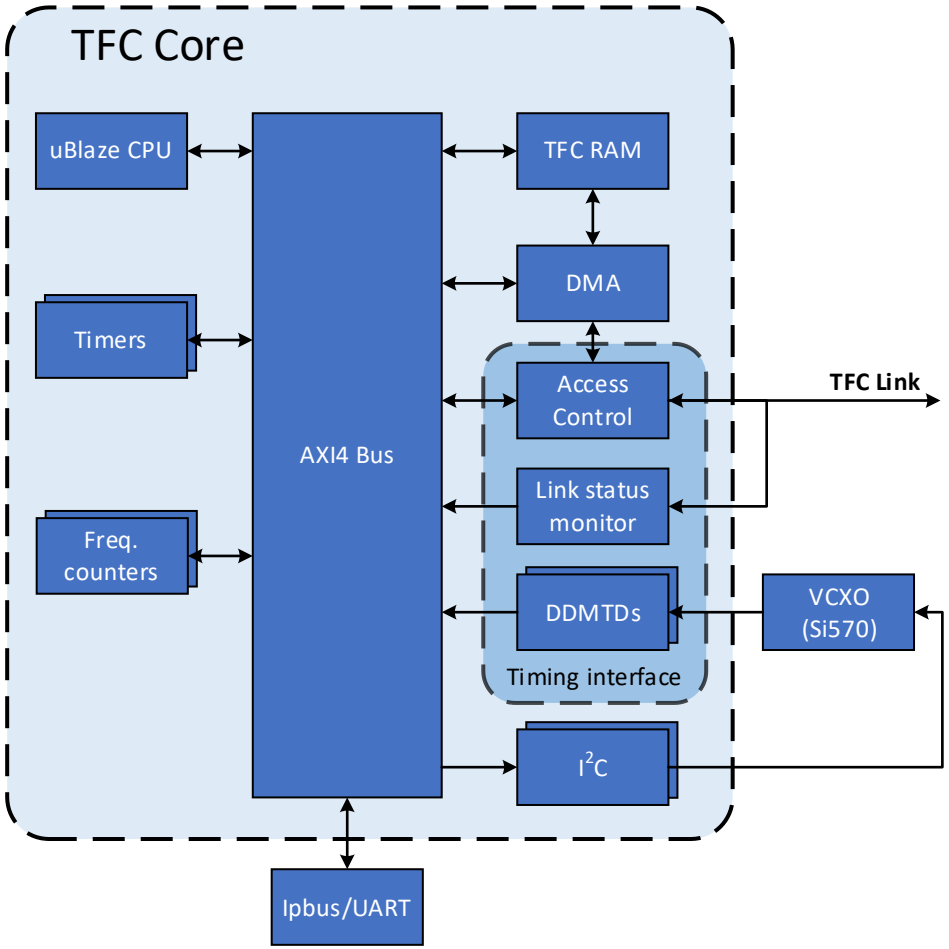
- (Re)synchronise data acquisition hardware with ~1 ns accuracy
- Perform system-wide flow control with round trip latency <10 us
- Scalable - >> 100 nodes



Problem structure

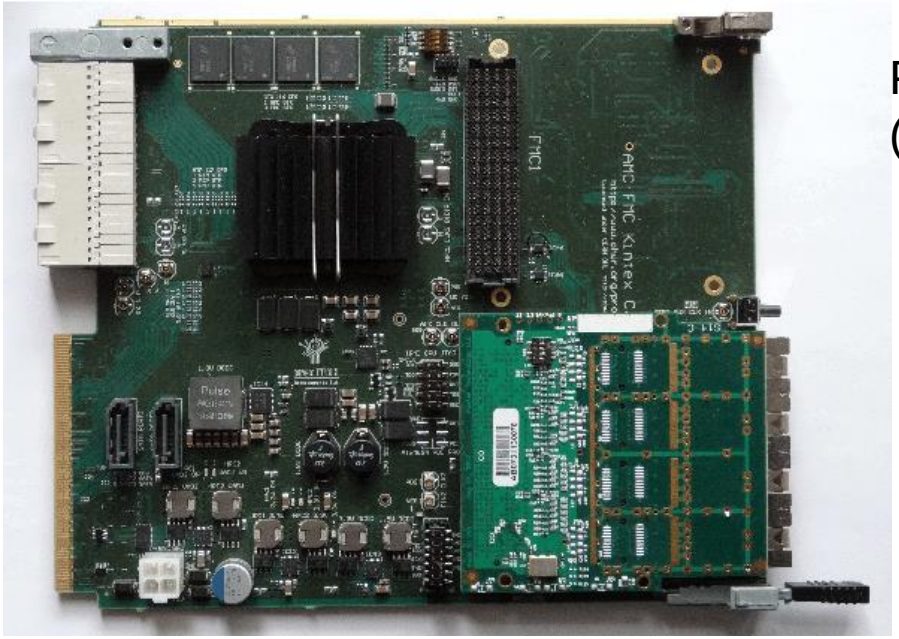


pre-TFC1



Features:

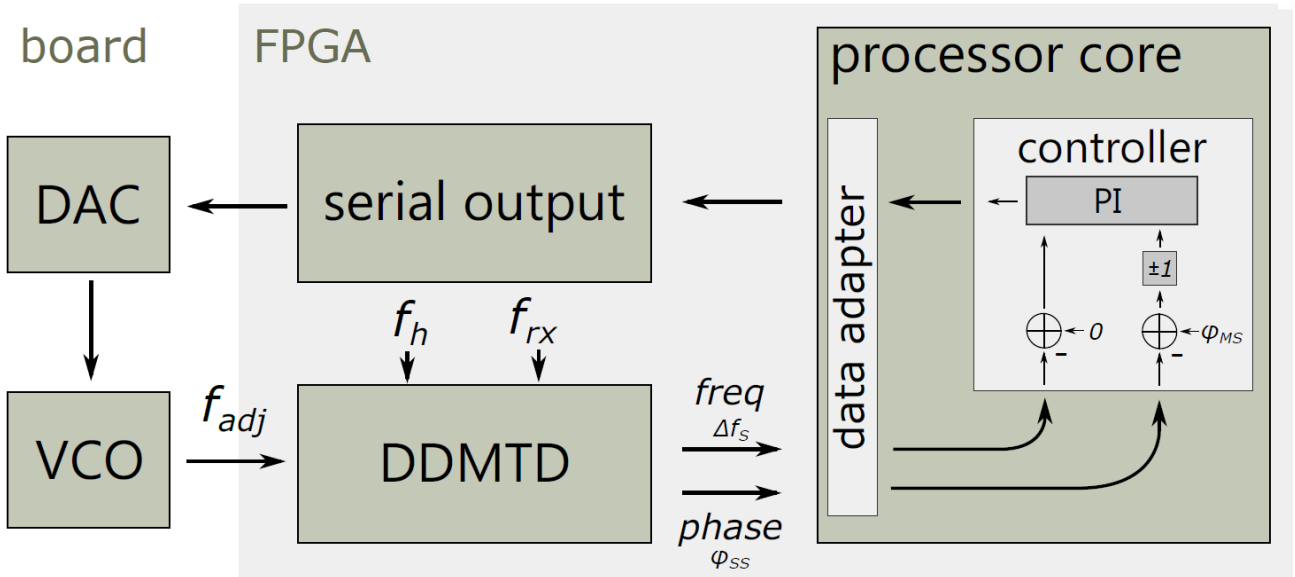
- Flexible Soft-PLL with accurate all-digital phase measurement
- Dual PI controller for parallel frequency and phase lock

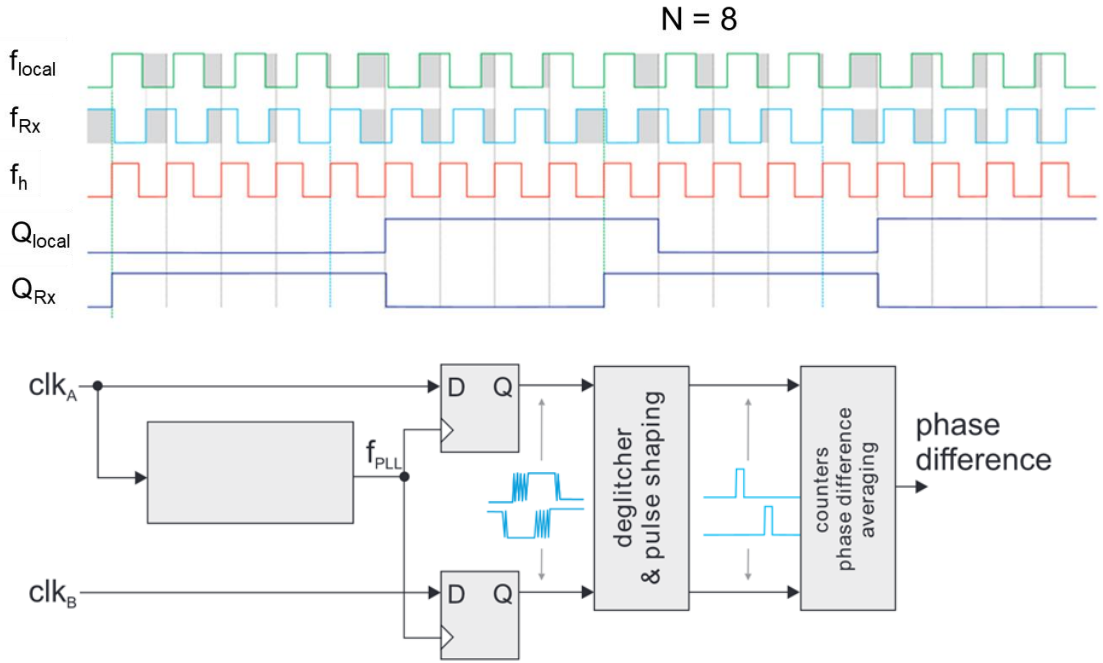


Platform: AFCK (Kintex-7)

SoftPLL

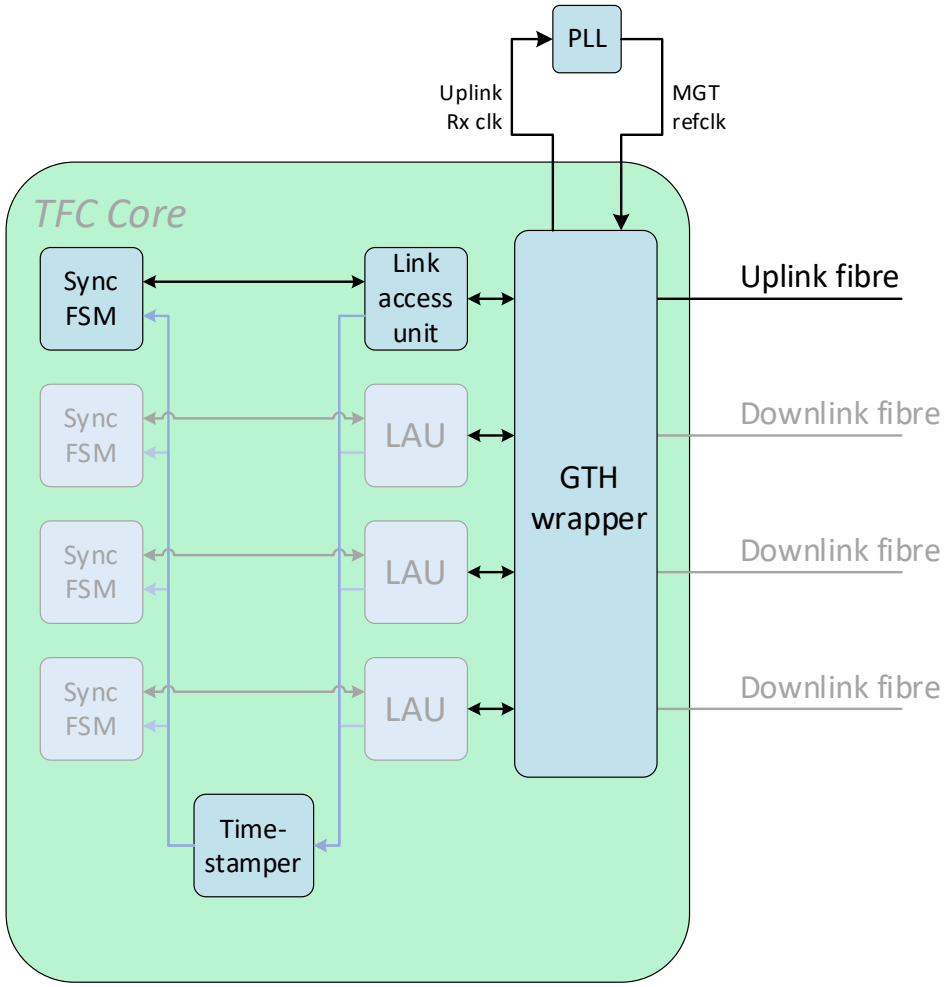
- Allows for easy implementation of complex control algorithms in C





$$f_{PLL} = \frac{N+1}{N} \cdot f_{\text{ref}}$$

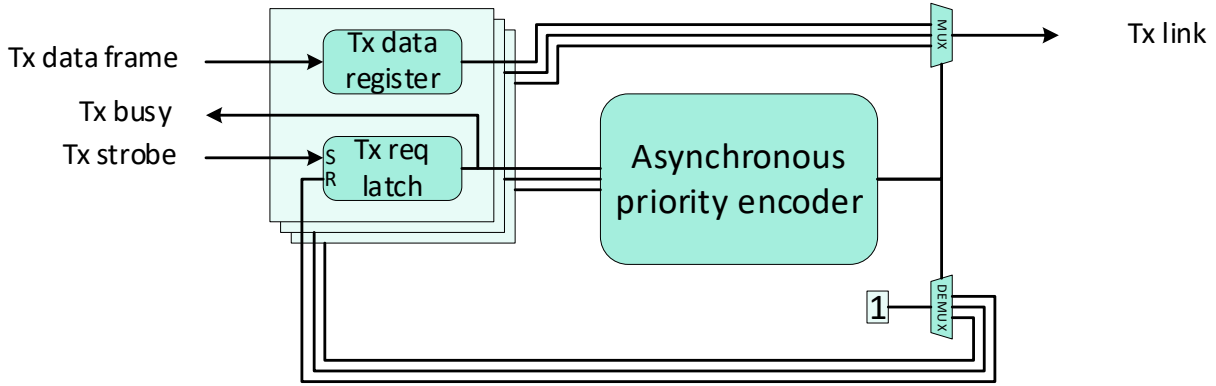
pre-TFC2



Features:

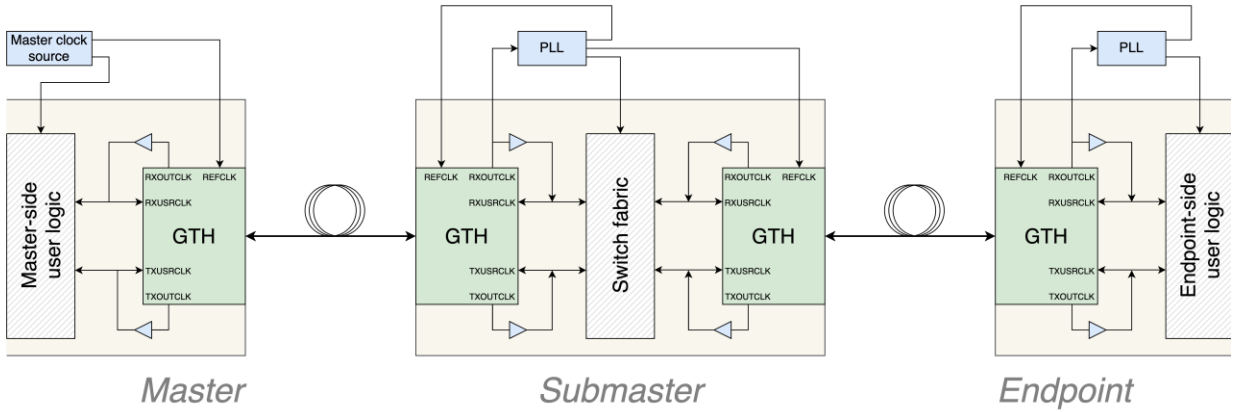
- Hard-PLL for frequency and phase alignment
- Original link access unit design for prioritised link access with no dead time

Traffic prioritisation in Link Access Unit (LAU)



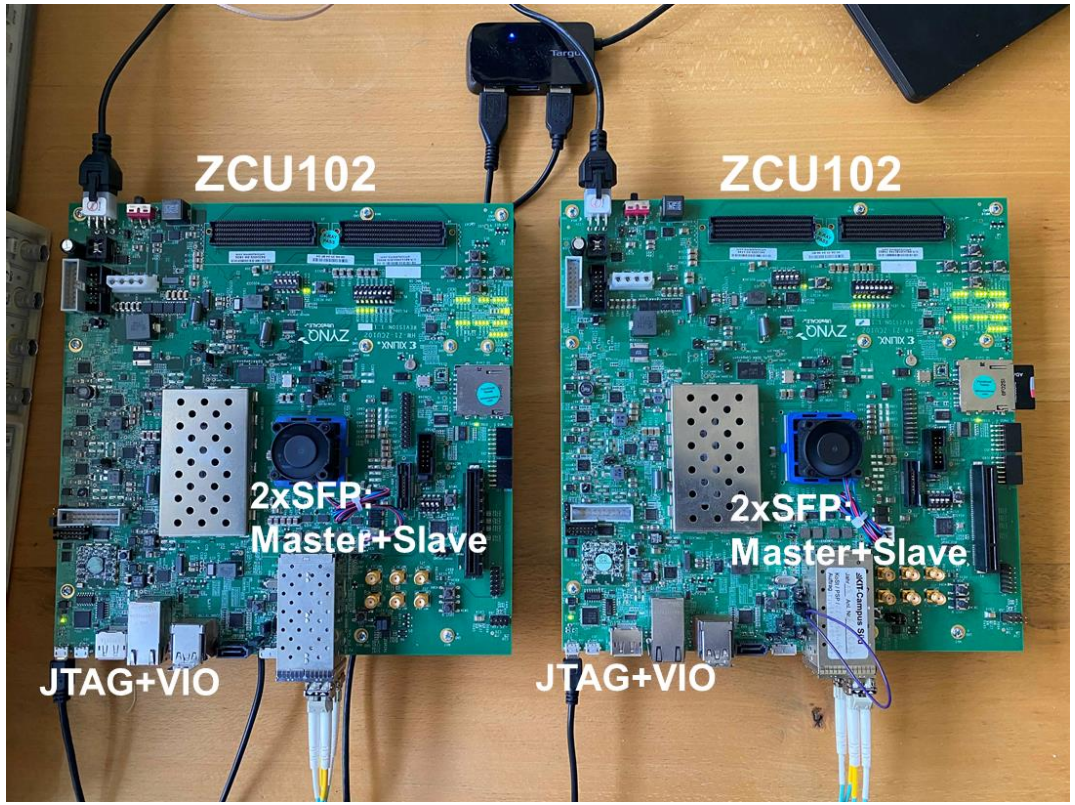
pre-TFC2

- Negotiation-based timestamp synchronisation (delay-compensated)
- Cascaded clock recovery



pre-TFC2

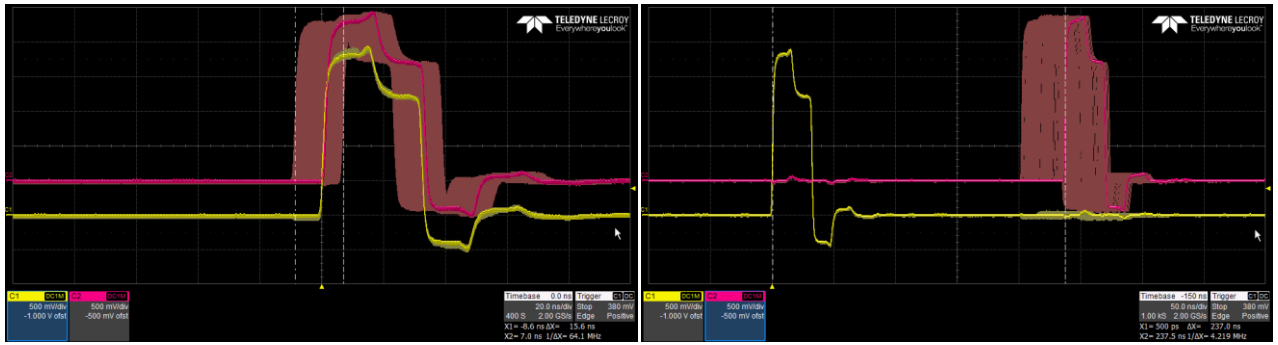
Prototype setup (Zynq-US)



Features:

- Hard-PLL for frequency and phase alignment
- Original link access unit design for prioritised link access with no dead time

First synchronisation and latency measurements (latency ~ 200 ns)

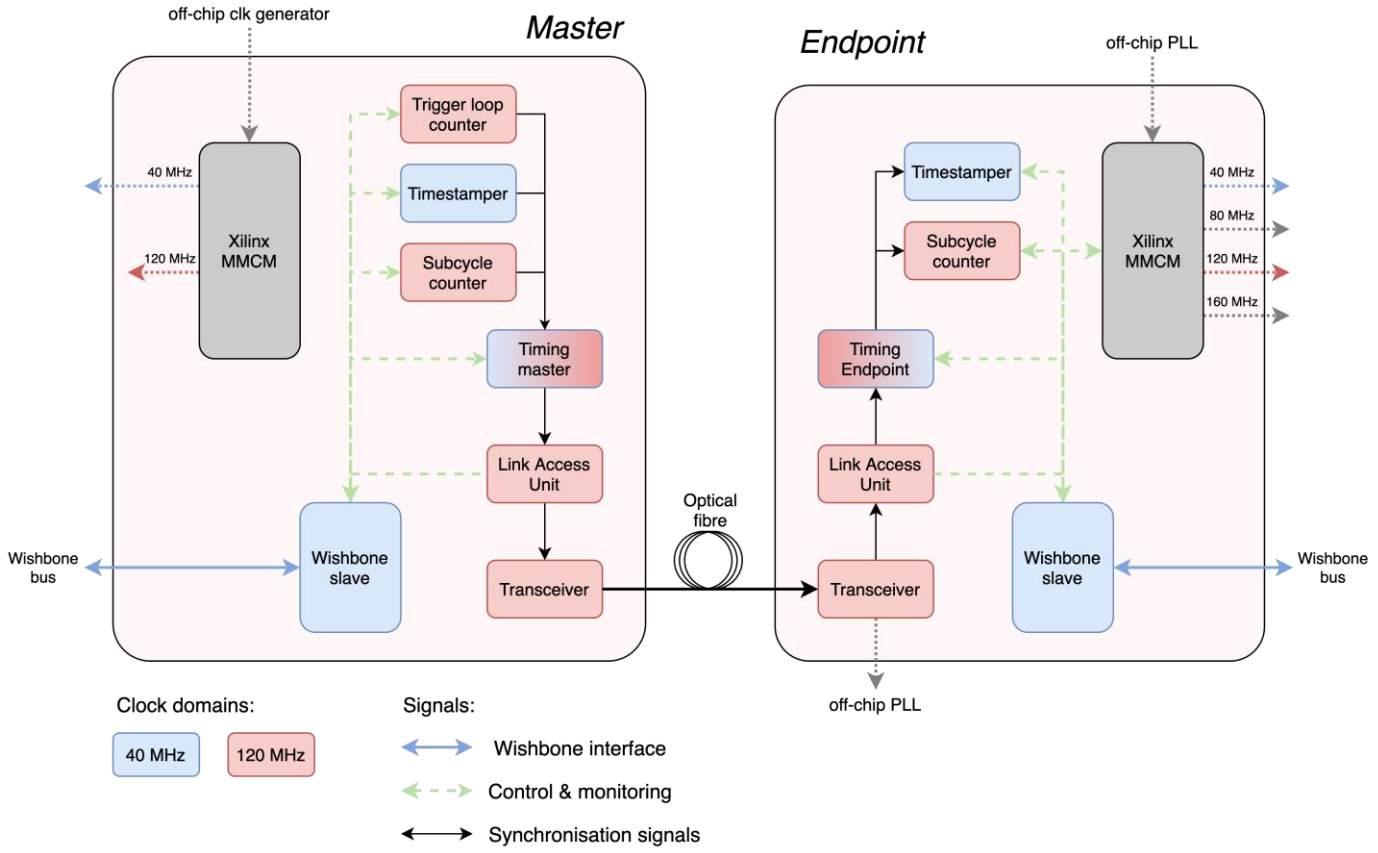


TFC1

- Timestamp broadcast scheme
- Cascaded clock recovery (hardware PLL)
- Rx and Tx FIFOs used
- Fully integrated into experimental infrastructure

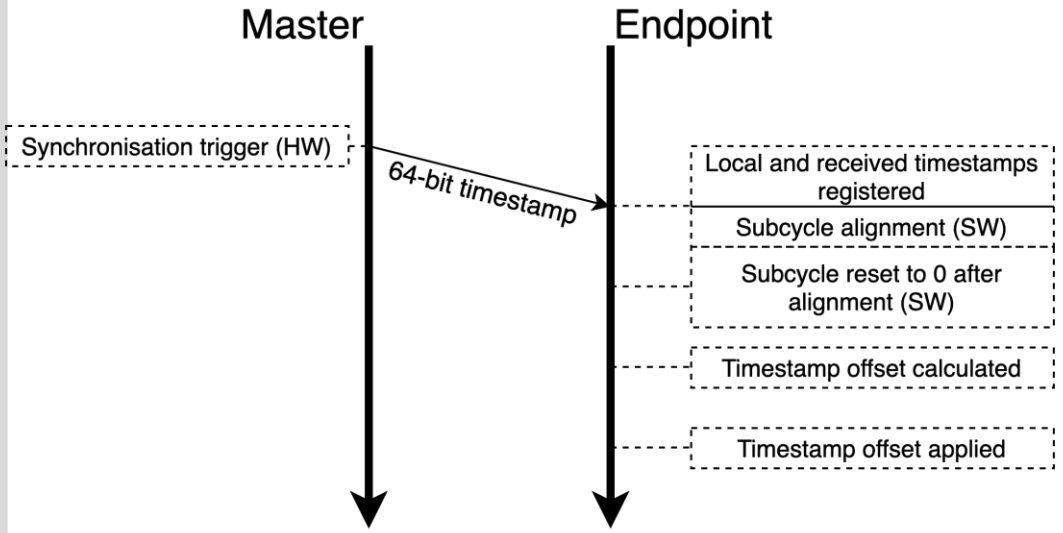
Platform board: BNL-712 (Kintex-US)

Prototype firmware architecture

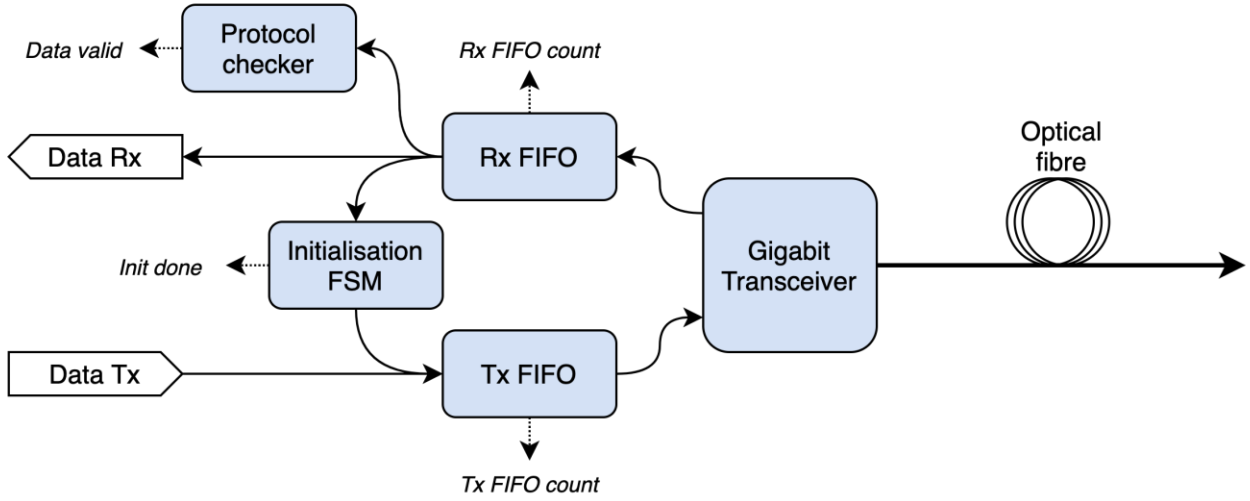


TFC1

Timestamp synchronisation



Link access unit

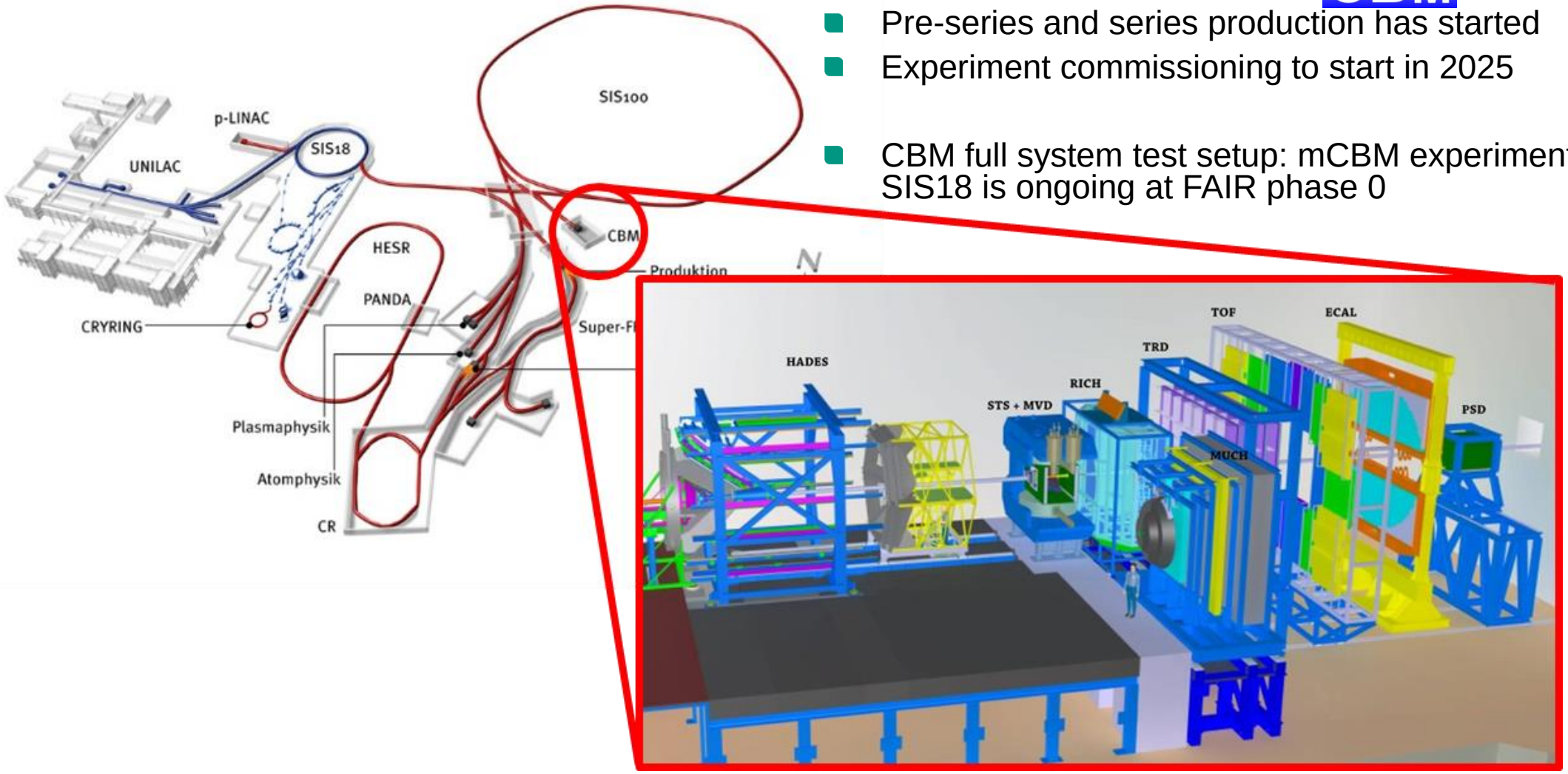


Next steps (global)

- GBT transport interface for out-of-box latency optimisation and determinism
- Integrate negotiation-based timestamp synchronisation
- Evaluate TClink for fine phase shift tuning

BACKUP

CBM Experiment @ FAIR



- Pre-series and series production has started
- Experiment commissioning to start in 2025

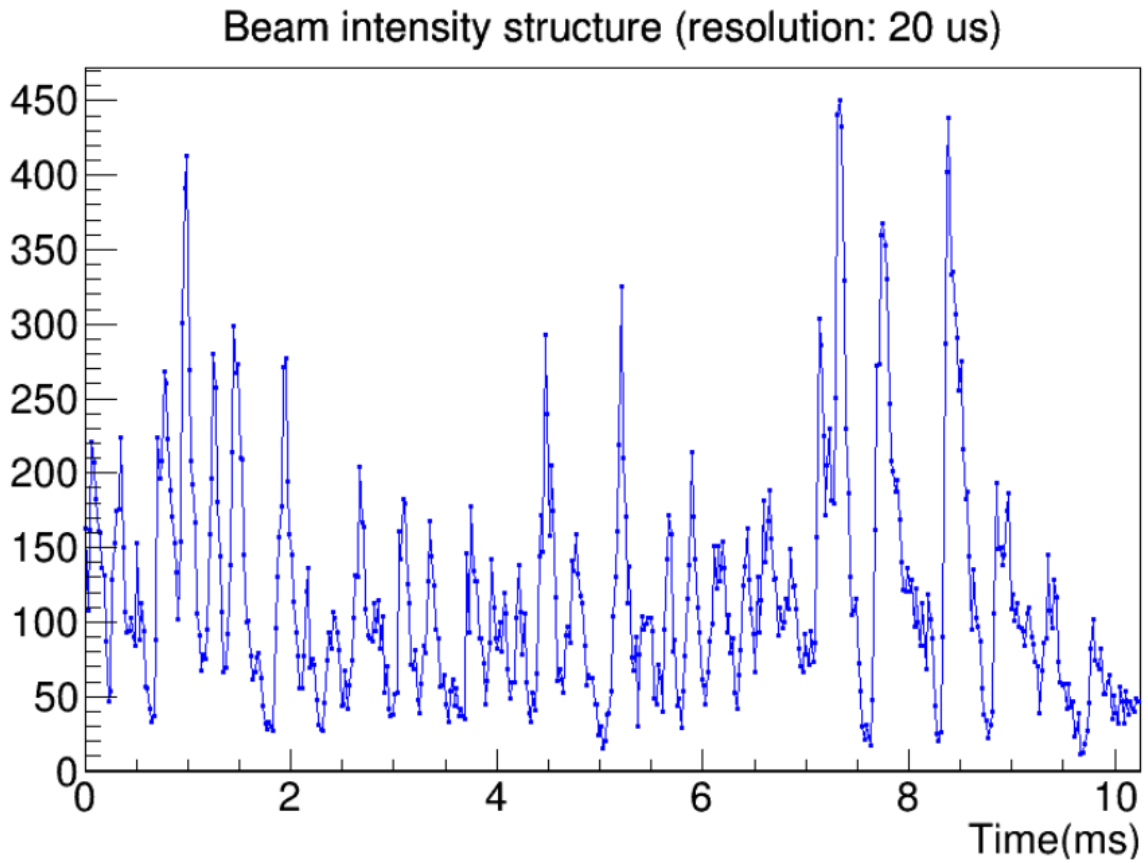
- CBM full system test setup: mCBM experiment at SIS18 is ongoing at FAIR phase 0

Data Acquisition System

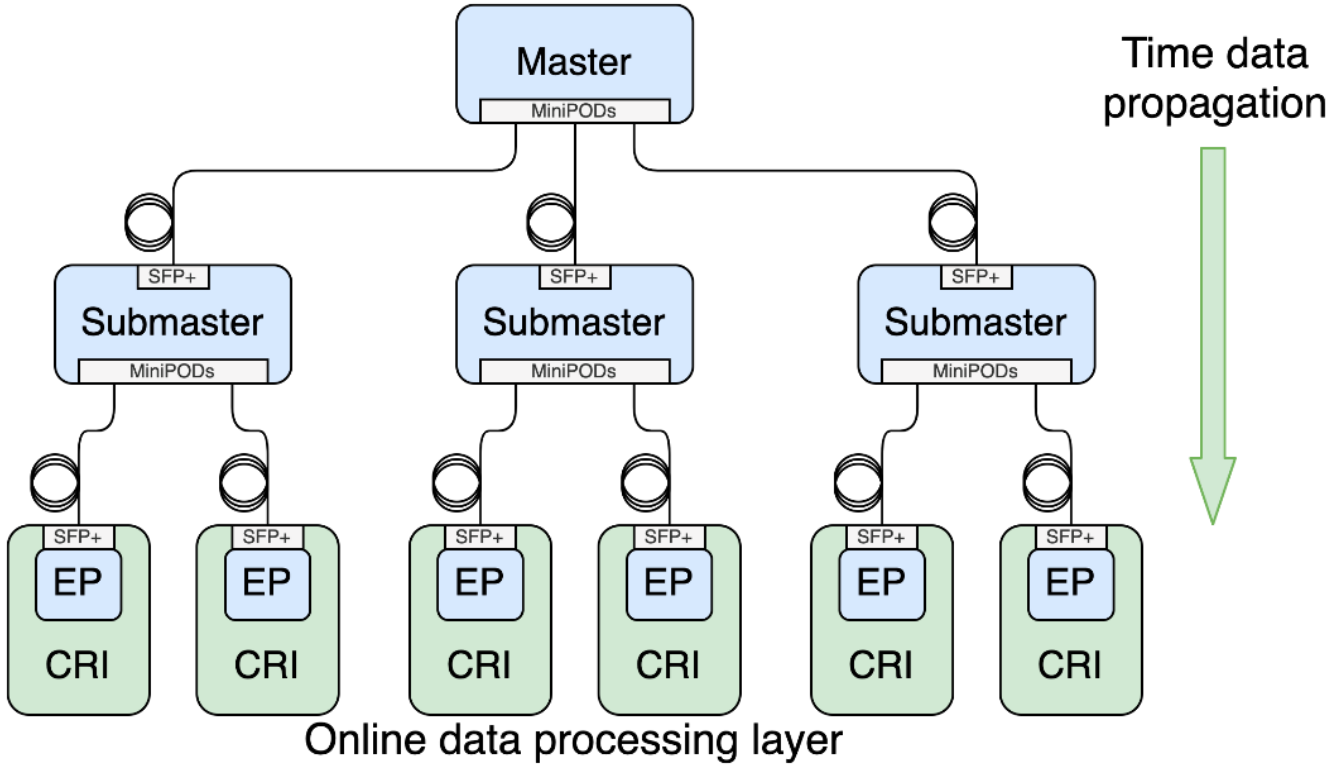
- Free-running DAQ (1 TB/s expected)
- Self-triggered timestamping front-end
- Occasional experimental data spikes

Throttling (study done by X. Gao):

- Versatile fast control network required



Topology


Master
MiniPODs
Time data propagation
SFP+
Submaster
MiniPODs
SFP+
Submaster
MiniPODs
SFP+
Submaster
MiniPODs
SFP+
EP
CRI
SFP+
EP
CRI
SFP+
EP
CRI
SFP+
EP
CRI
SFP+
EP
CRI
SFP+
EP
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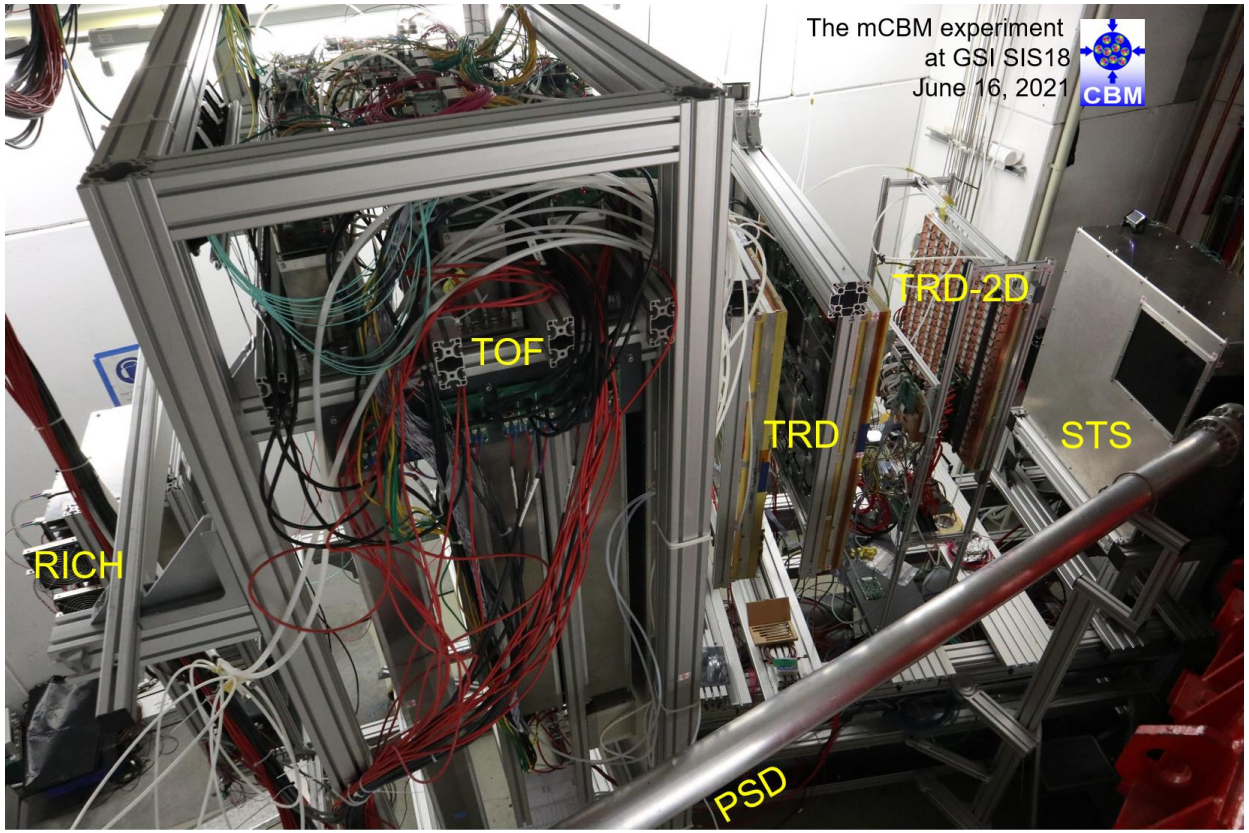
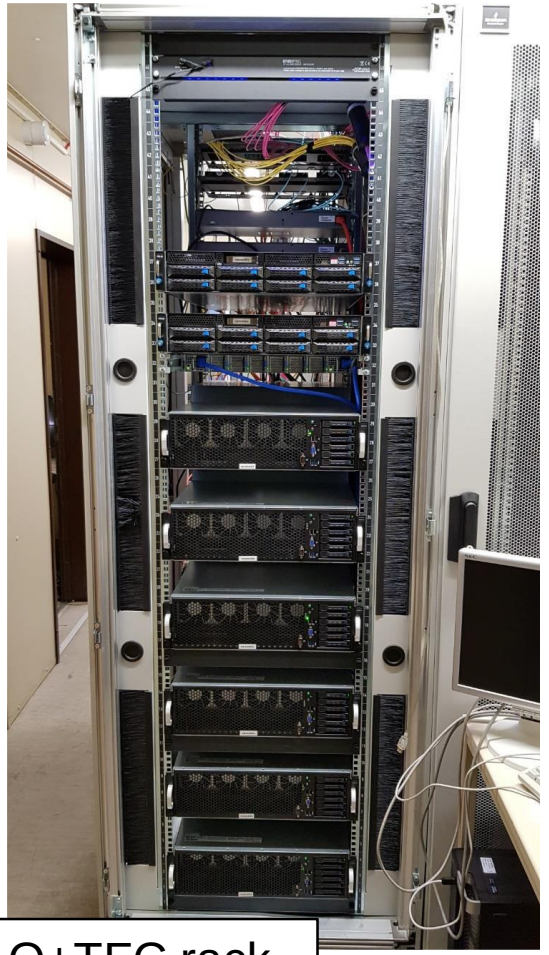
Online data processing layer

TFC1 beam test





DAQ+TFC rack

TFC1 beam test