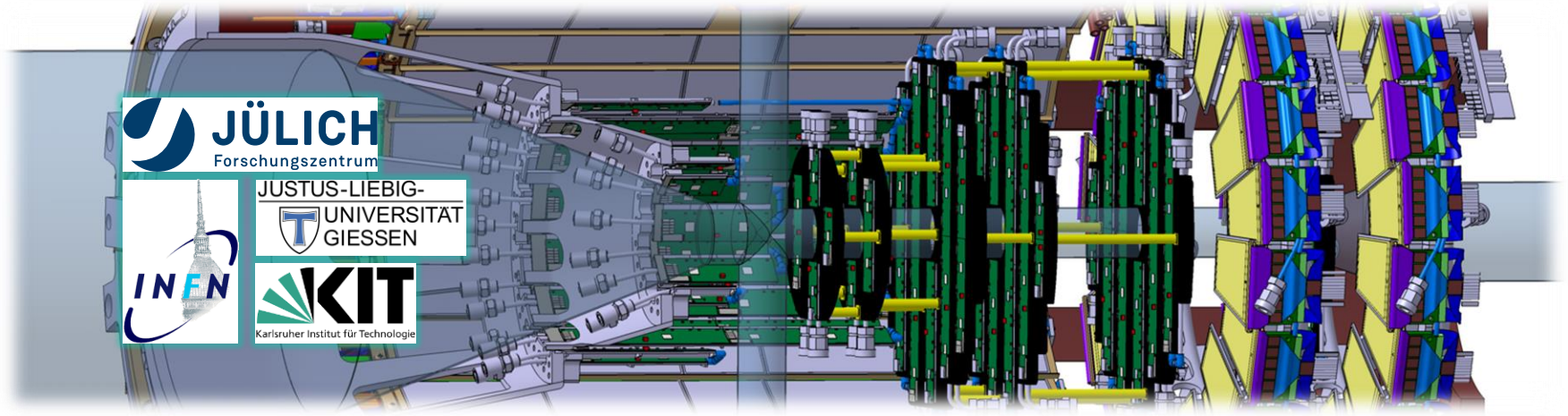
MDC architecture (Brainstorming)

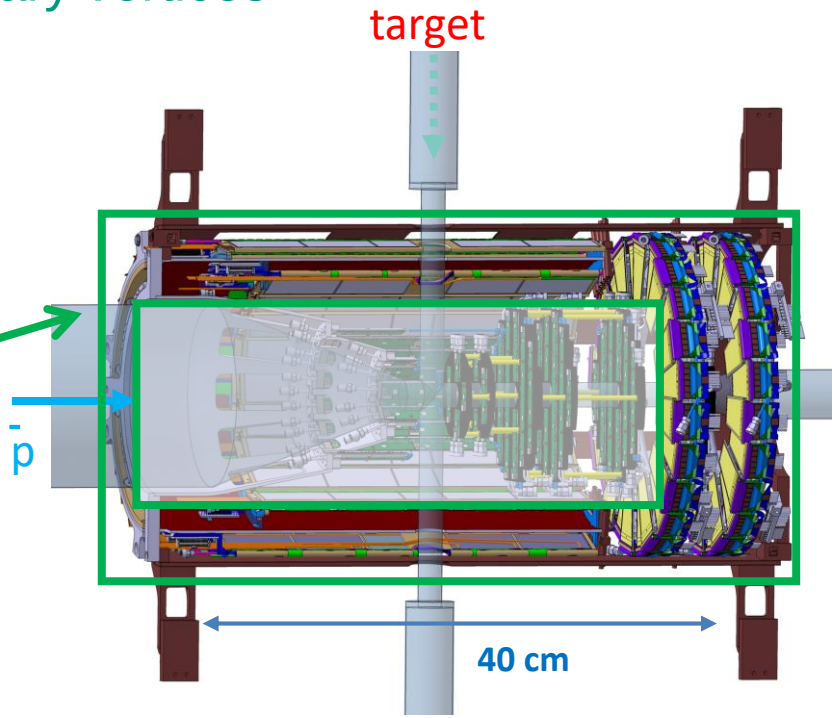
Michele Caselle



Micro Vertex Detector of PANDA

The innermost detector for precise tracking and detection of primary and secondary vertices

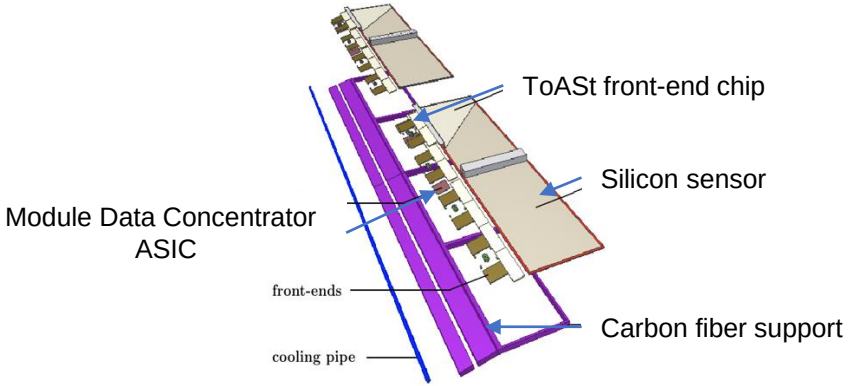
- **Hybrid silicon pixel**
  - 10 million pixel
  - 2 barrel layers + 6 disks
- **Silicon micro-strip**
  - 200,000 strip channels
  - 296 sensors
  - 2 barrel layers + 2 disks
  - 312 strip modules (Barrel)
  - 48 strip modules (Disk)



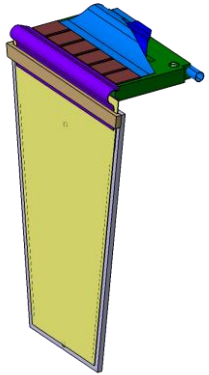
Silicon Strip Detector

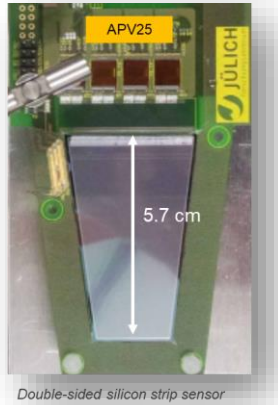
Complex detector modules for both barrel and disk

- **Barrel**
  - # 64 square sensor modules readout by 8 ToASt each
  - # 184 rectangular sensor modules readout by 11 ToASt each



- **Disk**
  - # 48 trapezoidal sensor modules readout by 12 ToASt each





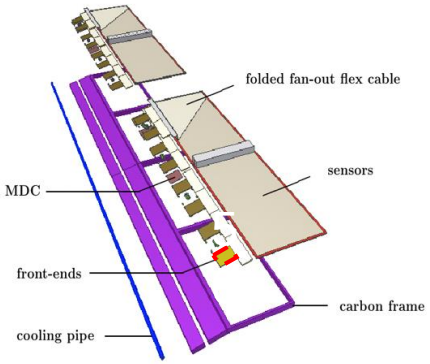
Double-sided silicon strip sensor

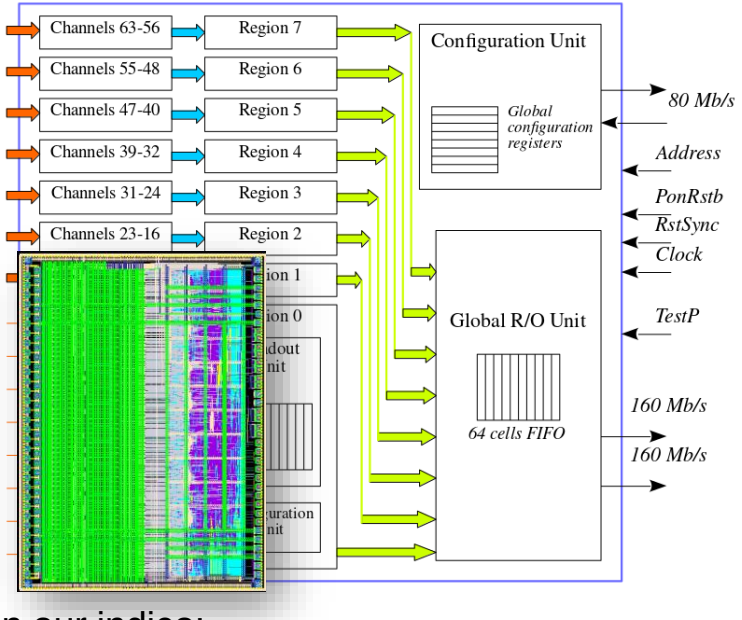
- # 296 MDCs are foreseen to transmit the data to the GBTX (or LpGBT) by e-link (320 Mb/s) interface
- # 30 GBTs are foreseen to readout the entire strip detector by optical links (to off-detector electronics)

Silicon Strip Detector

Status of ToASt front-end ASIC

- Design completed in UMC 110 nm by INFN-Turin
- Triple modular redundancy (TMR) logic protection
- Submitted on April, 28th , 2021
- HDL model still in preparation (Gianni)

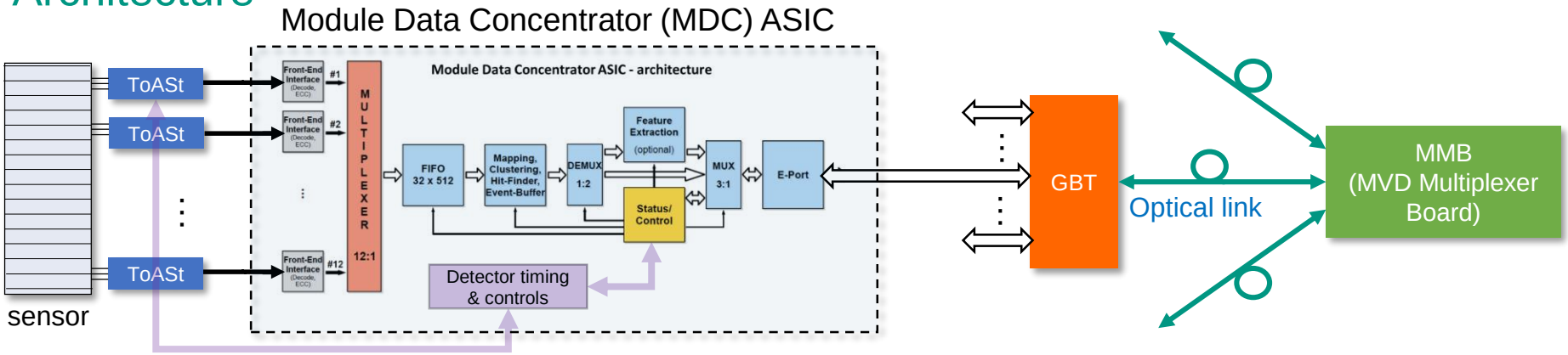




ToAST manual + material on our indico:
https://indico.scc.kit.edu/category/124/

Module Data Concentrator (MDC) - ASIC

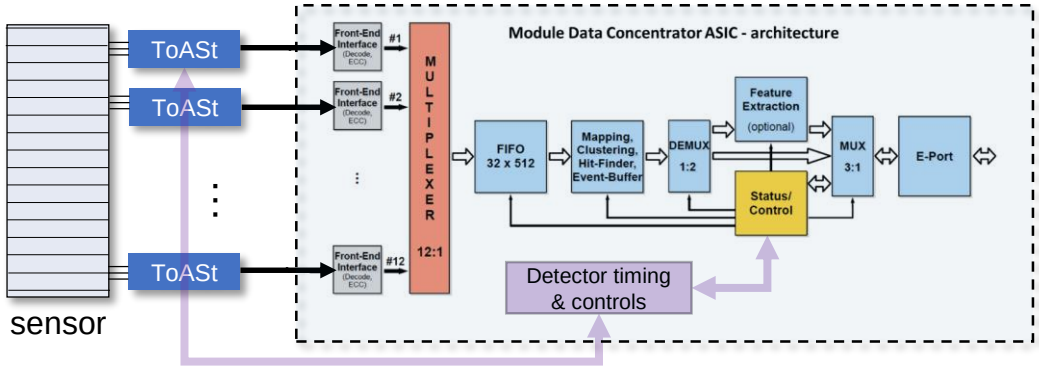
Architecture



- Developed in UMC 110 nm CMOS technology
- Digital logic based on *Triplicated Modular Redundancy* (TRM) for Single Event Upset mitigation (registers, memories and FSMs)
- First implementation on FPGA to prove the digital behaviour
- Electrical test by HghFlex 2 (HW platform)

Module Data Concentrator (MDC) - ASIC

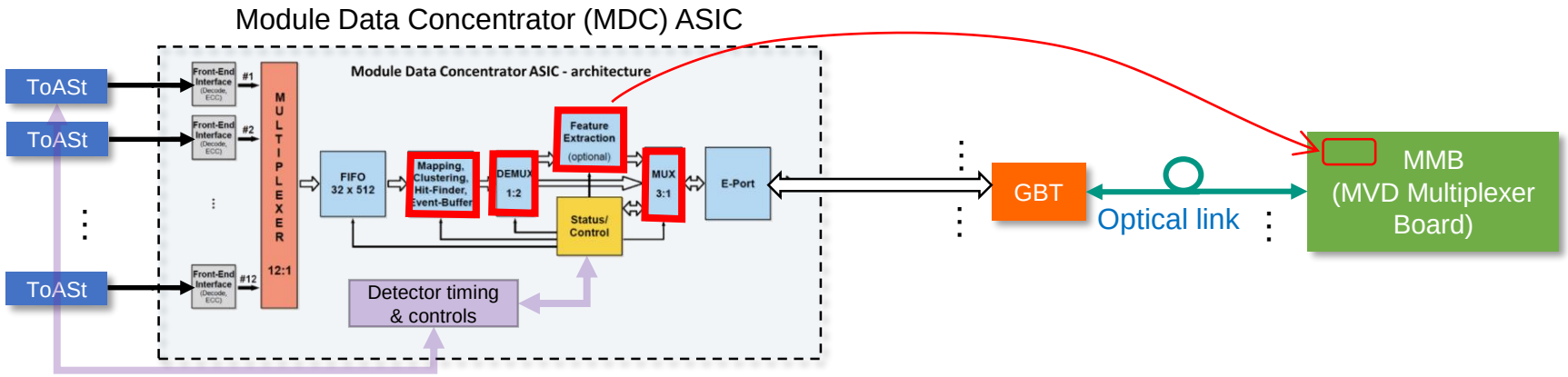
Architecture



- Only HDL codes (no IPcores)
- Reduce the logic as the minimum possible (no large memories user-space, limited number of states for FSM
- *Triplicated Modular Redundancy* (TRM) for Single Event Upset mitigation (registers, memories and FSMs)
- Power consumption as low as possible

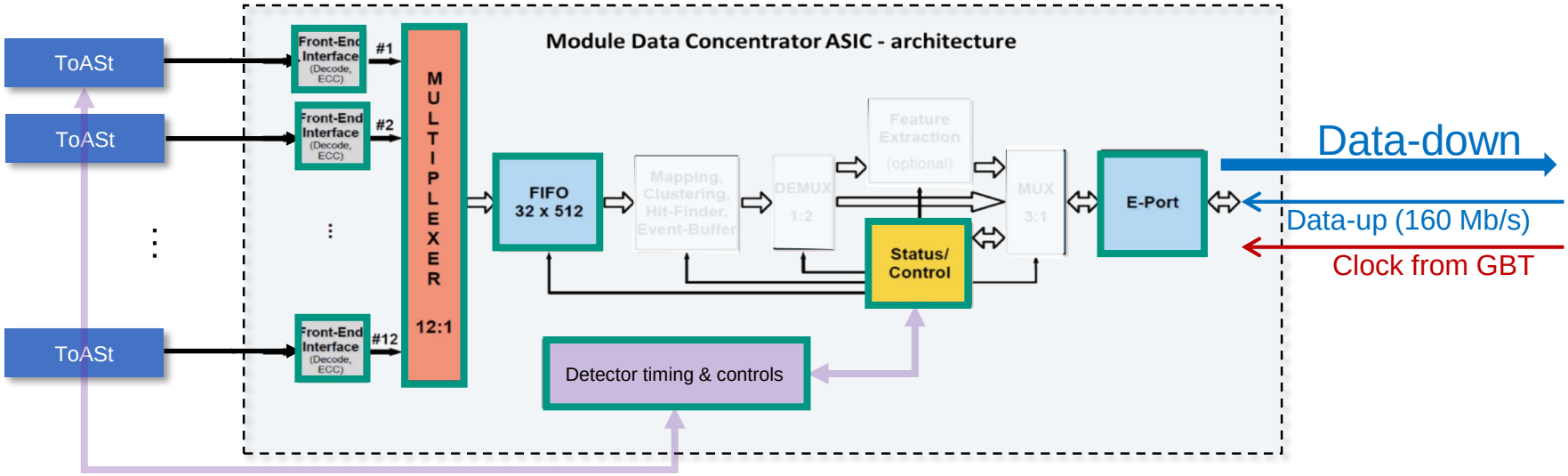
Module Data Concentrator (MDC) - ASIC

Current status and what's next



- Moving "Feature Extraction" data processing on more flexible programmable logic (FPGA)
- More flexibility, leveraging the ASIC design and more intelligent (ML) data processing on FPGA

Module Data Concentrator (MDC) - ASIC

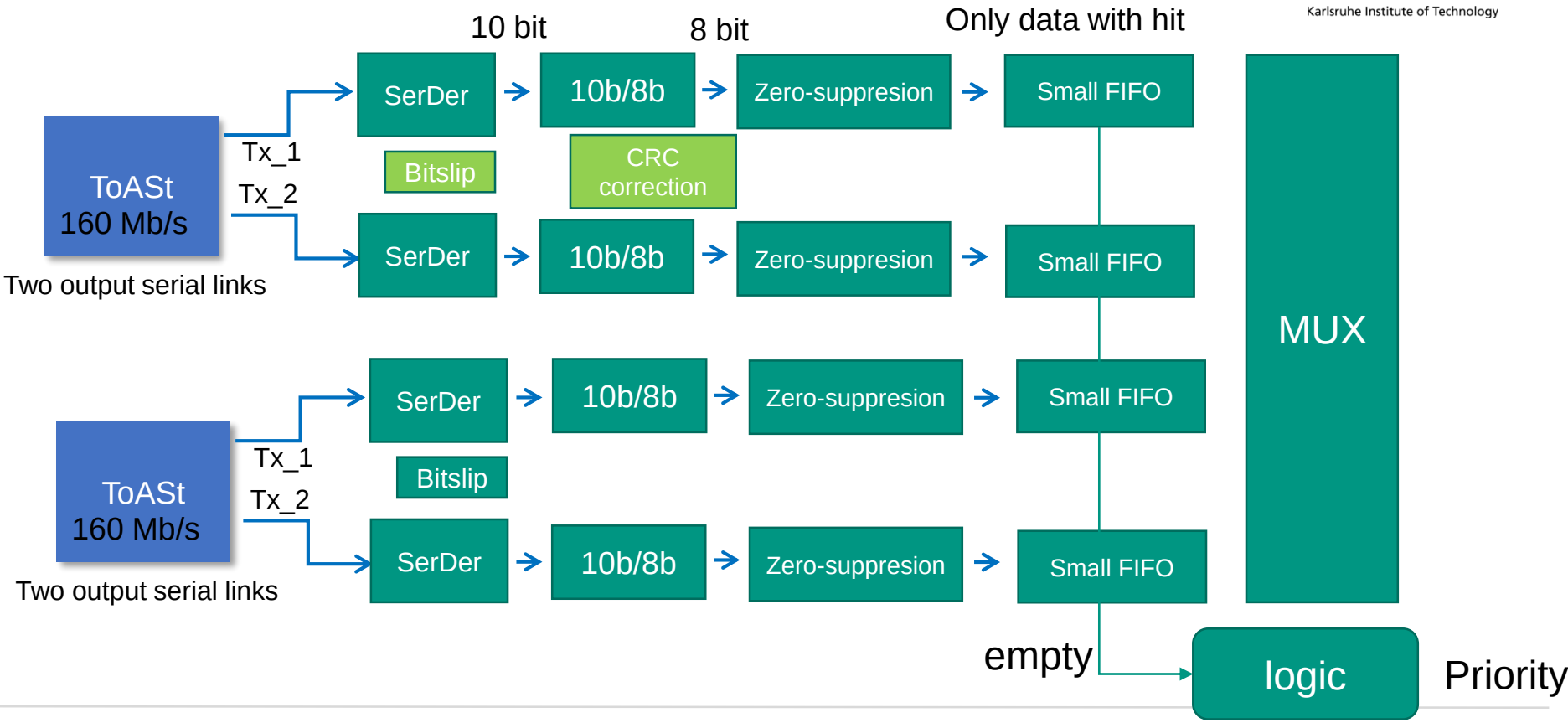


HIGH PRTIORITY

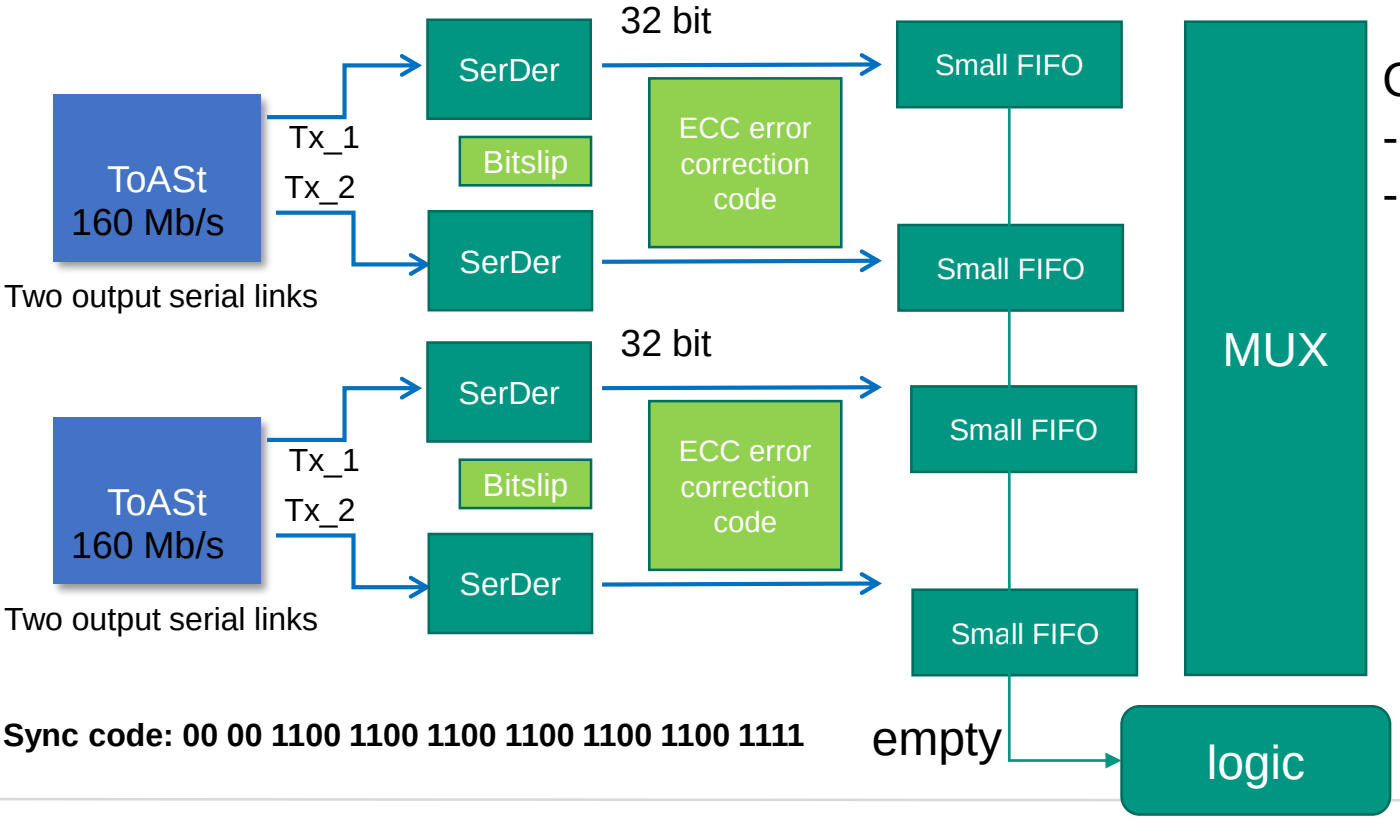
- Front-end interface (SerDes, bitslip, 8b/10b decoding)
- Intelligent multiplexer, only the active and working channels must be readout

We need the FPGA implementation of the E-port, for now (by CERN ?)

Module Data Concentrator (MDC) - ASIC



Module Data Concentrator (MDC) - ASIC



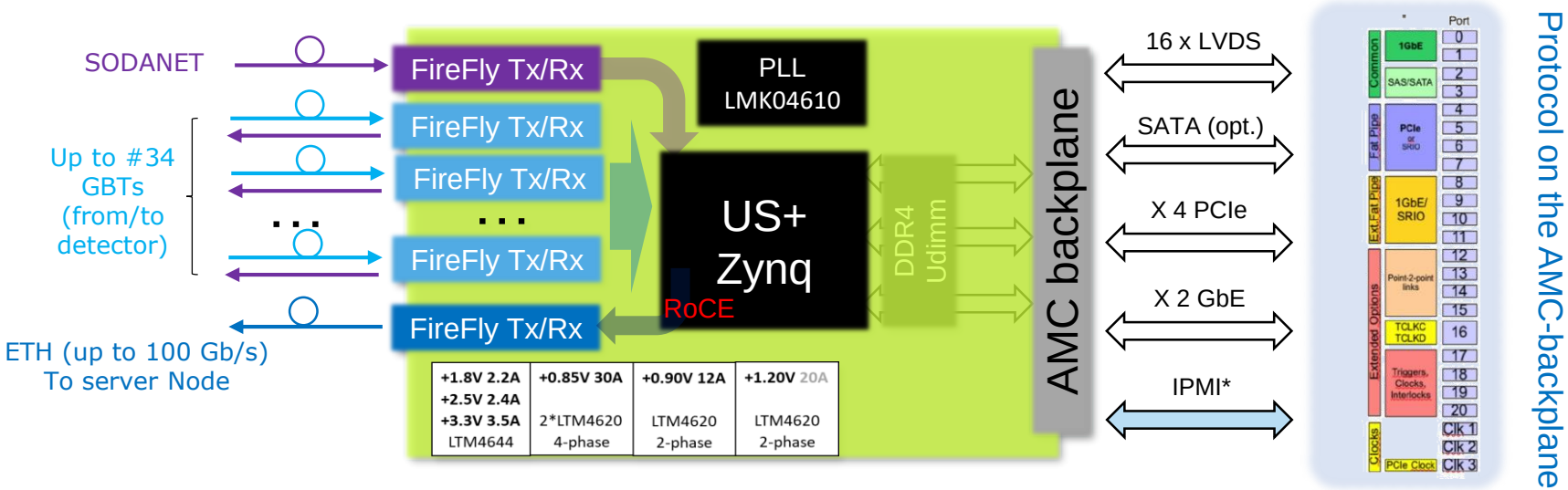
On case of:
- NO 8b/10b
- No zero-suppression

Sync code: 00 00 1100 1100 1100 1100 1100 1100 1111

Backup slides

Proposed DC-PANDA based on ZYNQ

Very-flexible, heterogenous and high-performance back-end

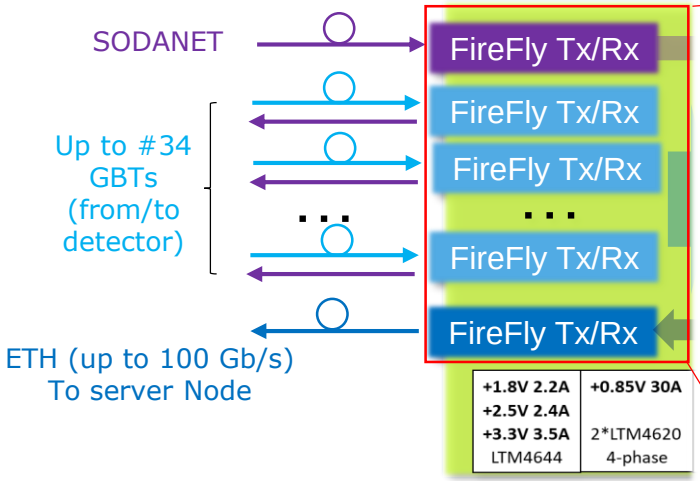


- Up to 60 optical links from/to GBTs still possible
- Up to 100 Gb/s ETH (upstream) + an additional 100Gb/s as spare
- Fully compilated AMC-backplane connections including 2 x GbE , 4 x lanes PCIe, 2x SATA and IPMI on ARM processors ➔ dramatic reduction of the necessary firmware (FPGA) for the implementation of the AMC protocols

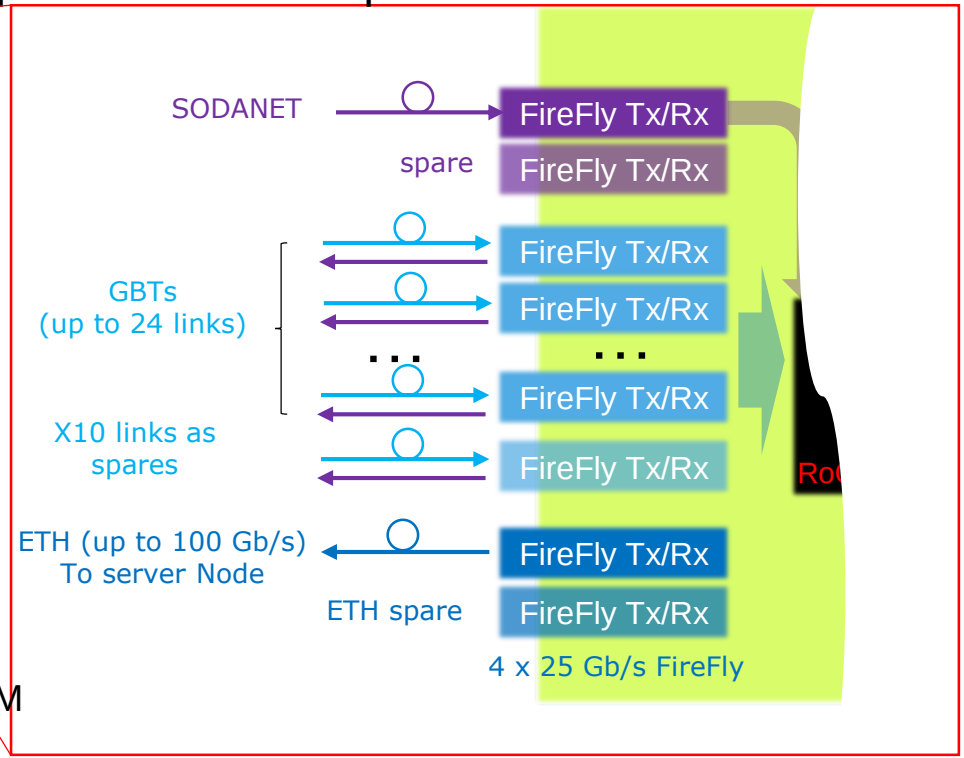
*Intelligent Plattform Management Interface
** Module Management Controller

Proposed MMB for MVD

Optical links - details



Optical fibers front-panel detail

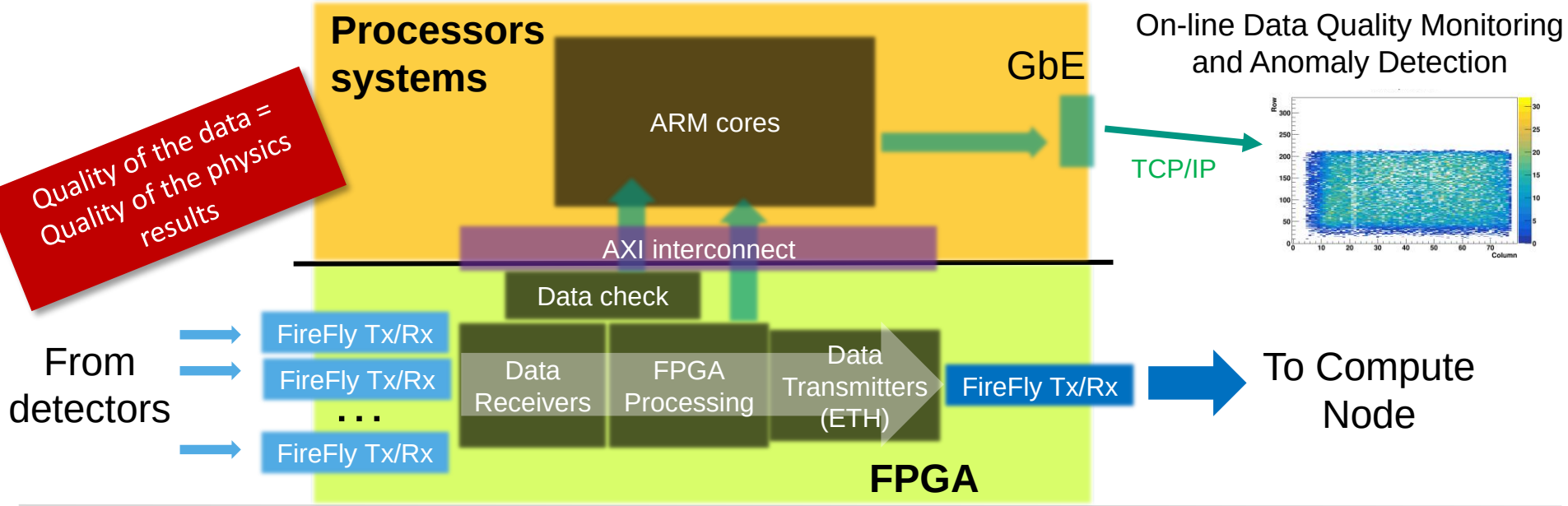


- Spares fibers
- Not used optical fibers in power-saving modes
- Dynamic reconfiguration of the transceivers by ARM processor and not by FPGA

MMB at the experimental area

Advantages of the ZYNQ – ARM processor for the MVD

- Data flow from the detector to compute node fully independent from the ARM processes
- ARM could process the incoming detector data without disturb the main data flow



Silicon Strip Detector

Readout architecture