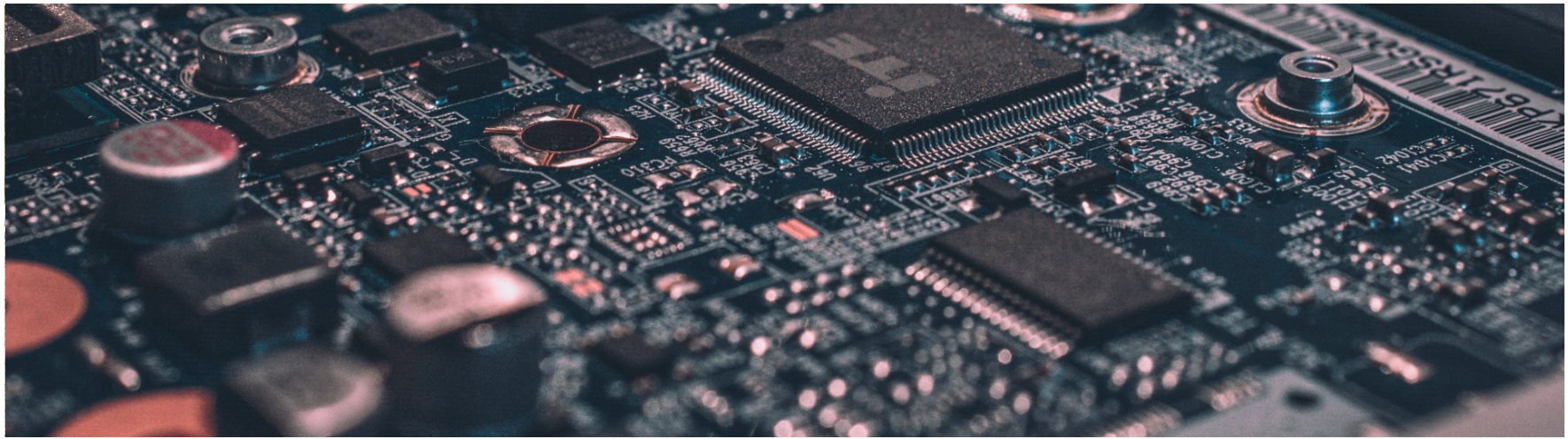
Karlsruhe Institute of Technology

# Development of a new generation of silicon detectors for particle physics experiment

**Ekaterina Trifonova**



# Outline

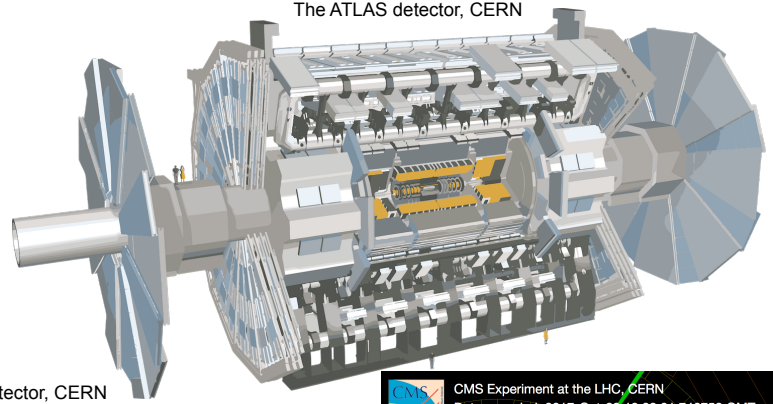
- Introduction to silicon detectors
  - Working principles
  - Sensor technologies
  - Recent developments
- Motivation for the research
  - Requirements of future pixelated detectors
- Latest development in silicon sensors
  - Low Gain Avalanche Diodes (LGADs)
  - Monolithic sensors

# Introduction to silicon detectors

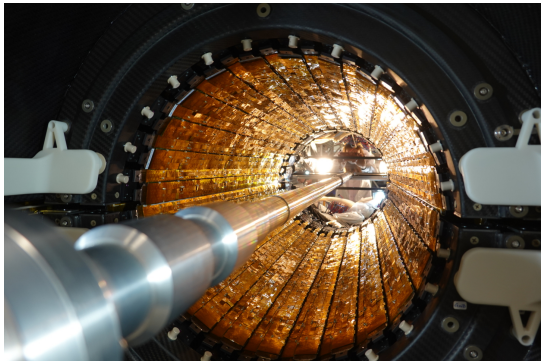
# Silicon detectors

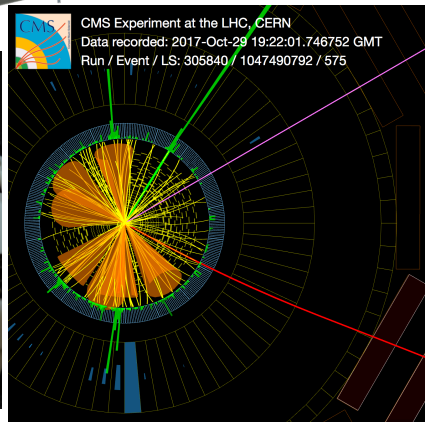
- Tracking detectors provide necessary information on the position and time of traversing particles
- The quality of the track reconstruction is crucial
- A widely used type of inner tracking detectors is a solid-state detector
- Silicon is today's material of choice for high-precision detectors and offers a high grade of engineering possibilities

The ATLAS detector, CERN



The ALICE detector, CERN



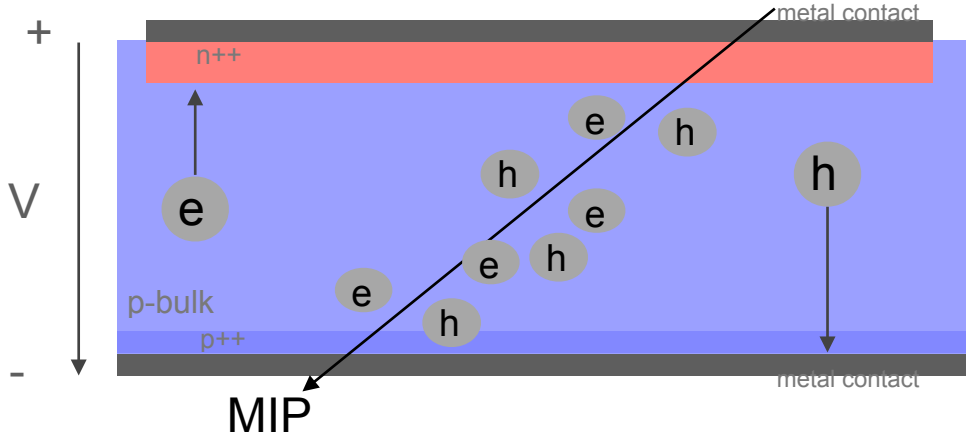



But how does silicon detector work?

* Illustration from CERN Document Server

# Detection mechanism of silicon sensor

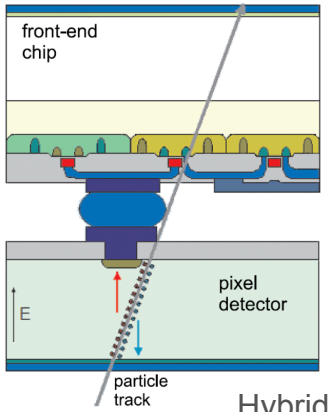
- Depletion region of p-n-junction works as detection region
- The traversing ionizing particle generates in the depleted bulk electron hole pairs which are then separated by the applied bias voltage
- Number of free charge carriers created by charge particle should be sufficient in order to create a detectable signal
- To get a more efficient detector reverse-bias is used




Cross-section of Si-detector penetrated by minimum ionising particle

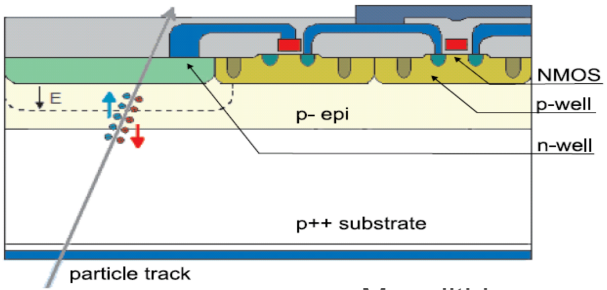
# Silicon sensor technologies

- Hybrid sensor where sensor and readout chip (ROC) are separated
- Allows to develop sensor and (ROC) separately
- Interconnection is done using bump-bonding or wire-bonding technics
- Challenge is to create reliable interconnection → expensive assembly




Hybrid sensor

- Monolithic sensor where read-out functionality is integrated into the sensor die
- Can be produced in large volumes in short production time
- A lot of different technologies, such as HV-CMOS, MAPS, DEPFET, SOI etc.



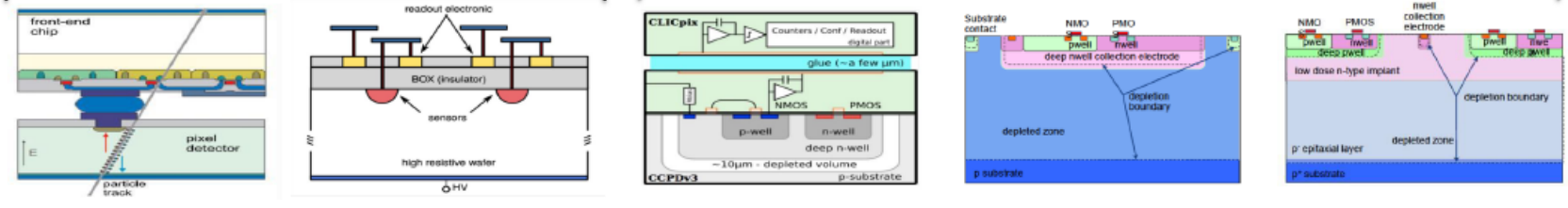

Monolithic sensor

# Recent silicon developments

*D. Contardo-IP2I Lyon CNRS/ IN2P3 (FCC-week, CERN, January 16-17 2020)*

**Hybrid design**
high $V_{dep}$ sensors bonded to separate ASIC

**CMOS Monolithic Active Pixels**
Readout grown on sensors



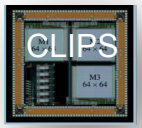

Planar/3D sensors finer pitch for resolution

HV/HR modified for rad. tol. + faster(precise time) & higher rate readout

3D Connection to ASIC, SoI TSV, CC glue

CMS Upgrade Phase 1 and 2

CLIC




TANGERINE


# Motivation for the research

# Request at future accelerators

| Facility | FCC-ee | ILC | CLIC |
|---|---|---|---|
| Spatial resolution [μm] | ~5 | <3 | <3 |
| Thickness of tracker material [μm] | ~100 | ~100 | ~100 |
| Hit rate [$10^6$ $s^{-1}$ $cm^{-2}$] | ~20 | ~0.2 | 1 |
| Power dissipation [$W/cm^2$] | 0.1-0.2 | 0.1 | 0.1 |
| Pixel size [$\mu m^2$] | 25 x 25 | 25 x 25 | 25 x 25 |
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High-accuracy 4D particle trackers with Resistive Silicon Detectors (AC-LGADs)
Roberta Arcidiacono, TWEPP 2021

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- High radiation tolerance → Hybrid pixel

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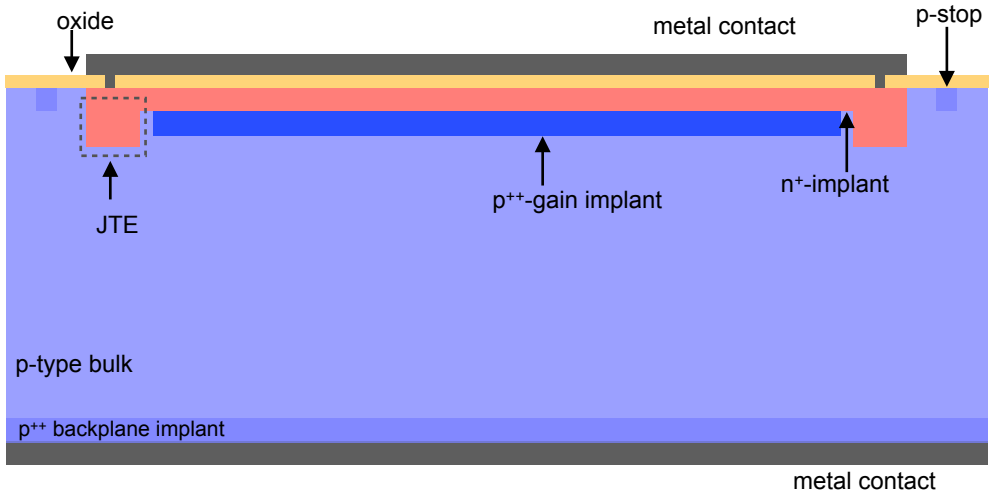
What can be next?

High-accuracy 4D particle trackers with Resistive Silicon Detectors (AC-LGADs)
Roberta Arcidiacono, TWEPP 2021

# Latest development in silicon sensors

# Low Gain Avalanche Diode (LGAD)

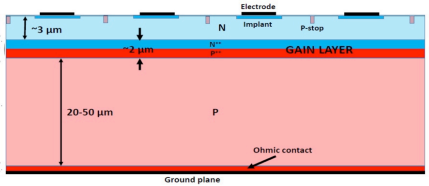
- Thin (<5 µm) and highly doped ($10^{16}$ $cm^{-3}$) multiplication (gain) layer
- High electric field in the multiplication layer
- LGADs have intrinsic modest internal gain (10-50)
- Time resolution < 30 ps
- Junction Termination Extension (JTE) is used between pixels to prevent premature breakdown and high electric field
- P-stop used as isolation between pixels
- Several LGAD-based sensors are under development




Cross-section of standard LGAD

# LGAD technologies overview

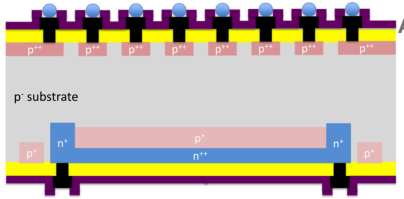
## "Deep Junction" LGAD (DJ-LGAD)




- Main idea is to bury the P-N junction
- Electric field is lower at the surface
  → conventional granularity
  → maintaining modest gain
  → breakdown voltage over 300 V
- But only simulation

*Dr. Simone M. Mazza - University of California Santa Cruz; 15° Trento Workshop (2020, Wien)*

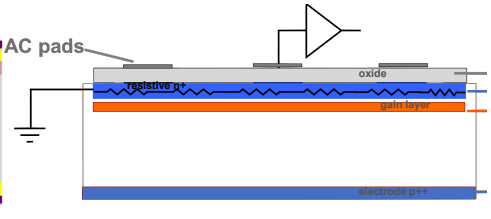
## Double Sided LGAD (DS-LGAD) or Inverted LGAD (i-LGAD)




- Main idea is to reverse position of the gain layer to decrease dead area and increase granularity
- Requires double-side diffusion, which is expensive and technologically difficult process

*M. Centis Vignali, Technology Development of LGADs at FBK,18/02/2020*

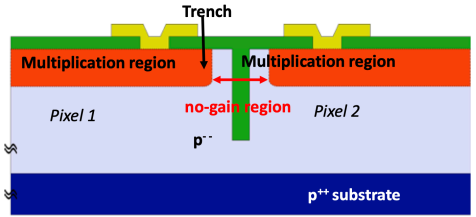
## Resistive AC coupling (RSD-LGAD)




- Main idea is to create multiplying junction using a resistive n+-layer
- No segmentation by inner structure, but by AC-coupled pads

*IEEE ELECTRON DEVICE LETTERS, VOL. 40, NO. 11, NOVEMBER 2019*

## Trench-Isolated LGADs (TI-LGAD)




- Main idea is to replace JTE and p-stop by a insolation trench
- Increasing of fill-factor, close to 100%

*M. G. Paternoster et al. Novel Strategies for Fine-Segmented LGA's; HSTD12, Hiroshima, Japan.*

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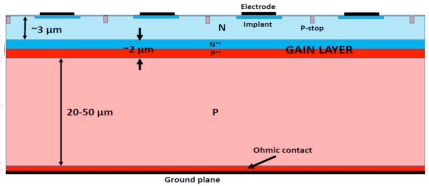


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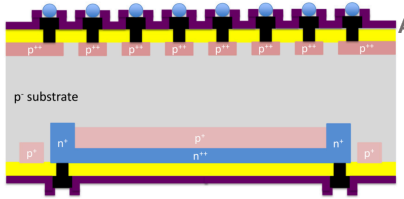


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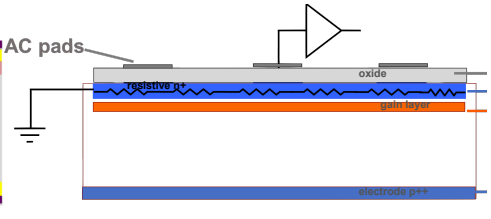


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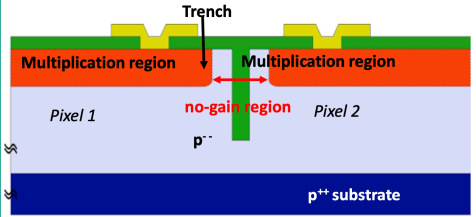


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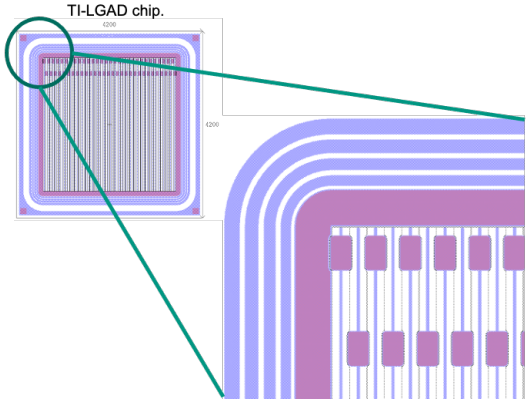
- Increasing of fill-factor, close to 100%

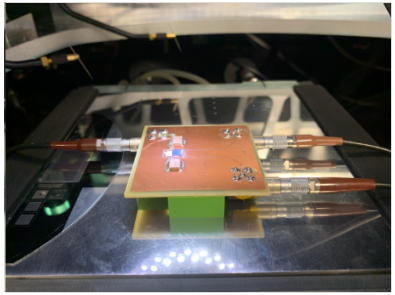
Produced at FBK, designed and studied at KIT

*M. G. Paternoster et al. Novel Strategies for Fine-Segmented LGA's; HSTD12, Hiroshima, Japan.*

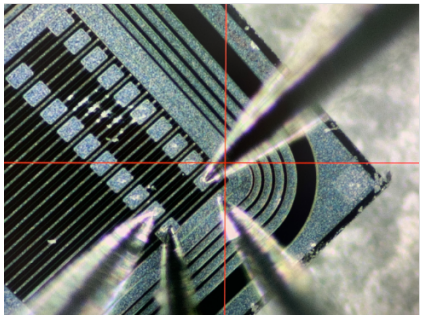
# Characterization of Ti-LGAD at IPE

- First Ti-LGAD produced by FBK has been delivered and characterized at KIT
- Designed sensors with different pixel pitches (50 µm and 100 µm), different numbers of tranches (one or two). Also types of gain doping, trenches and contacts varied
- Equipment of ETP was used to perform IV and CV measurements
- First PCB was created to improve grounding of microstrips
- Excellent result: low leakage current is bellow 10 pA, low capacitance and gain activation is already around 30 V
- New PCB for TCT characterization was developed and currently is in a production



First PCB



Probing with needs at EKP

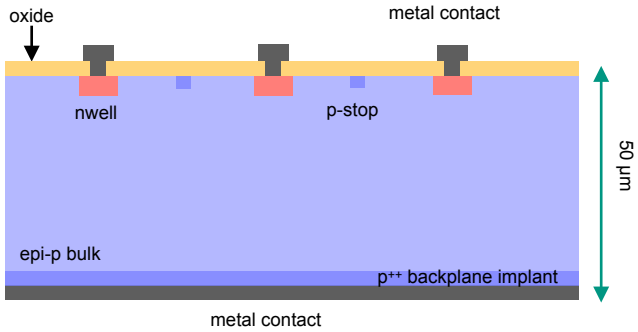
This work was done by Johannes Deutsch as part of Master Thesis

# Monolithic SiGe BiCMOS

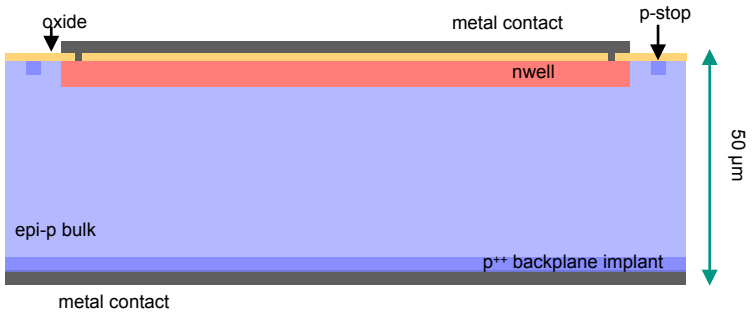
- Proposed by Dr. Michele Caselle, design belongs to Monolithic Active Pixel Sensor (MAPS)
- Produced by The Leibniz Institute for High Performance Microelectronics (IHP) in IHP SG13G2 technology
- Readout electronic was developed by Alexander Elsenhans

- The main feature of the design was to dramatically reduce the size of collection node (10 µm by 10 µm) and pixel pitch of the sensor to 100 µm
  - reduce the time collection
  - test charge sharing effect

- Another sensor with 230 µm pixel pitch and 198 µm collection node was developed by Prof. Ivan Peric



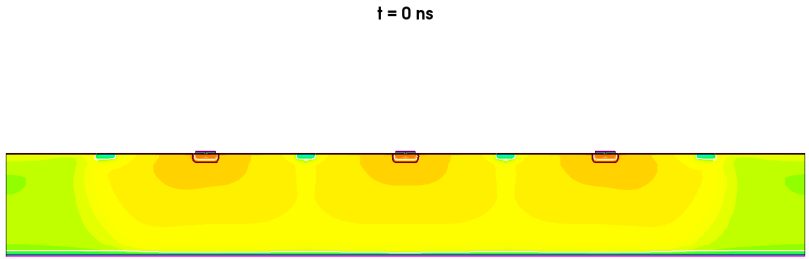

Cross-section of “small” SiGe sensor

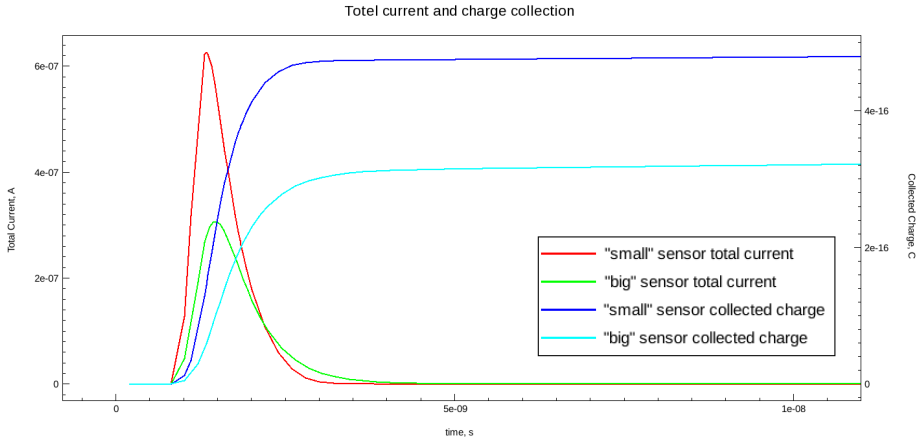



Cross-section of “big” SiGe sensor

# “Small” SiGe sensor. Beam simulation

- Beam simulation was done using TCAD Heavy Ion Model
- Bais voltage is - 100 V




Based on simulation results the structures have been submitted to IHP for the production

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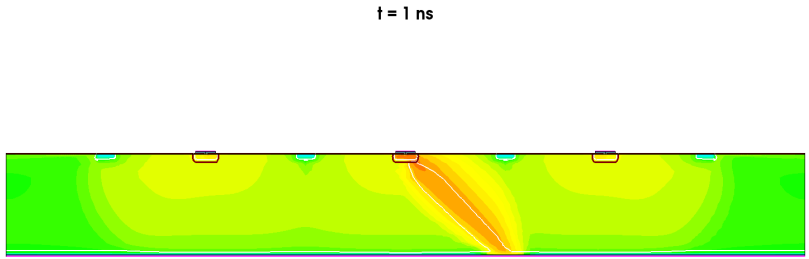


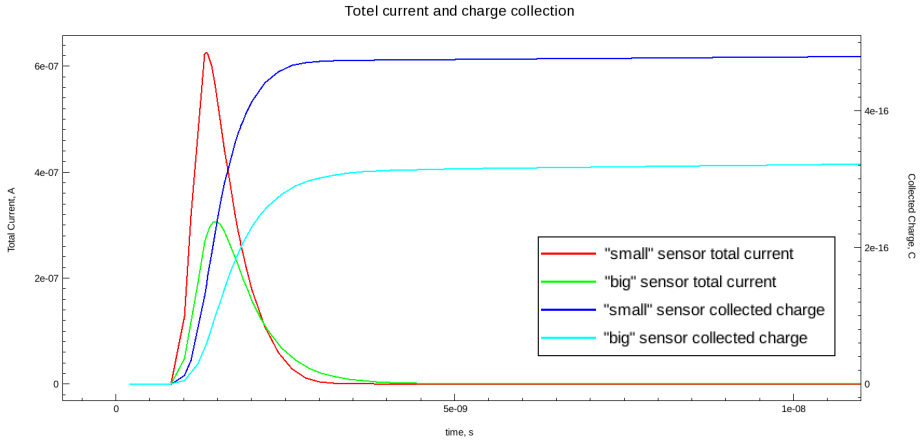


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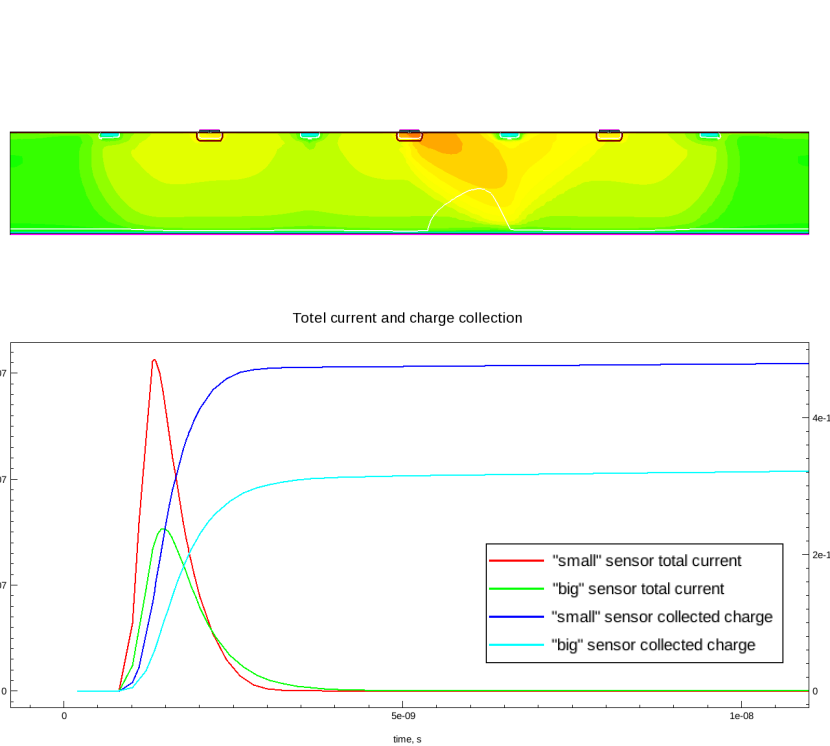

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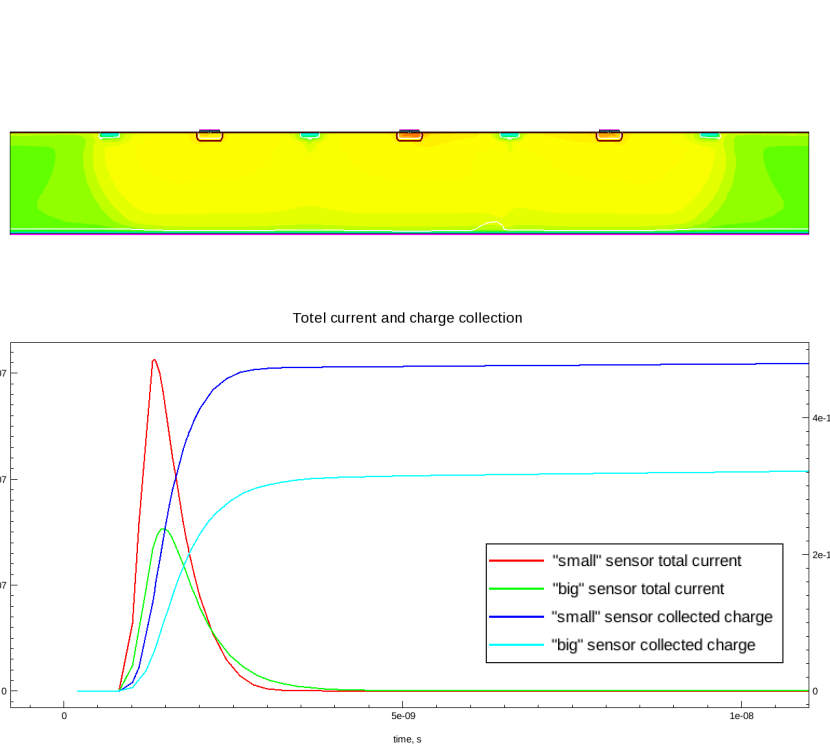

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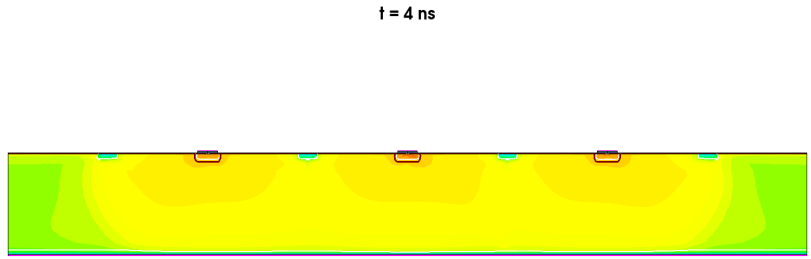


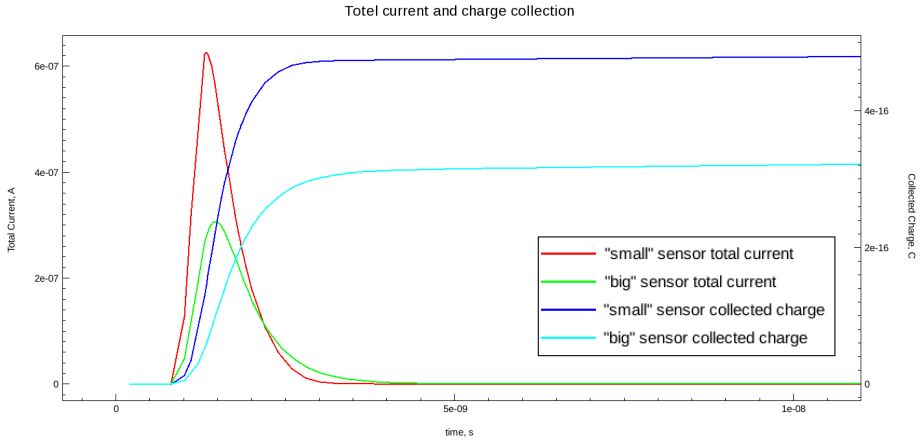


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- Charge collection < 5 ns

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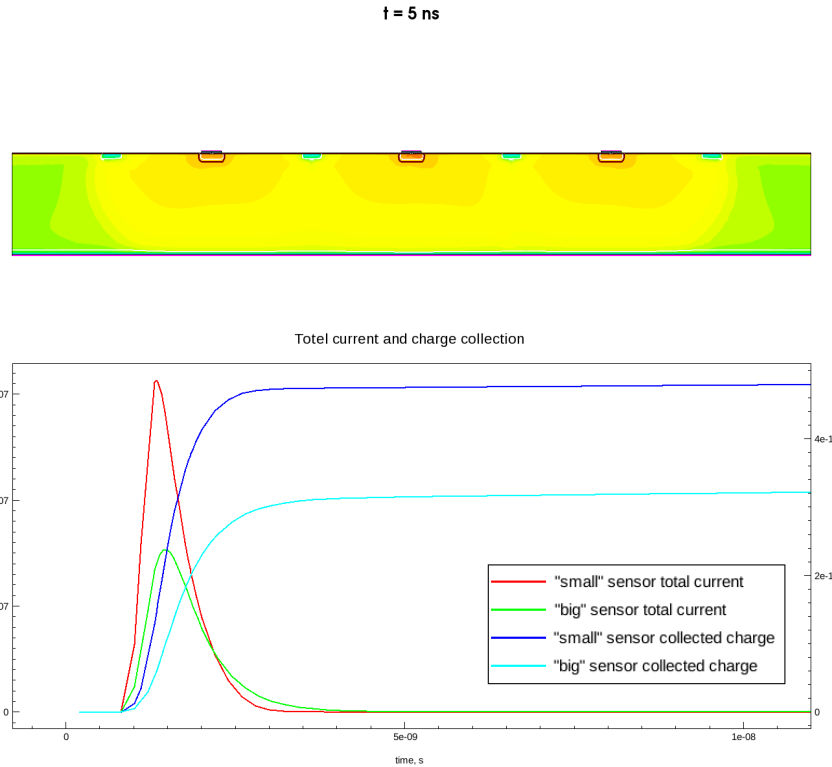

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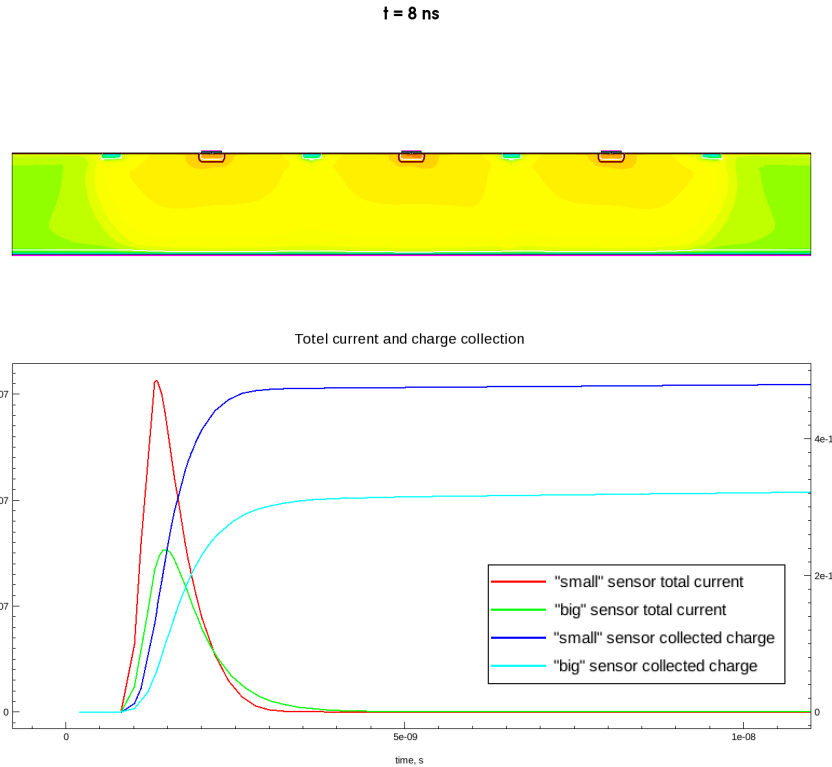
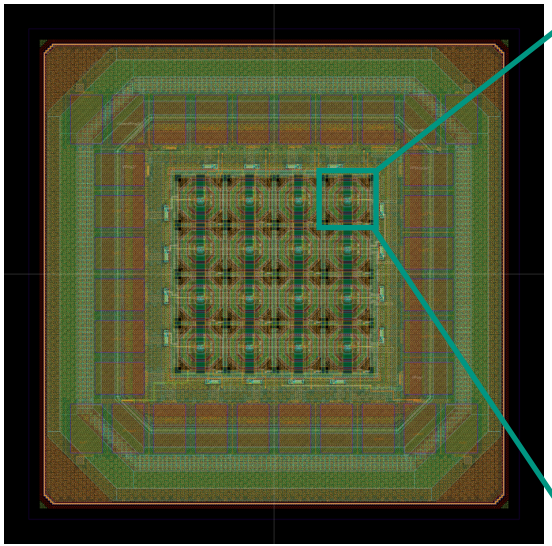
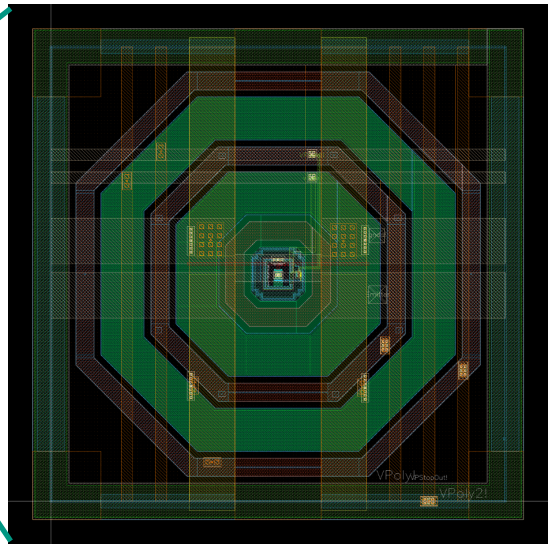


# “ABC-SiGe” ASIC layout

- Total size of chip is 1µm x 1µm
- Matrix consists of 4 x 4 pixels
- Pixels are surrounded by n-well guarding ring which is grounded and electronics are placed within
- Then there are 2 additional guarding rings, both connected to individual pads
- The pads for the negative HV for the substrate are placed in the corners
- The charge collection node is surrounded by two poly-rings and a p stop
- Waiting for delivery
- Plan to study charge sharing and impact angle of particle



Chip layout

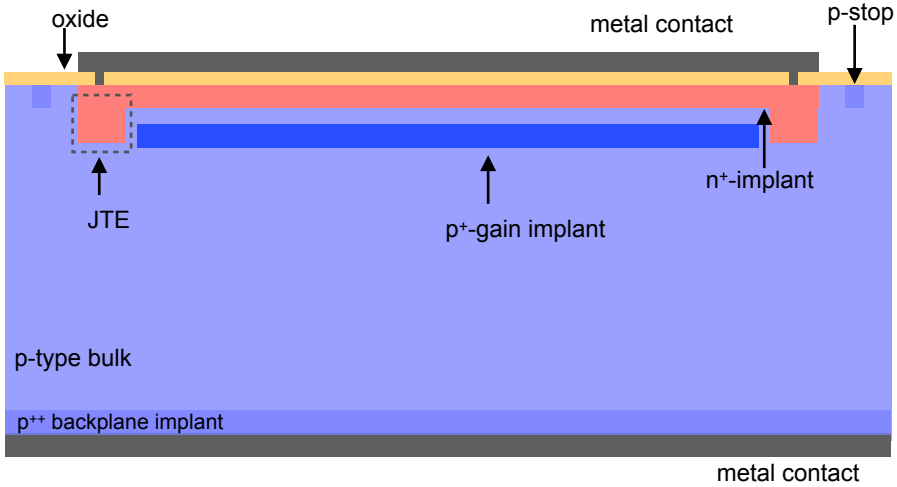


One pixel layout

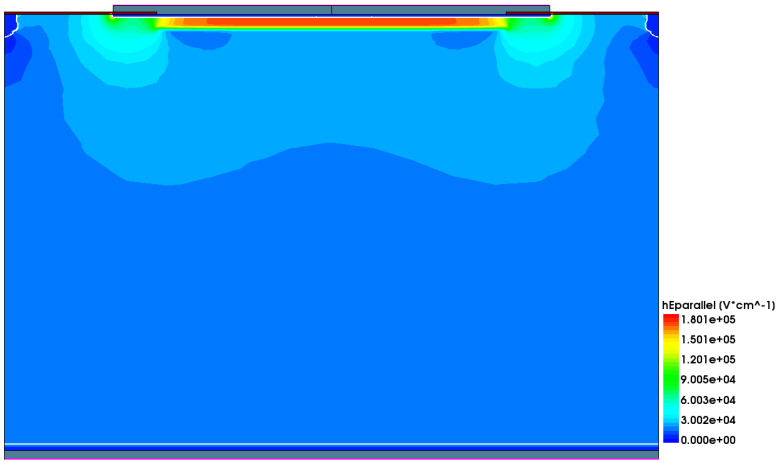
# Development within Tangerine project

- Main goal is to establish availability of sensors with high spatial (20μm) and time resolution (20 ps) for charged particles
- We are targeting:
  - pixel pitch 25 x 25 $\mu m^2$
  - time resolution < 30 ps
  - charge sharing → to improve the spatial resolution over the binary resolution, but also to improve the time resolution
  - possibility to detect the impact angle of the track on the sensor
- Main concept can be presented in 3 steps
  - 1 - to design sensor with internal gain → wafer with gain layer is needed
  - 2 - to implement analog part of electronic on sensor → SiGe technology electronic at IHP
  - 3 - to connect it to digital part of readout → AC-coupled sensor with high density CMOS technology, FDSOI 22 nm or 28 nm TSMC

# Development of LGADs in HVCMOS technology




Cross-section of LGAD in HVCMOS




Electric field of LGAD in HVCMOS

- Using standard HVCMOS dopings and substrates in TSI technology
- Investigation of gain layer placement and doping concentration
- Next step is beam investigation

Work performs together with Prof. Ivan Peric

# Conclusion

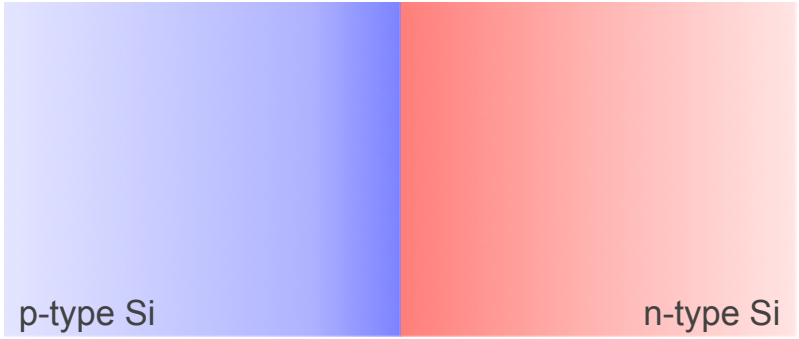
- Silicon is today's material of choice for high-precision detectors and offers a high grade of engineering possibilities
- Increasing requirements push sensors development for searching for new technologies
- Low Gain Avalanche Diode is the promising candidate for High Energy Physics, where Ti-LGAD already shows remarkable results
- One of the most attractive sensor technology is Monolithic
- Future for the silicon sensors is develop Monolithic LGAD

Thank you for attention

# Backup slides

# Working principle

- The working principle of a detector based on silicon is adapted from creating a p-n- junction



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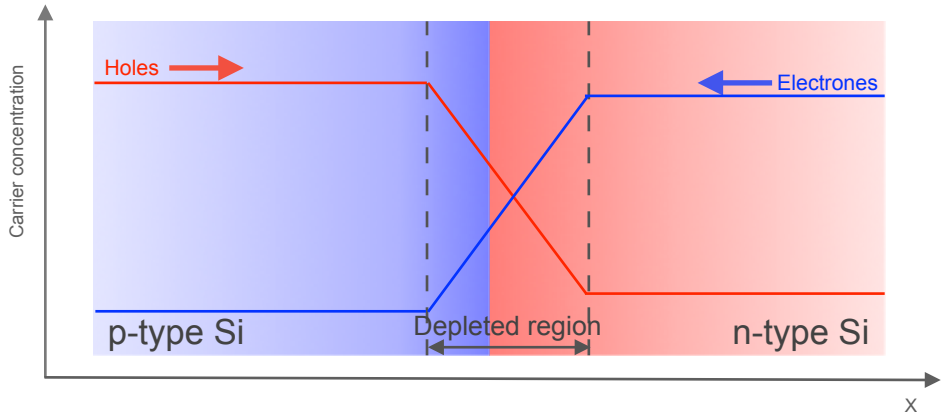

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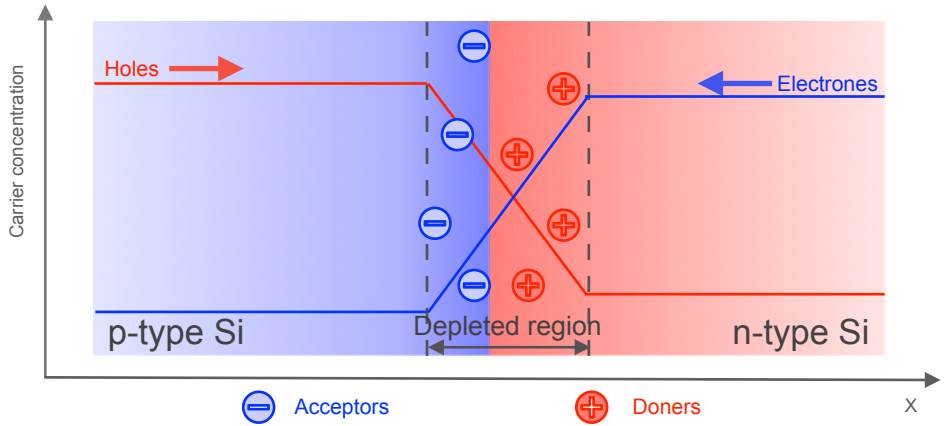
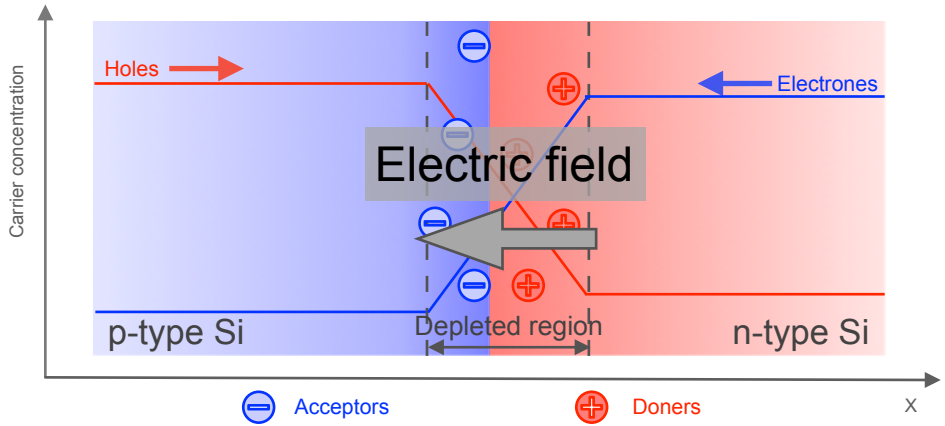


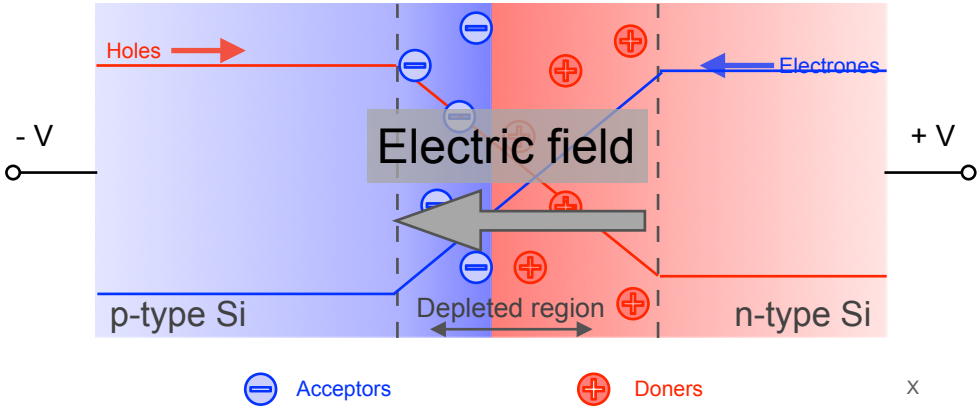
# Working principle

- The working principle of a detector based on silicon is adapted from creating a p-n- junction
- The described p-n-junction or more precisely the depleted region at the junction now already can serve as a particle detector.



# Working principle

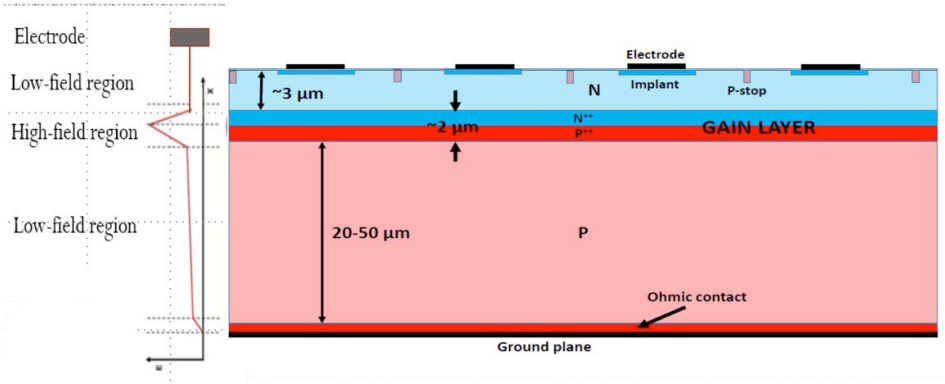
- The working principle of a detector based on silicon is adapted from creating a p-n-junction
- The described p-n-junction or more precisely the depleted region at the junction now already can serve as a particle detector.
- To get a more efficient detector, an outer voltage Vbias can be applied to the p-n-junction leading to a non-equilibrium state.



# “Deep Junction” LGAD (DJ-LGAD)

**Main idea** is to bury the P-N junction so that fields are low at the surface, allowing conventional granularity + to avoid high field near the electrodes while maintaining modest gain.

- High field region with multiplication ~5μm deep
- Velocity is saturated in the low field regions (P and N)
- Stable gain up to 15
- 8% gain variation over 30 μm pitch pads
- Fast rise time (100ps)
- Full charge collection within 1 ns
- Breakdown voltage over 300V



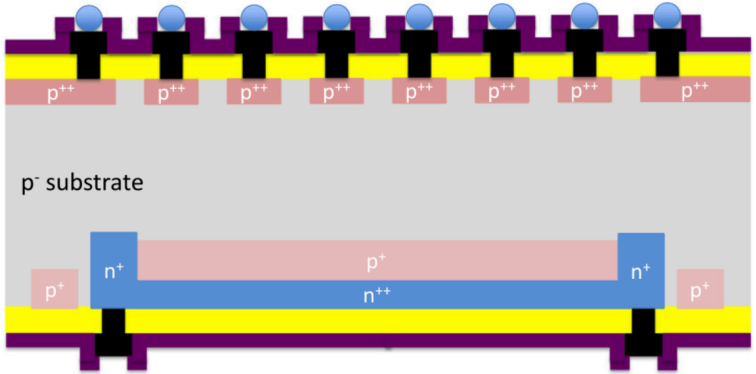

(TCAD simulation result)

*Dr. Simone M. Mazza - University of California Santa Cruz; 15° Trento Workshop (2020, Wien)*

# Double Sided or Inverted LGAD

**Main idea** is to reverse position of the gain layer to decrease dead area and increase granularity.

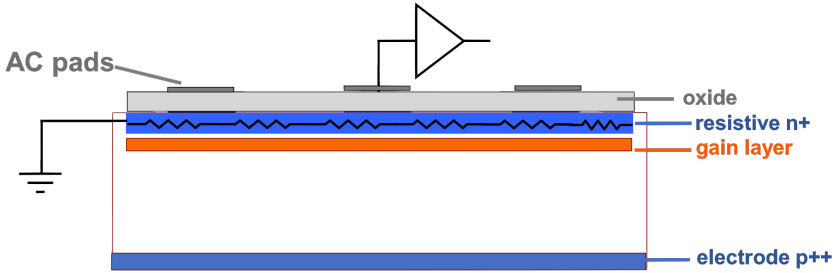
- High field region with multiplication ~5μm deep
- Continuous gain area in the active region ⇒ 100% fill factor Double sided process
- Active thickness is the wafer thickness
- Readout side is ohmic
- Design not optimal for timing applications
- Readout side separated from LGAD side ⇒ no restrictions on channel dimensions




*M. Centis Vignali, Technology Development of LGADs at FBK,18/02/2020*
*G.-F. Dalla Betta et al. / Nuclear Instruments and Methods in Physics Research A 796 (2015) 154–157156*

# Resistive AC coupling (RSD-LGAD)

- 100 % fill-factor: unsegmented gain layer, which spreads throughout all the sensor area
- AC coupling: the readout segmentation is obtained at the level of the AC metal pads
- High-granularity: no JTE and p-stop are present between pixels
- Excellent time resolution: gain layer provides signal multiplication
- Large signal and low noise: It provides larger signals while keep the same noise level like standard pixel sensor or avoiding at the same time the additional noise contribution

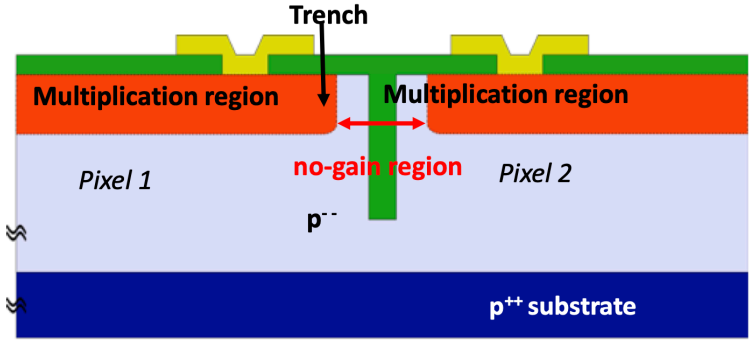


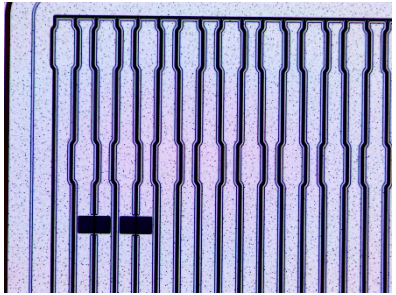

*M. Mandurrino et al., "Demonstration of 200-, 100-, and 50- micron Pitch Resistive AC-Coupled Silicon Detectors (RSD) With 100% Fill-Factor for 4D Particle Tracking," in IEEE Electron Device Letters, vol. 40, no. 11, pp. 1780-1783, Nov. 2019.*

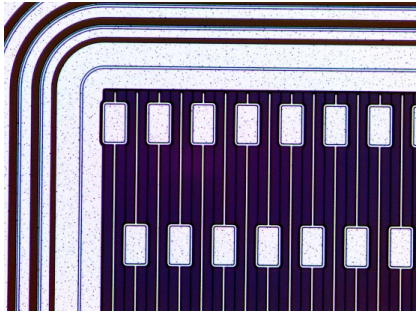
# Trench-Isolated LGADs

**Main idea** is to replace JTE and p-stop by a single trench.

- High field region with multiplication ~5µm deep
- Trenches act as a drift/diffusion barrier for electrons and isolate the pixels
- The trenches are a few microns deep and < 1µm wide
- Filled with Silicon Oxide
- The fabrication process of trenches is compatible with the standard LGAD process flow.

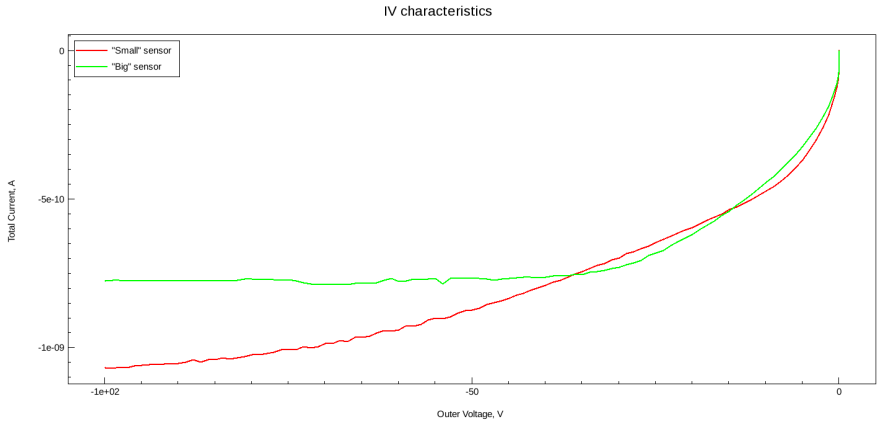


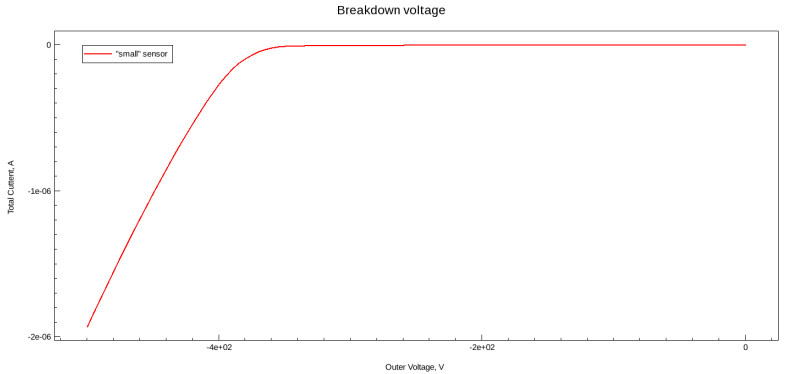





*M. G. Paternoster et al. Novel Strategies for Fine-Segmented LGA's; HSTD12, Hiroshima, Japan.*

# “Small” and “big” SiGe

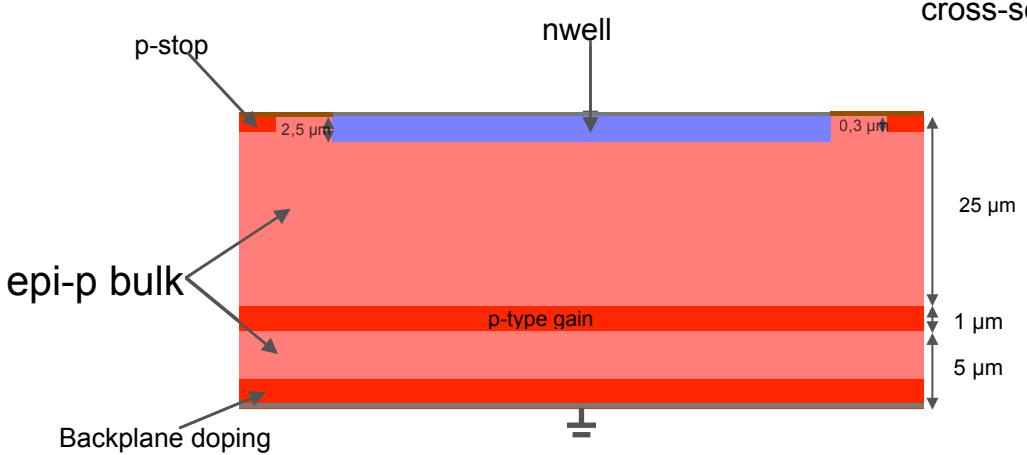


# SiGe LGAD development

- Develop together with University of Genève
- Main idea is to place gain layer to the bottom of the structure to increase holes collection
- Very thin structure
- Not inverted LGAD
- Gain layer investigation was made

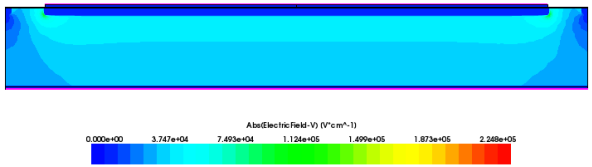
Sensor cross-section



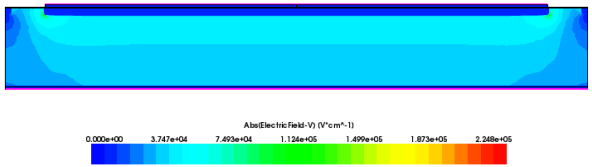
# SiGe LGAD. Gain investigation

- Investigated structures have gain layers in a range from $10^{14}$ $cm^{-3}$, to $10^{17}$ $cm^{-3}$, and structure without gain
- Structures with gain doping $10^{16}$ $cm^{-3}$ and $10^{17}$ $cm^{-3}$ ware not depleted before breakdown at - 320 V

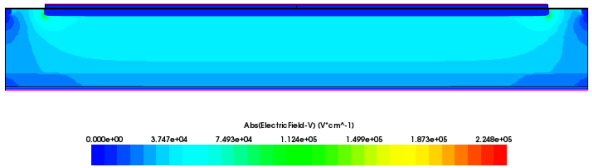
No gain



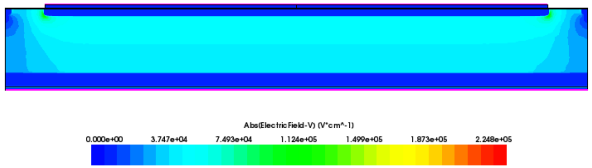

gain concentration $10^{14}$ $cm^{-3}$



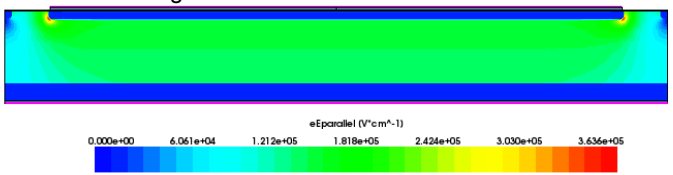

gain concentration $10^{15}$ $cm^{-3}$




gain concentration $10^{16}$ $cm^{-3}$




gain concentration $10^{17}$ $cm^{-3}$



# SiGe LGAD. Gain investigation

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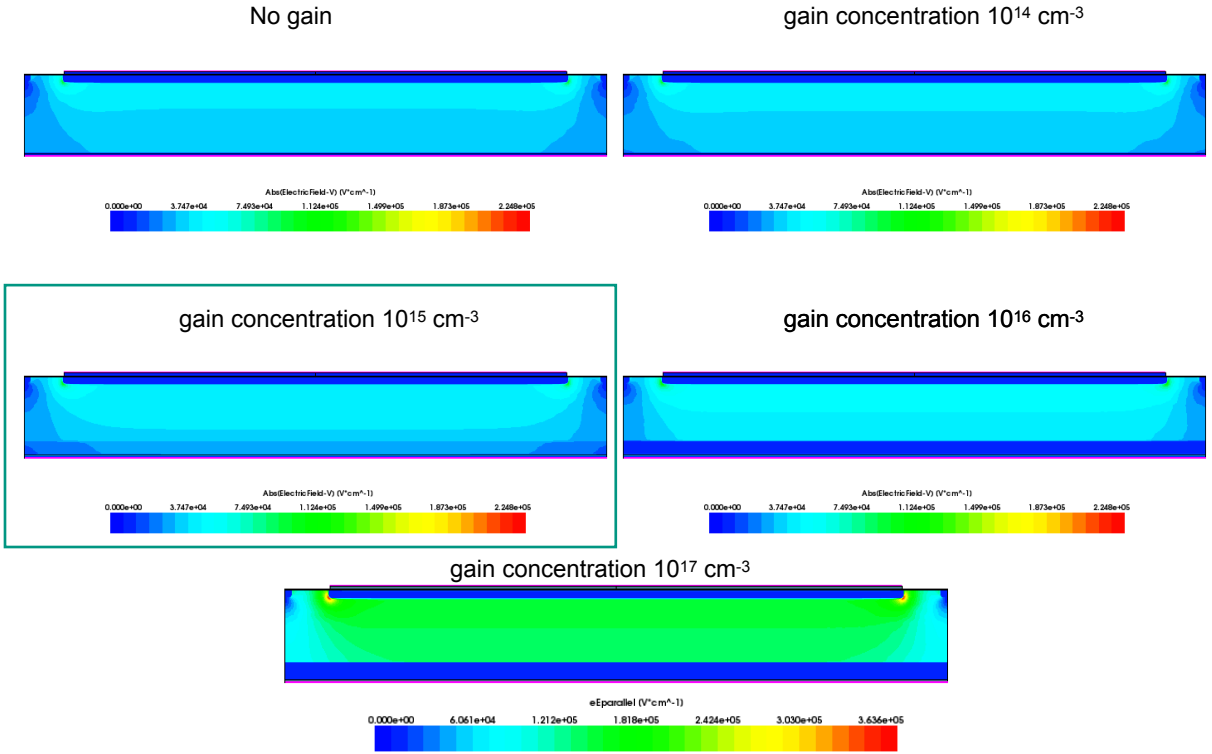
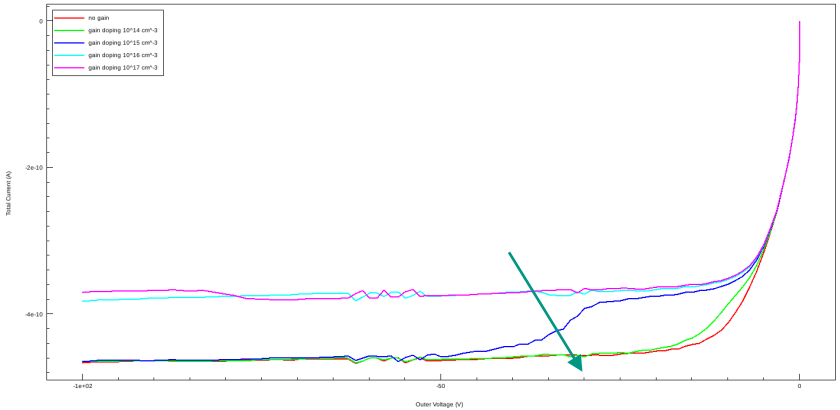
- Structures with gain doping $10^{16}$ $cm^{-3}$ and $10^{17}$ $cm^{-3}$ ware not depleted before breakdown at - 320 V
- More detailed investigation of structure with gain doping $10^{15}$ $cm^{-3}$ due to non-zero electric field underneath gain layer



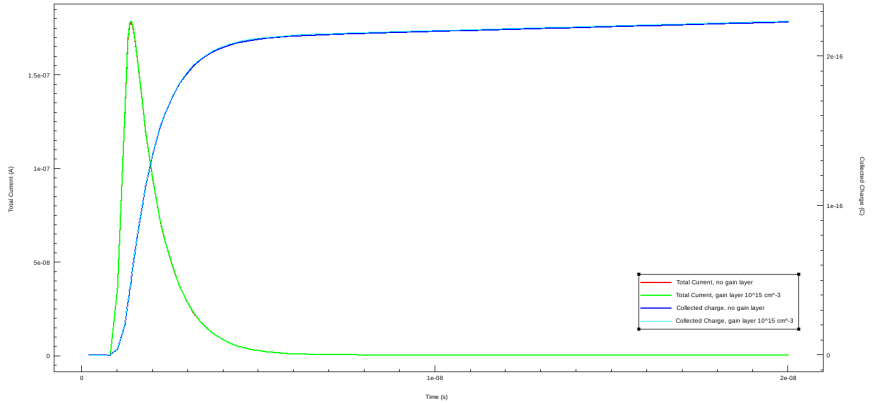
# SiGe LGAD with gain layer doping $10^{15}$ $cm^{-3}$

IV characteristic




- Gain activation at “step” -30 V looks promising

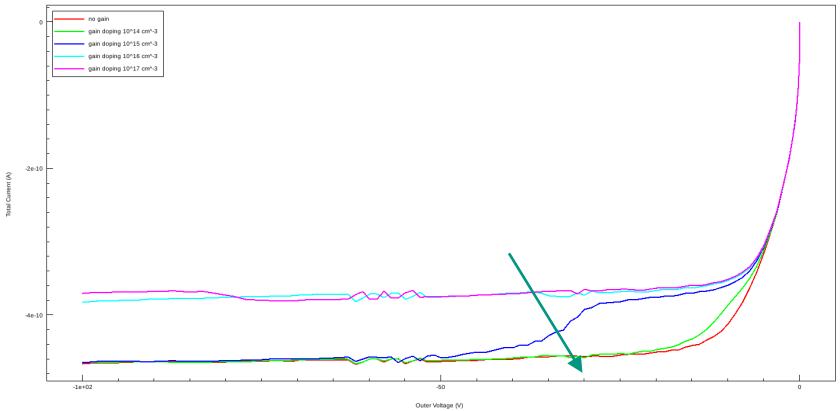
Charge collection



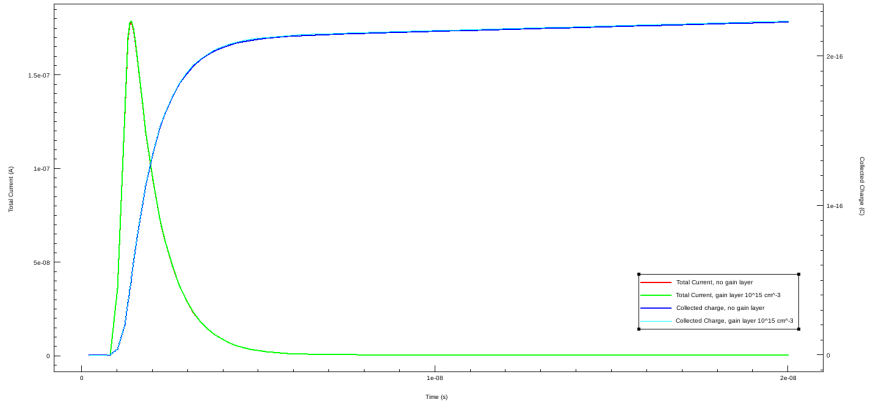

- Charge collection investigation using beam simulation
- Diode shows almost full charge collection of elections in 10 ns

# SiGe LGAD with gain layer doping $10^{15}$ $cm^{-3}$

IV characteristic




Charge collection



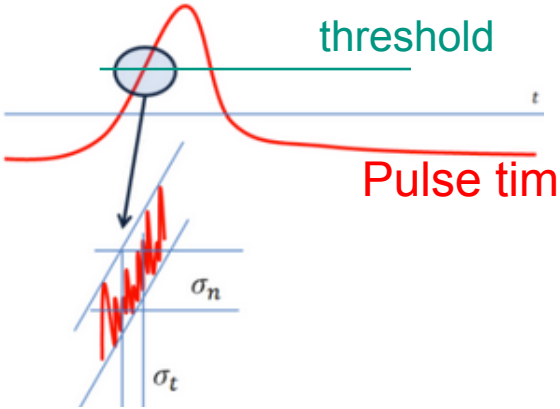

- Gain activation at “step” -30 V looks promising

- Charge collection investigation using beam simulation
- Diode shows almost full charge collection of elections in 10 ns

Result: no gain in charge collection

# Temporal resolution and noise

- The time resolution depends mostly on the amplifier performance




$$\sigma_t = \frac{\sigma_V}{\frac{dV}{dt}} \cong \frac{t_{rise}}{\frac{Q}{ENC}} = \boxed{\frac{t_{rise}}{Signal/Noise}}$$

We need large and short signals

- Need large dV/dt → need internal gain (sensor)
- Need an ultra-fast, low noise, low power-consumption electronics with fast rise time and small capacitance

- ***Our solution***: High $f_T$, single transistor preamplifier SiGe HBT technology IHP SG13G2 130nm
- Large $g_m/I_D$ compared to CMOS technology → **low-noise** and potentially **low-power** consumption
- **High** Transit frequency $f_T$ = 800 GHz (in SG13G3) → **fast rise** time and **small capacitance**