Karlsruher Institut für Technologie

Institut für Technik der Informationsverarbeitung

ITIV

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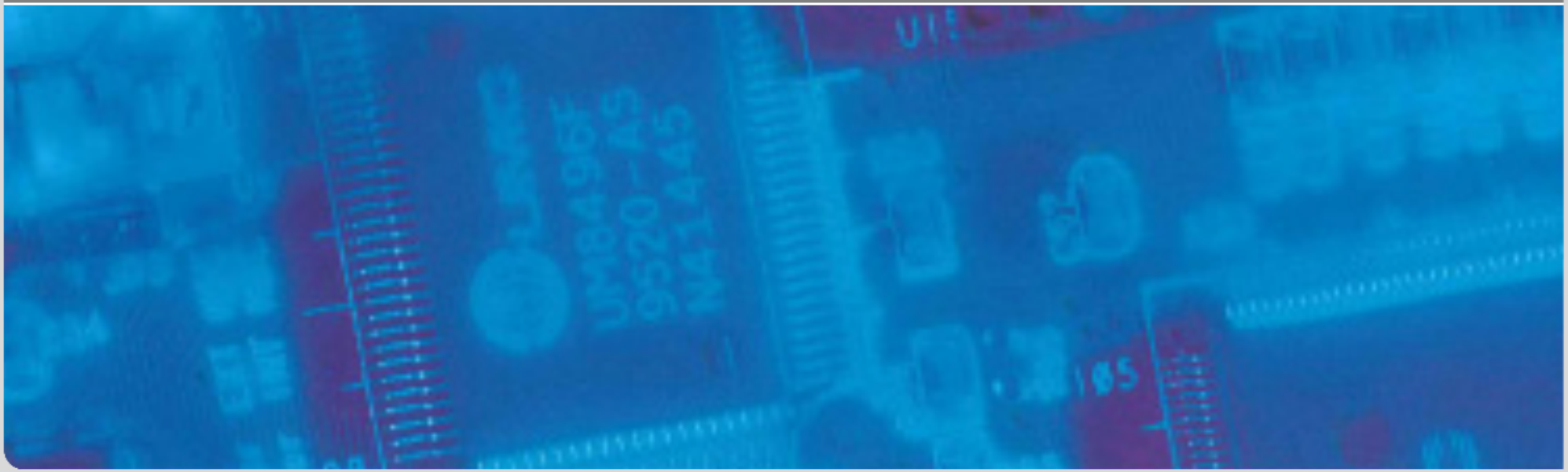
FPGA-based High-speed Signal Processing

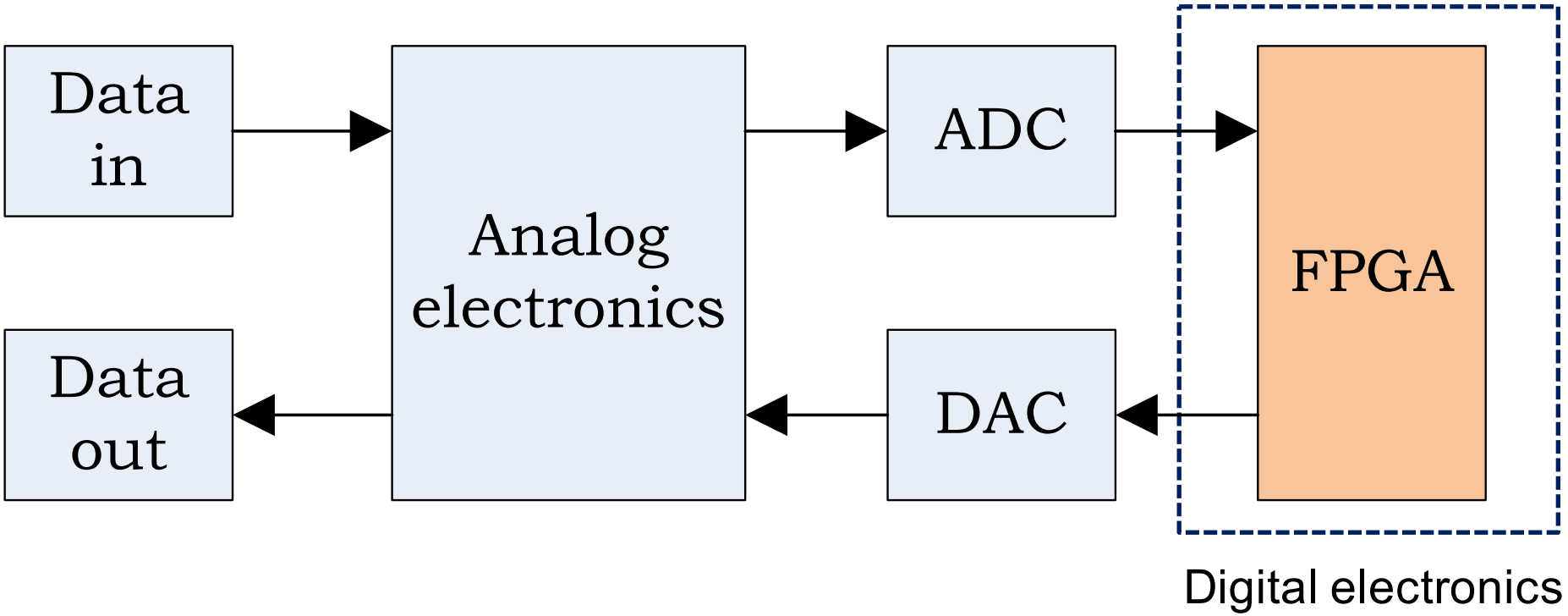
Shalina Percy Delicia Figuli, M.Tech

Institut für Technik der Informationsverarbeitung (ITIV)



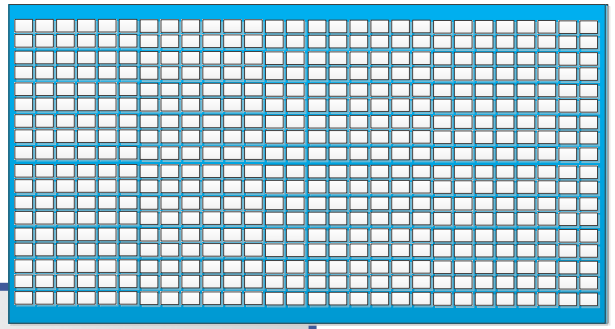
Motivation

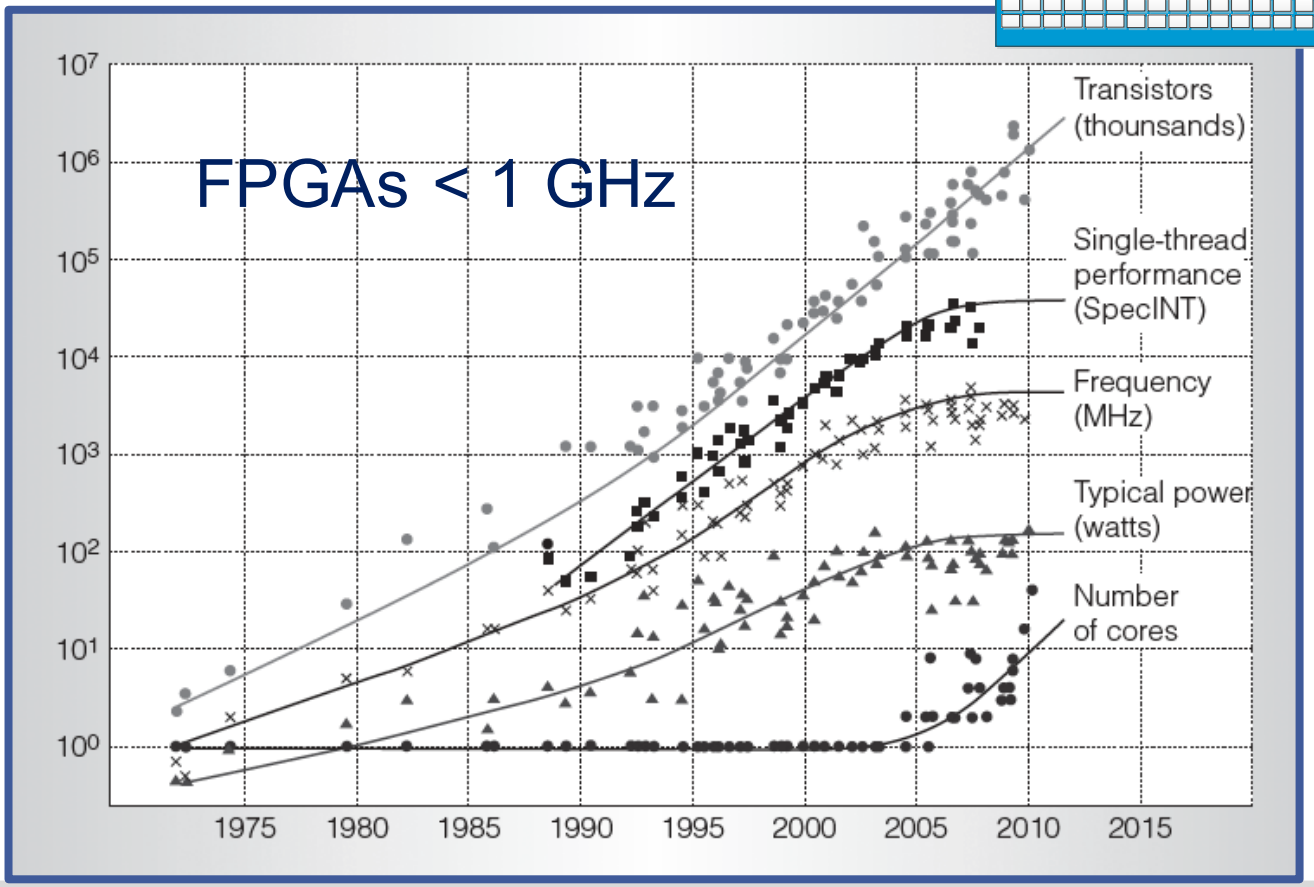
- Software Defined Ratio



Motivation

- Software Defined Ratio
- Frequency wall

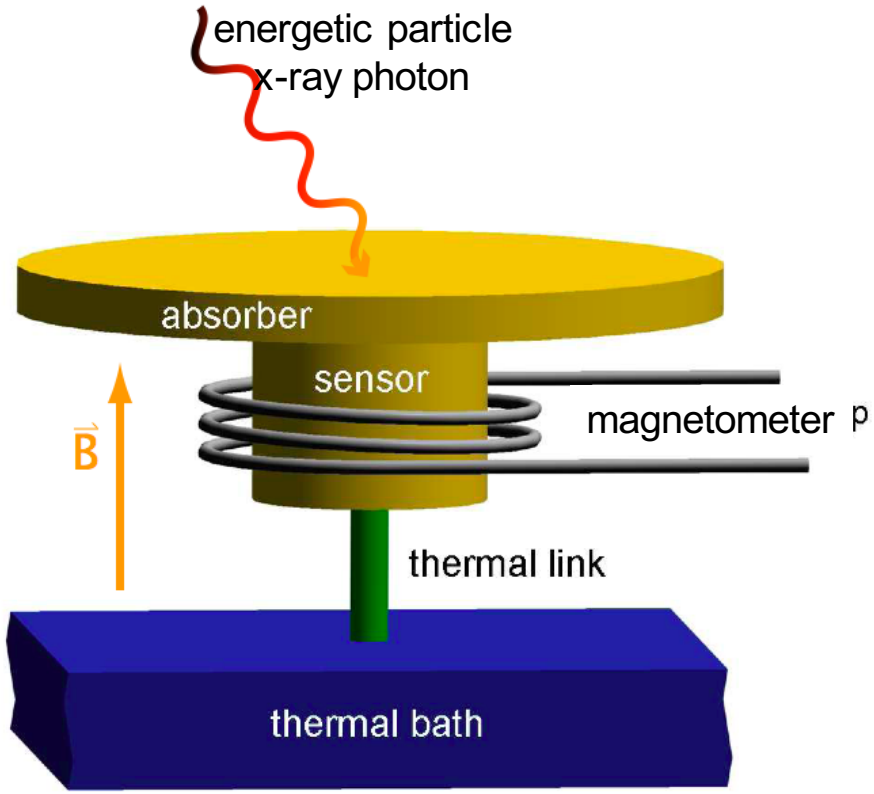




Contents

- Motivation
- Channelization
  - Combined FFT
- Transmission Chain
  - Frequency-domain
- Performance optimization
  - Modulator
  - Forward Error Correction (FEC)
- Summary

Metallic Magnetic Calorimeter (MMC)



massive particle absorber

paramagnetic or superconducting temperature sensor

operation at low temperatures

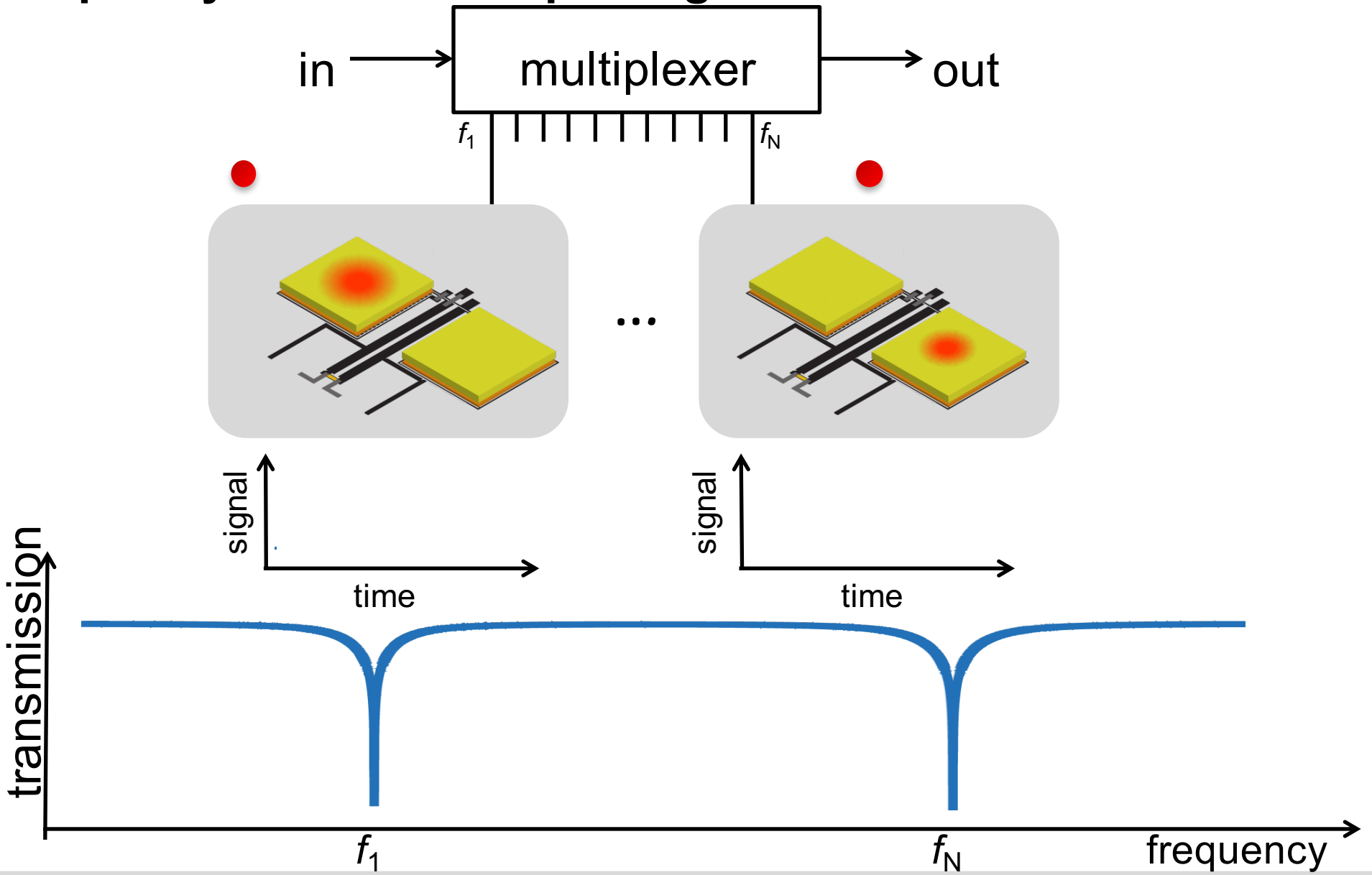
- small heat capacity
- low thermal noise
- large temperature change

no power dissipation in the sensor

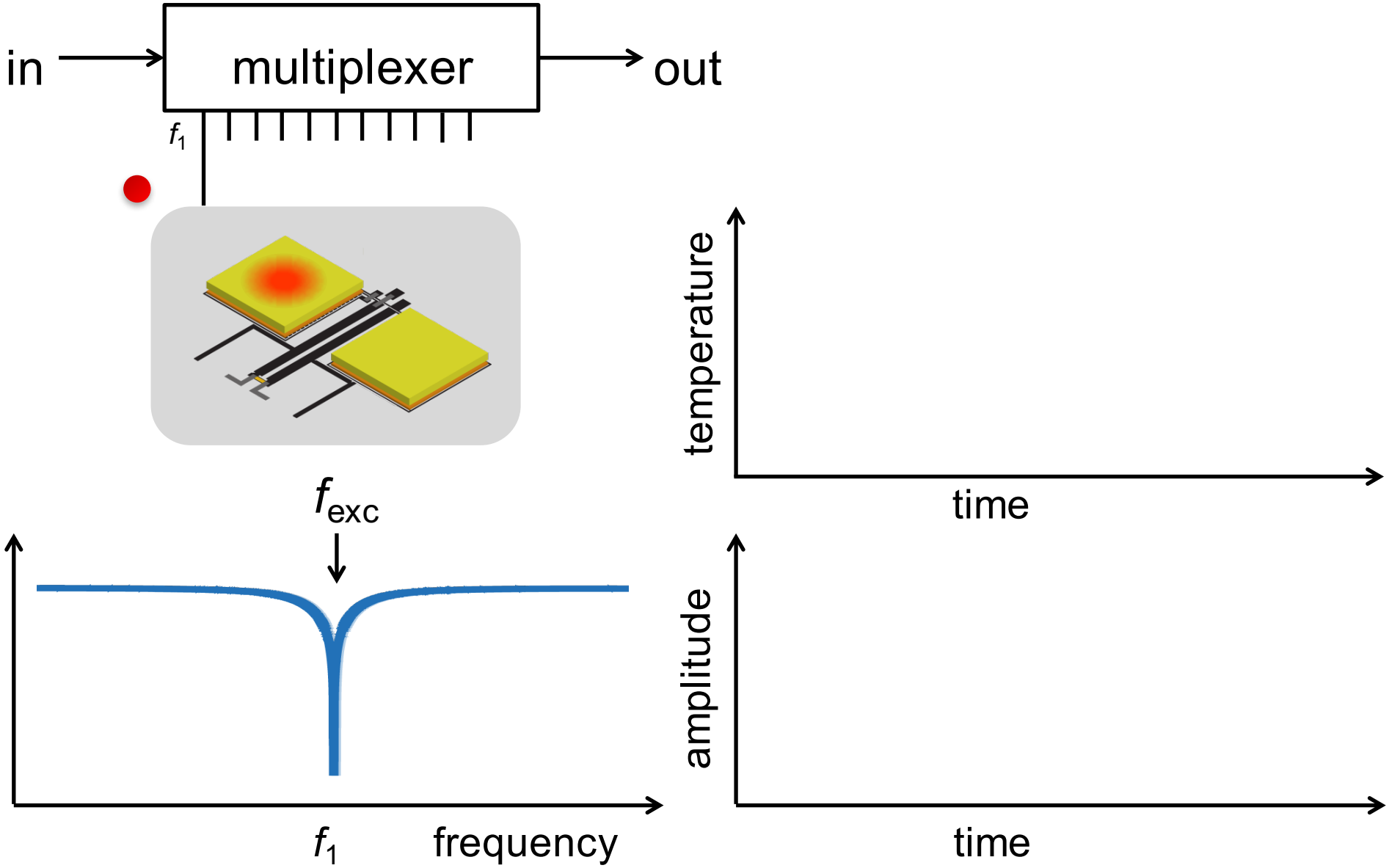
no galvanic contact to the readout circuit

Sebastian Kempf - Kirchhoff-Institute for Physics,
Heidelberg University

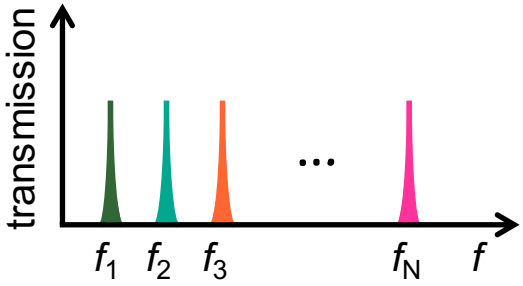
frequency domain multiplexing

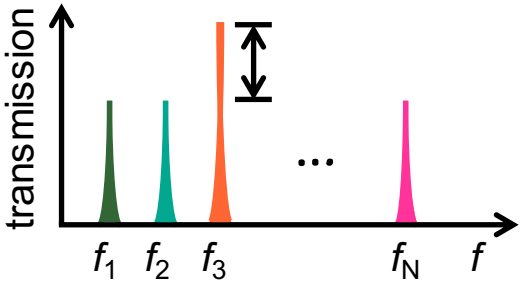


Frequency Domain Multiplexing



microwave SQUID multiplexer

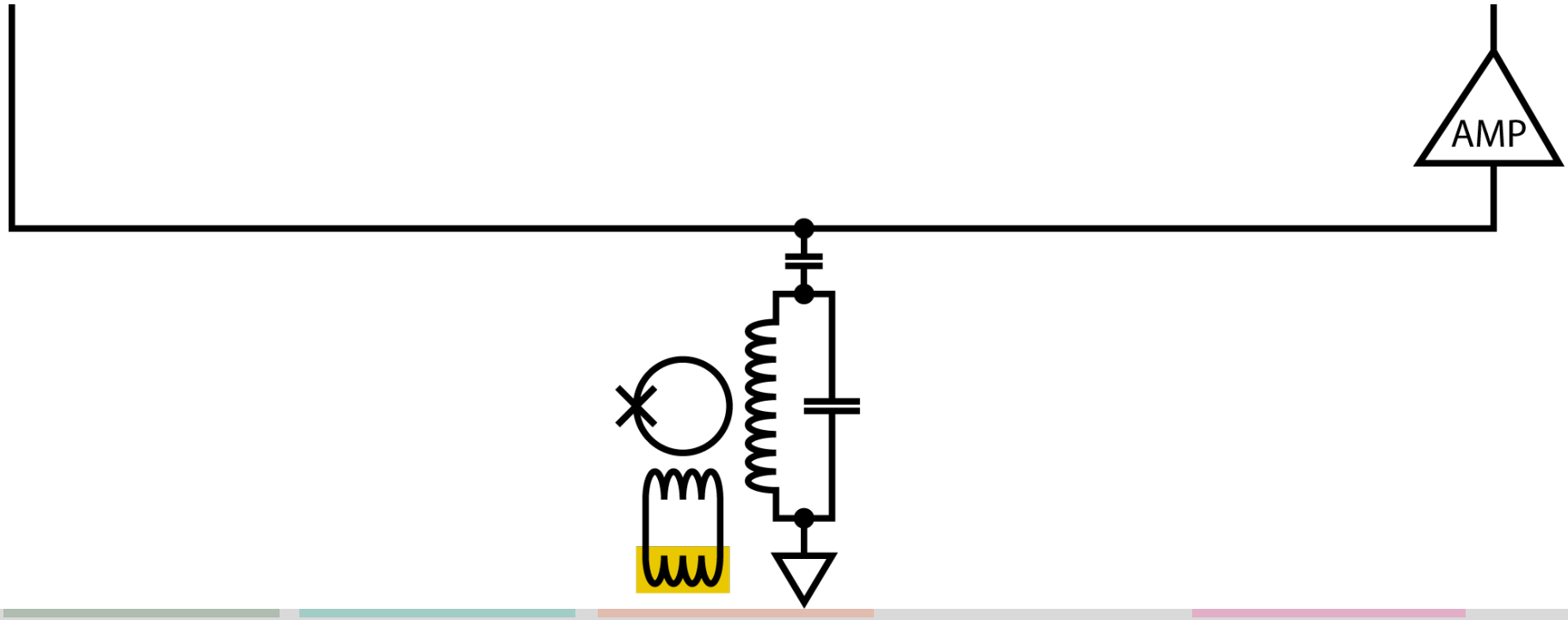




IN

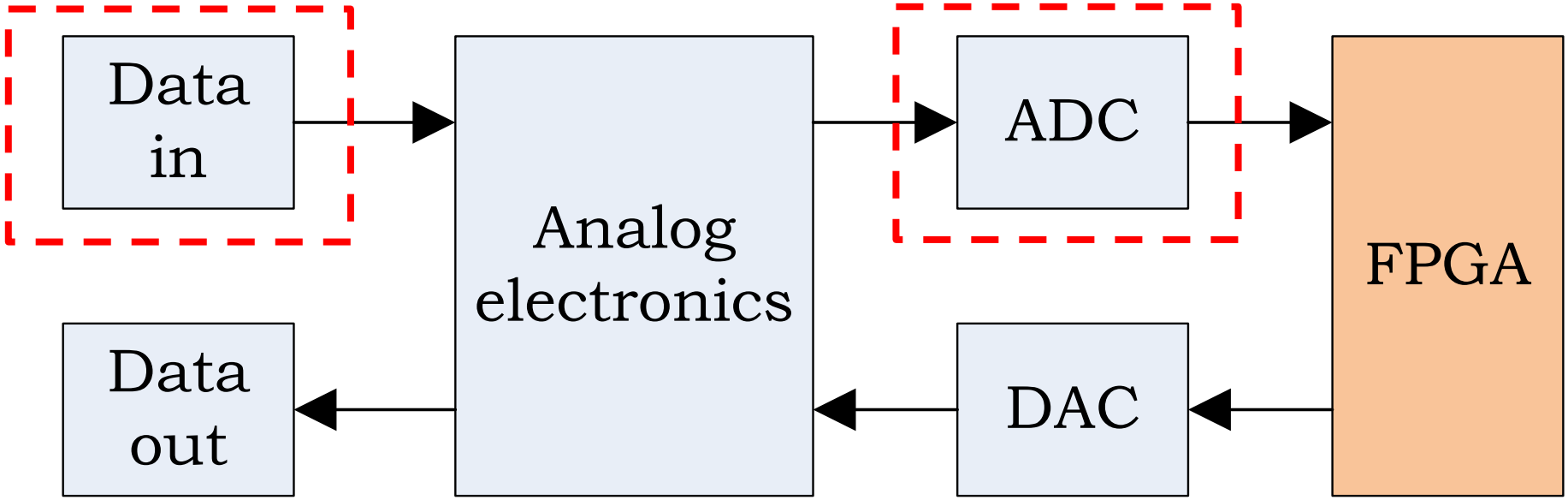
4 GHz – 8 GHz

OUT



Channelization

- MMCs :
  - 5 SQUIDs with excitation frequency :
    15 MHz, 80 MHz, 119 MHz, 147 MHz and 150 MHz
  - Spacing of the frequency bins : 10 KHz
- ADCs :
  - Sampled at 500 MSPS (fs)

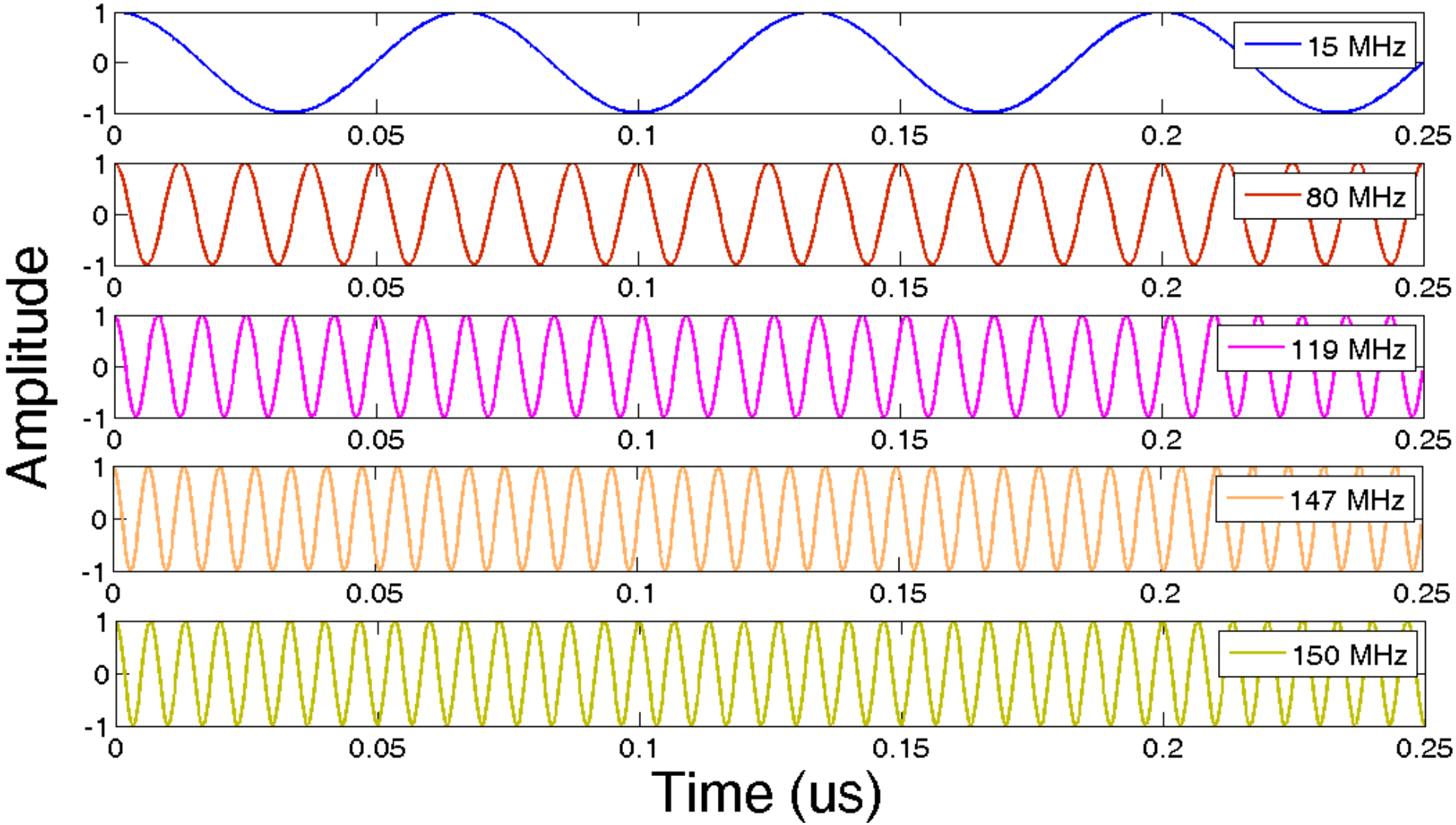


Channelization

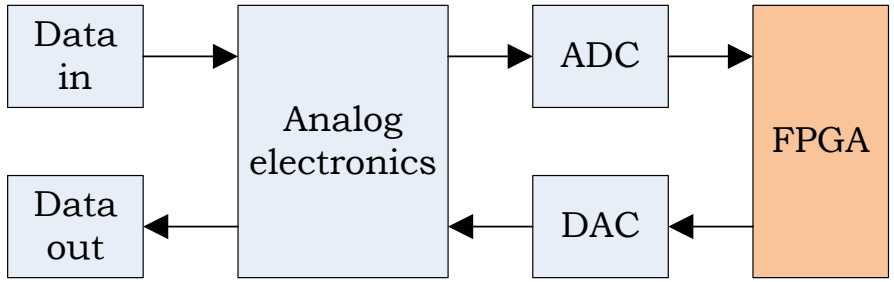
- MMCs :
  - 5 SQUIDs with excitation frequency :
    15 MHz, 80 MHz, 119 MHz, 147 MHz and 150 MHz
  - Spacing of the frequency bins : 10 KHz
- ADCs :
  - Sampled at 500 MSPS (fs)

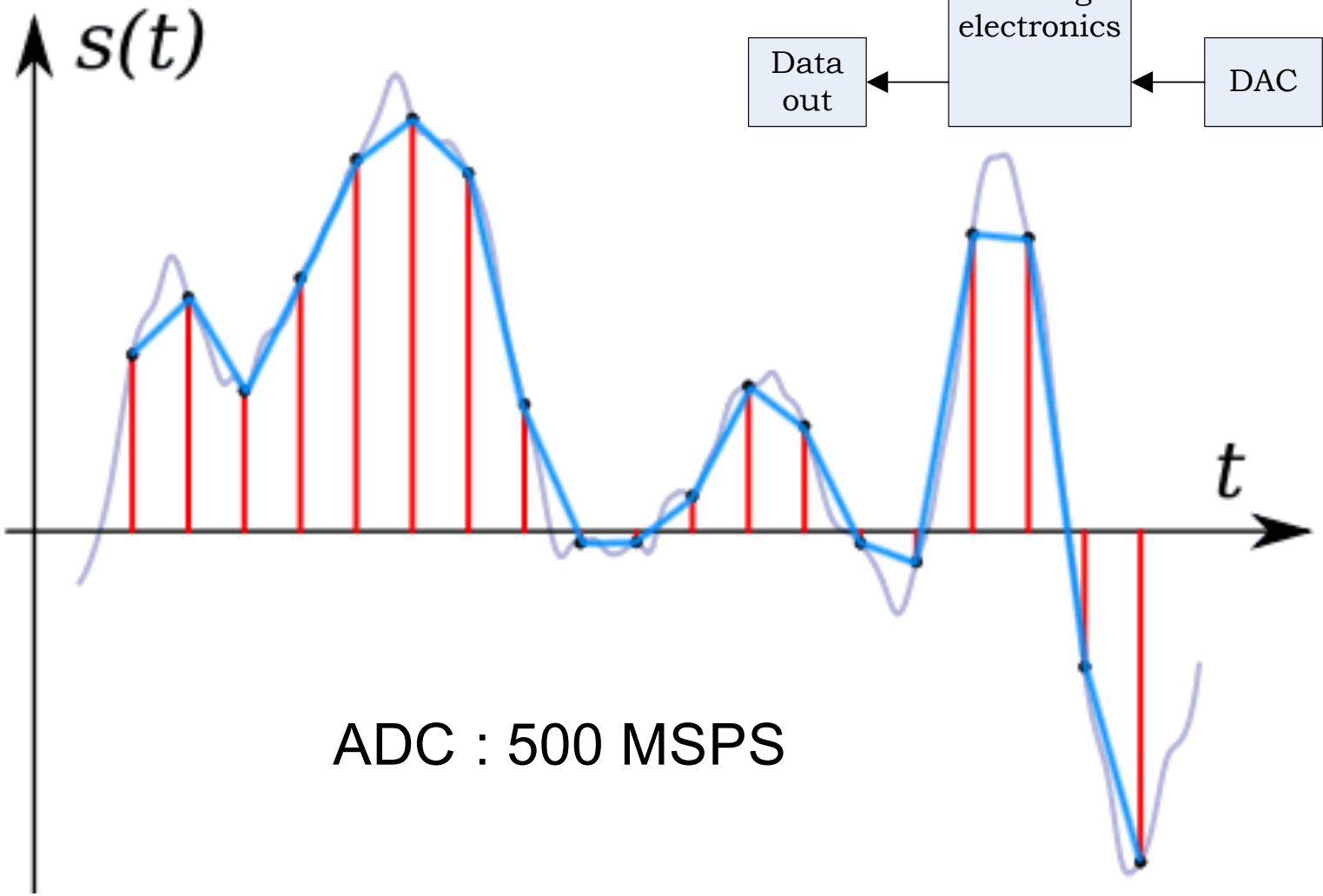
- Time domain
  - Digital down conversion
  - Poly-phase filter banks
- Frequency domain
  - Fast Fourier Transform (FFT)

Channelization

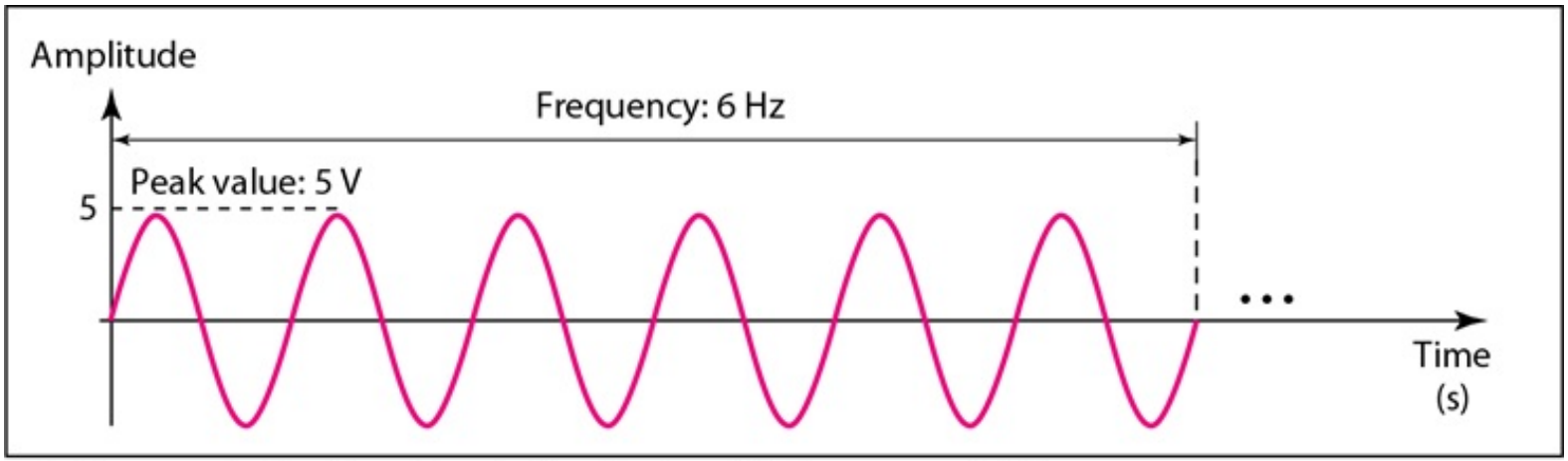


Sampling

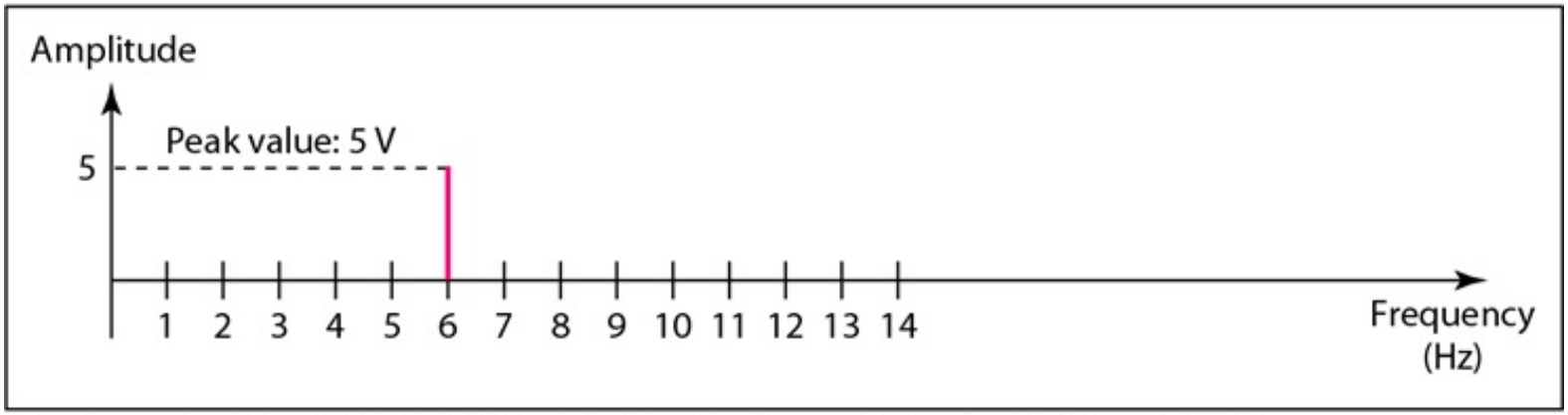

Data in
Analog electronics
ADC
FPGA
Data out
DAC


s(t)
t
ADC : 500 MSPS

FFT - basics

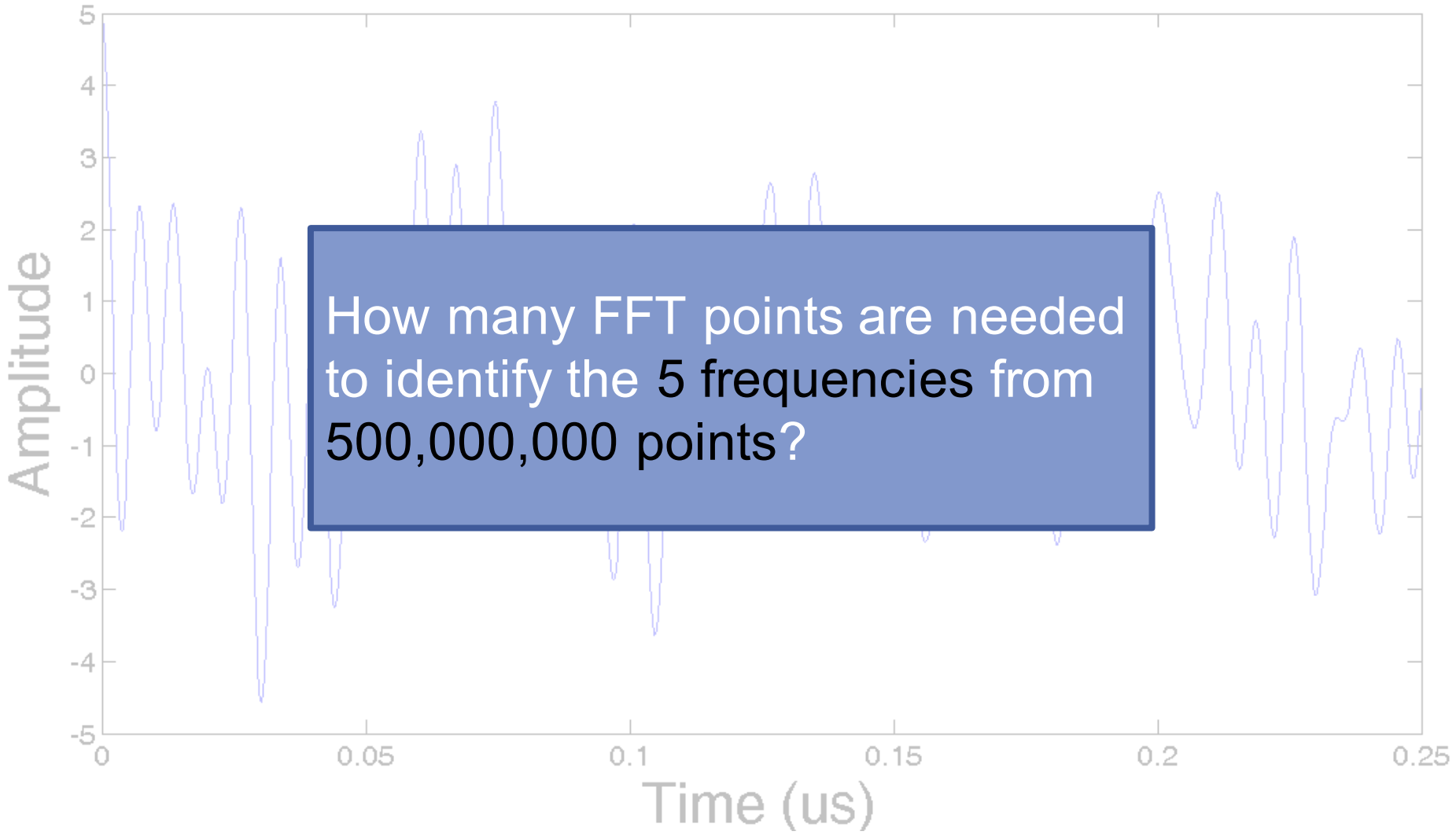


a. A sine wave in the time domain (peak value: 5 V, frequency: 6 Hz)



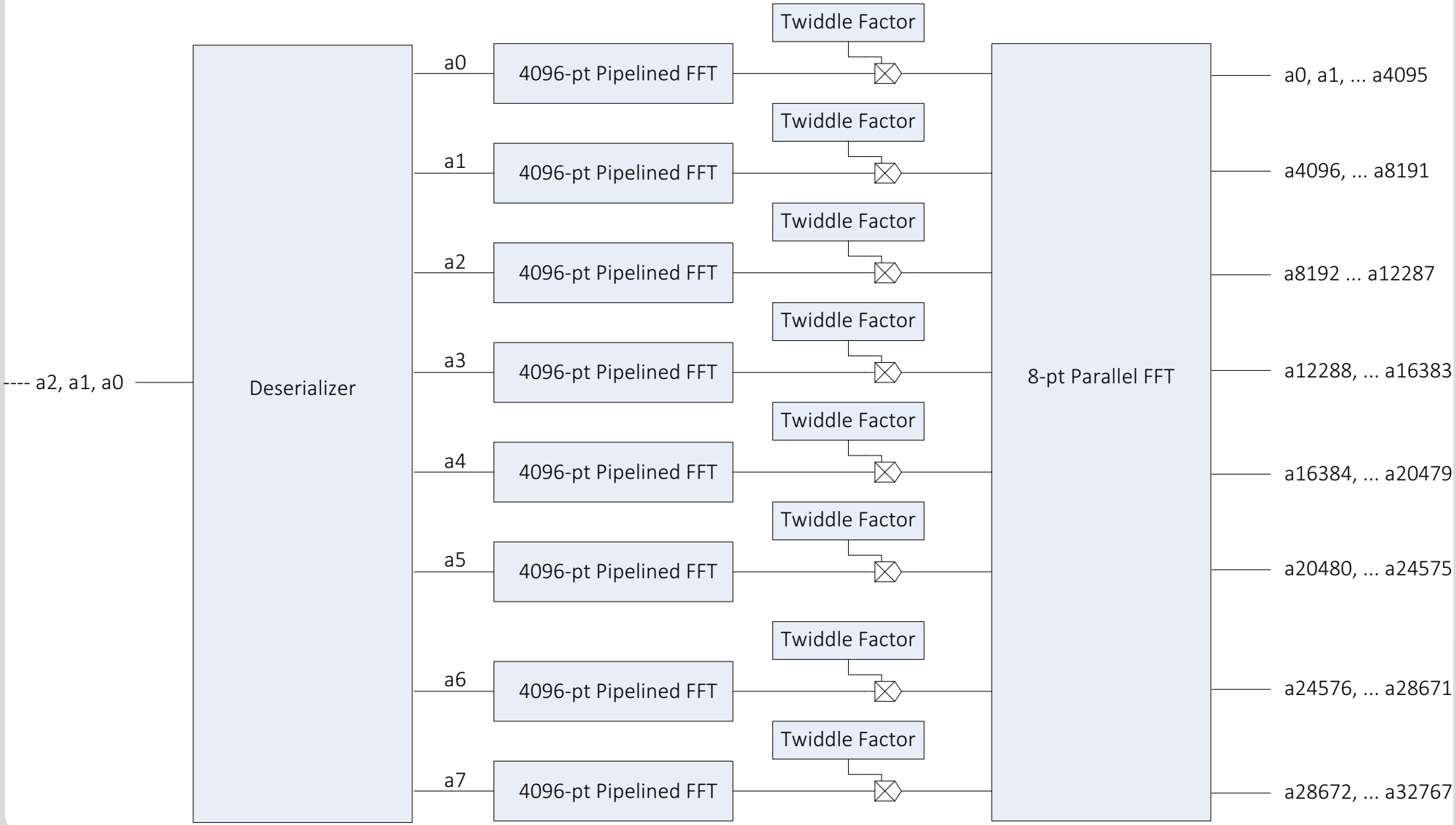
b. The same sine wave in the frequency domain (peak value: 5 V, frequency: 6 Hz)

Data In

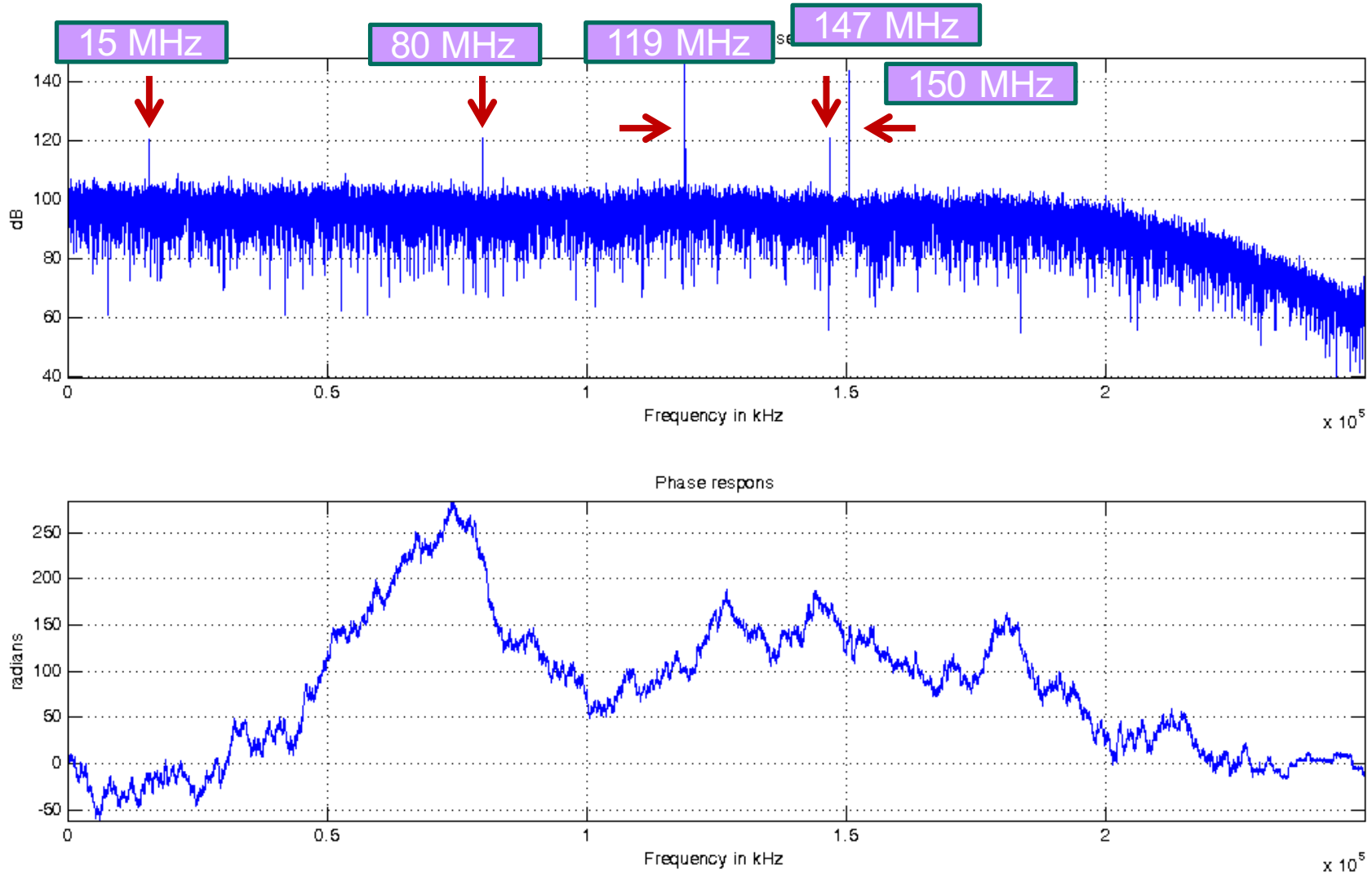


How many FFT points are needed to identify the 5 frequencies from 500,000,000 points?

Combined FFT: Simplified Block Diagram

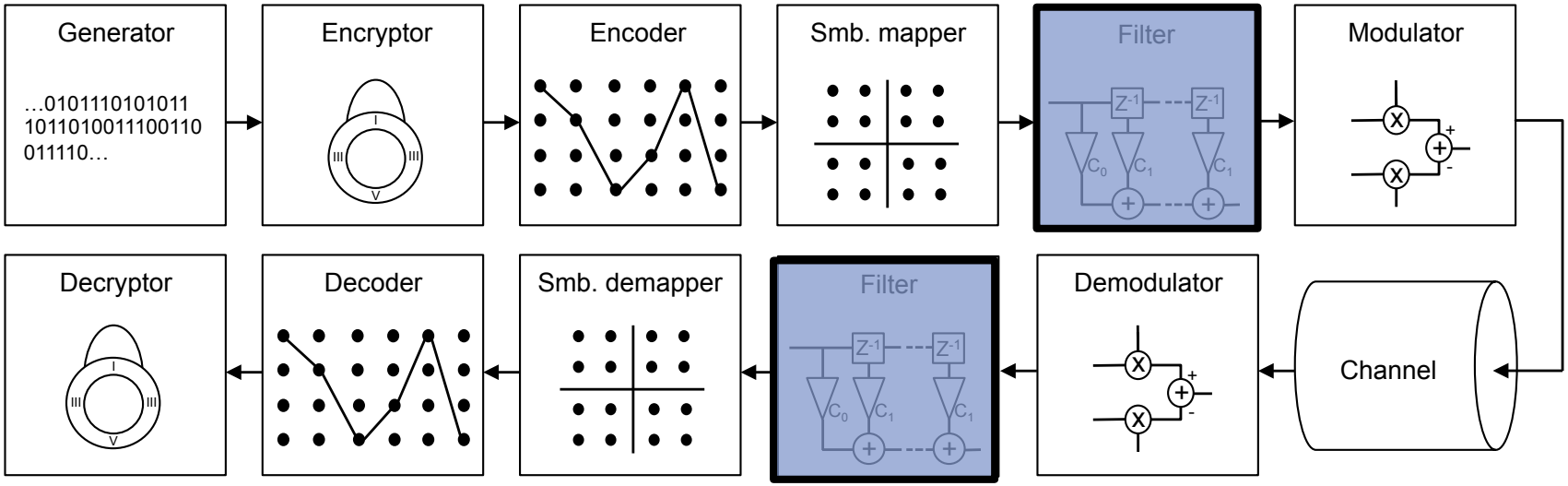


Combined FFT : Simulation

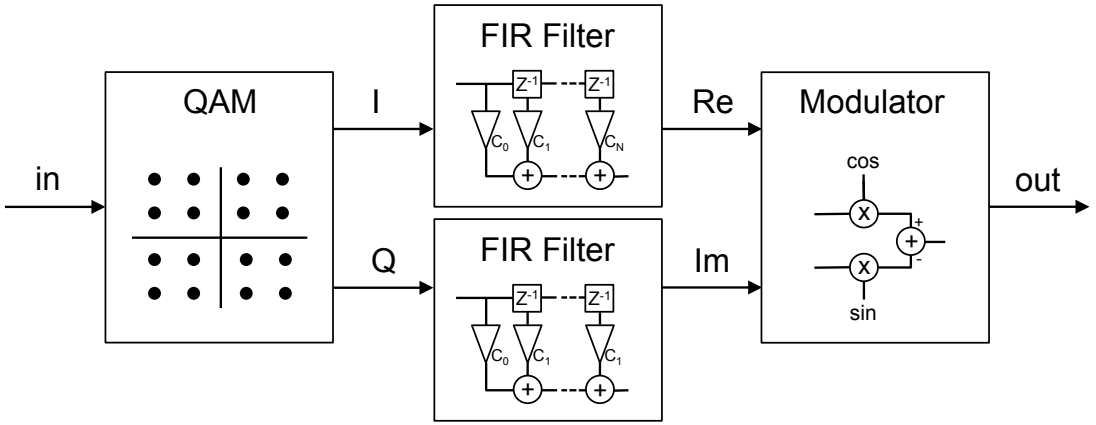


Standard Transmission Chain

- Standard Transmission Chain



- Optimization
  - Time domain
  - Frequency domain



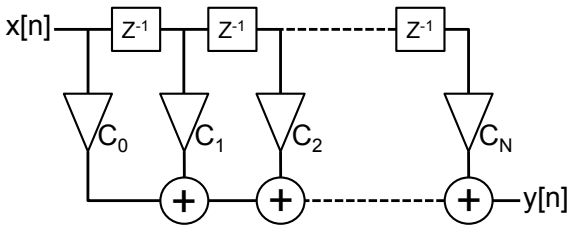
Filter Optimization - Frequency Domain

- Filter
  - Nyquist criteria avoids ISI
  - Pulse Shaping Filter to limit the transmission band
  - FIR filter: linear phase, inherent stability, no feedback
  - Matched filter improves SNR (if only stochastic noises)
  - Good compromise: SRRC filter

Time Domain

$$y[n] = x[n] \circledast h[n]$$

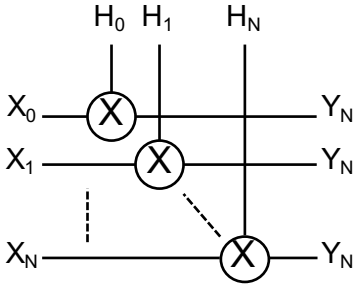
- Convolution: difficultly parallelizable



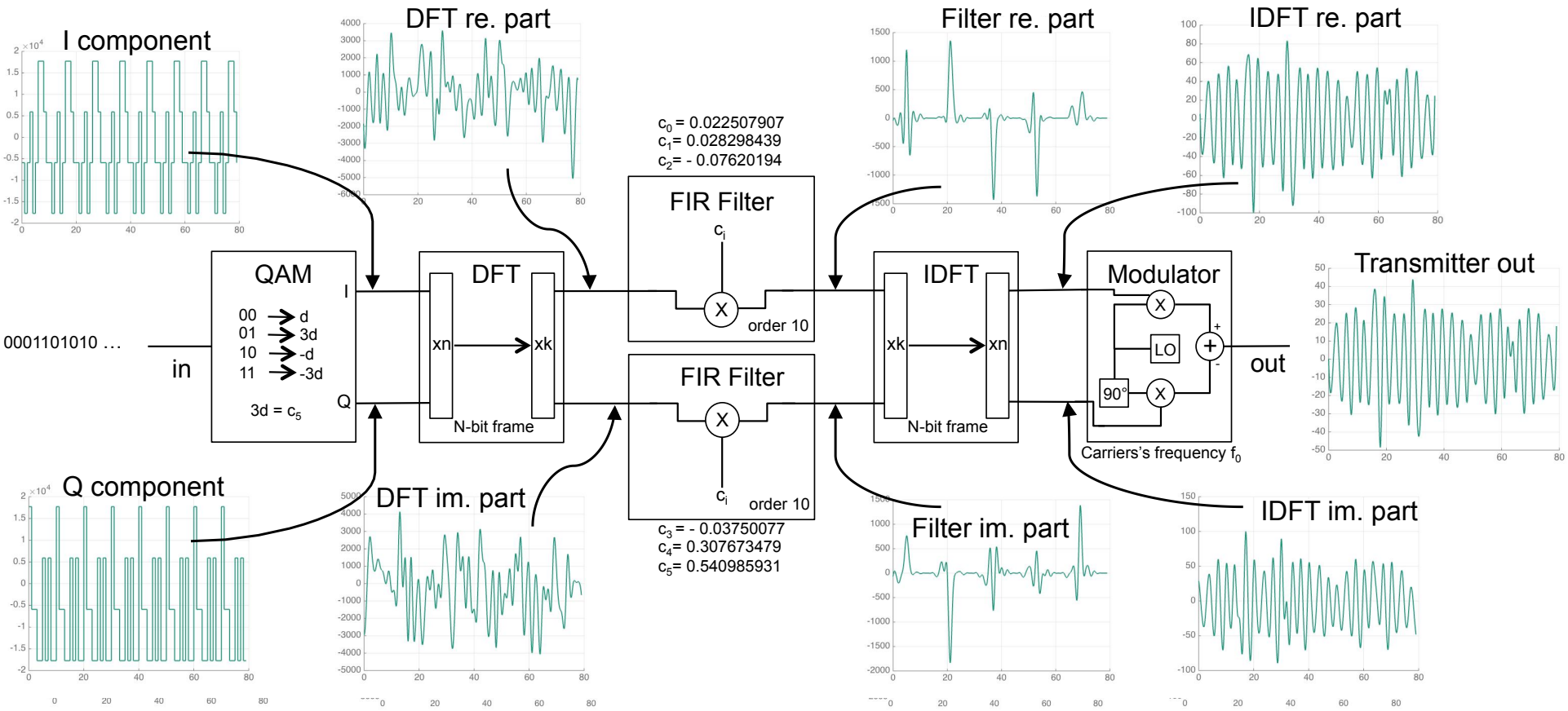
Frequency Domain

$$Y[k] = X[k] \cdot H[k]$$

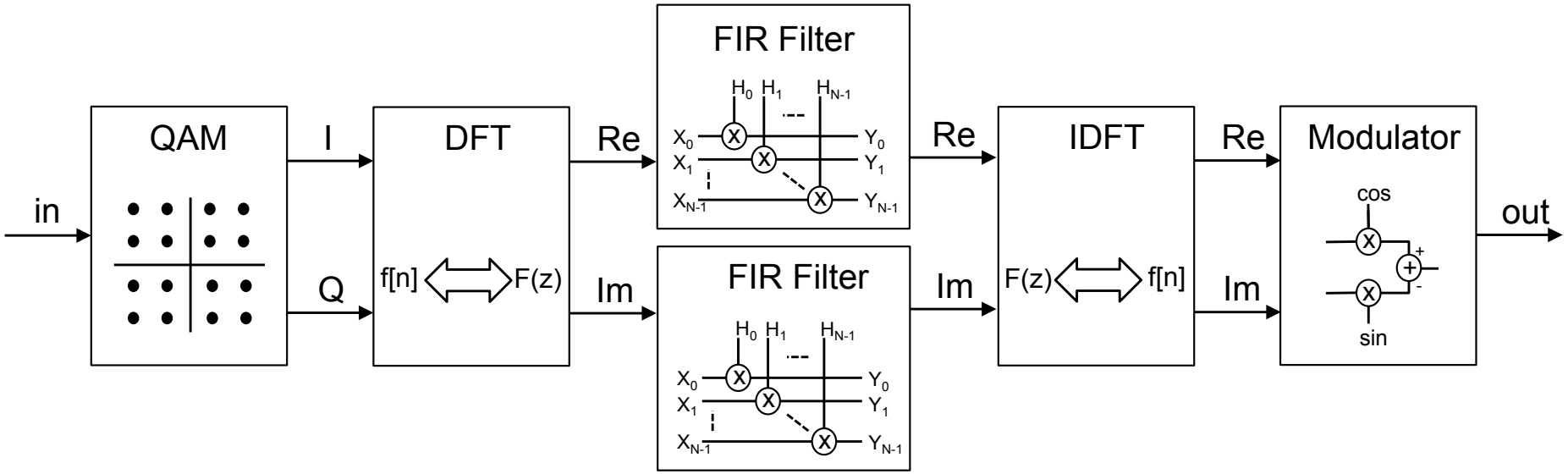
- Multiplication: easily parallelizable

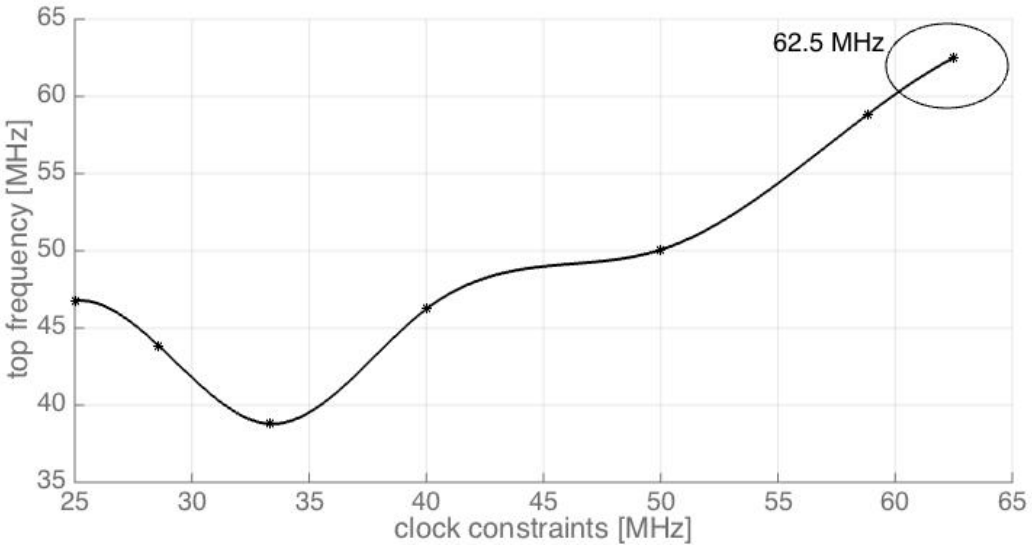


Filter Optimization - Frequency Domain



Mixed-Domain Approach

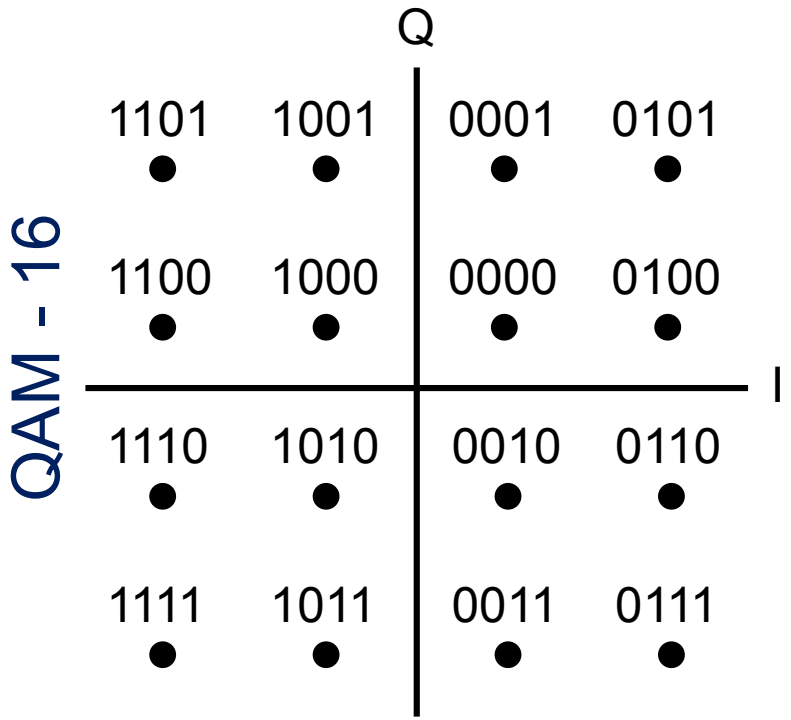


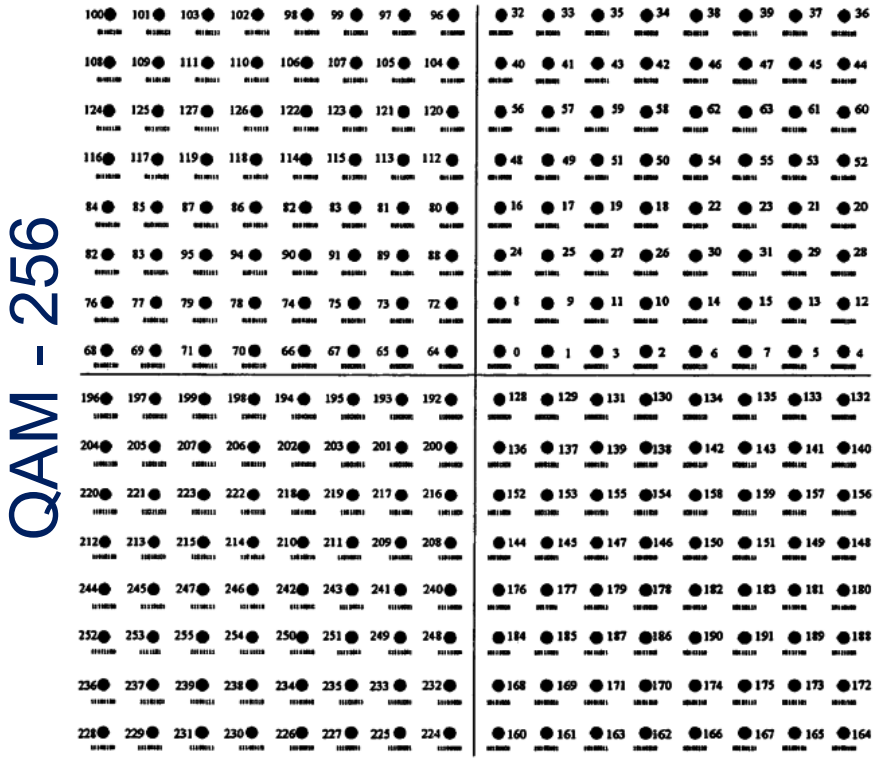


Effective speed of
16 x 62.5 = 1 GHz

Performance optimization – QAM Modulator

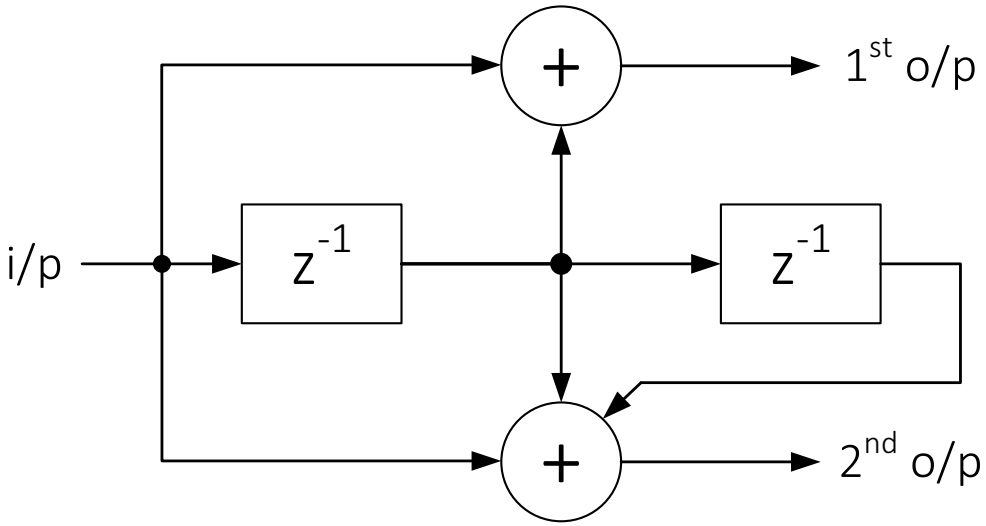
- QAM Mapper
  - M-QAM formats (M=8, 16, 32, etc.)
  - Clusterization in $\log_2(M)$ bits
  - Gray code for hamming distance of 1
  - Rectangular constellation is considered





Performance optimization – FEC

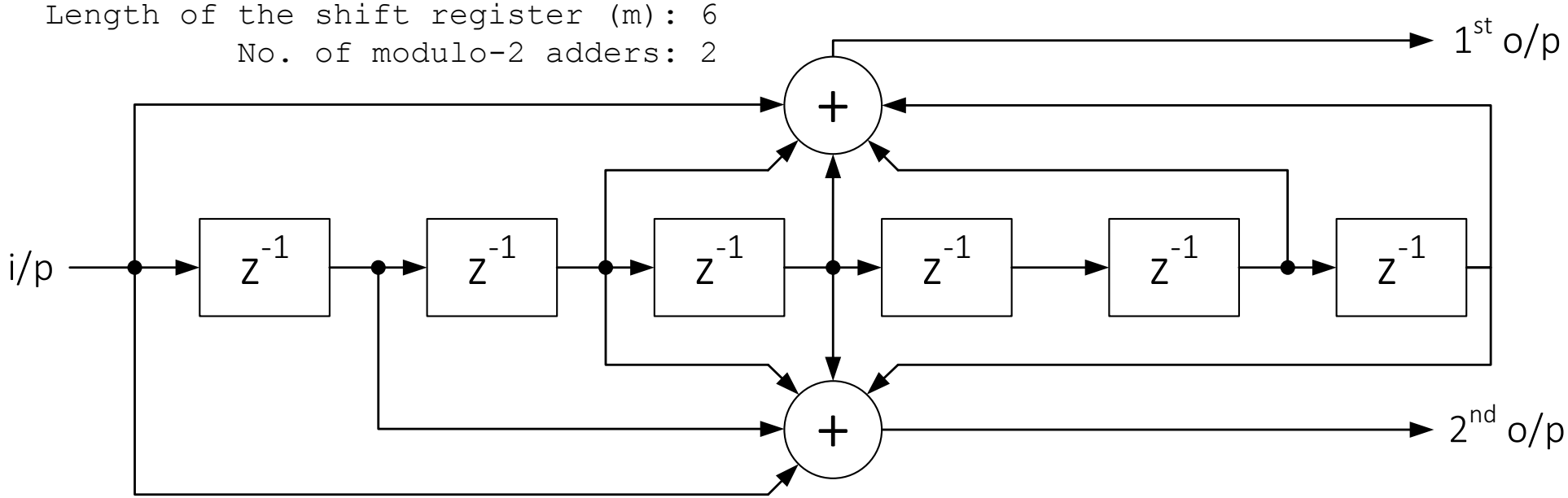
- Forward Error Correction
  - Convolutional Encoder and Viterbi Decoder
- Code rate
  - 1/2, 1/3 and 2/3



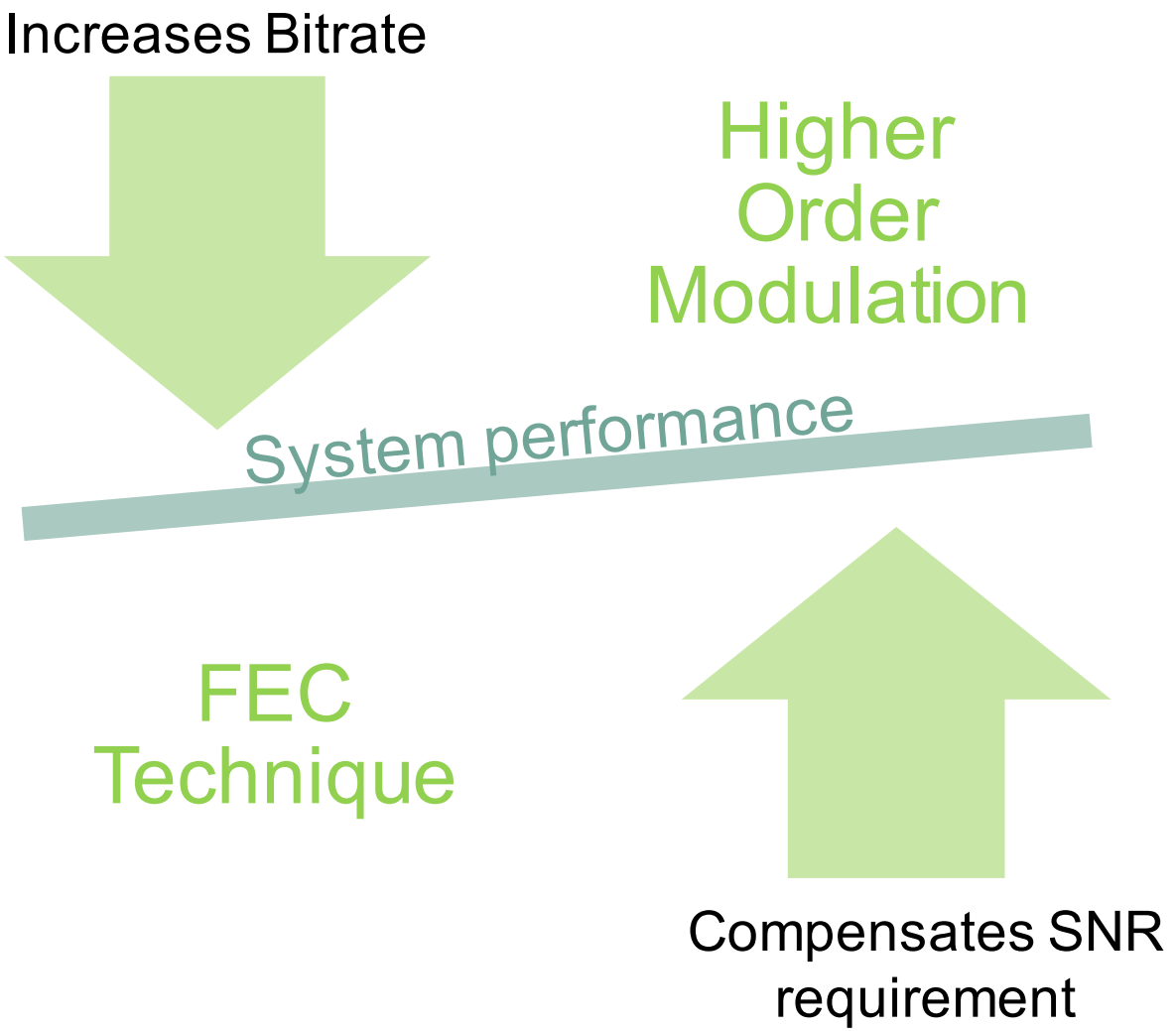

```
Trellis code:(3, [6 7])
Code rate (k/n): 1/2
Generator Polynomials:[6 7]
In octal: [110, 111]
Constraint length (M): 3
Length of shift register (m): 2
No. of modulo-2 adders: 2
```

Performance optimization – FEC

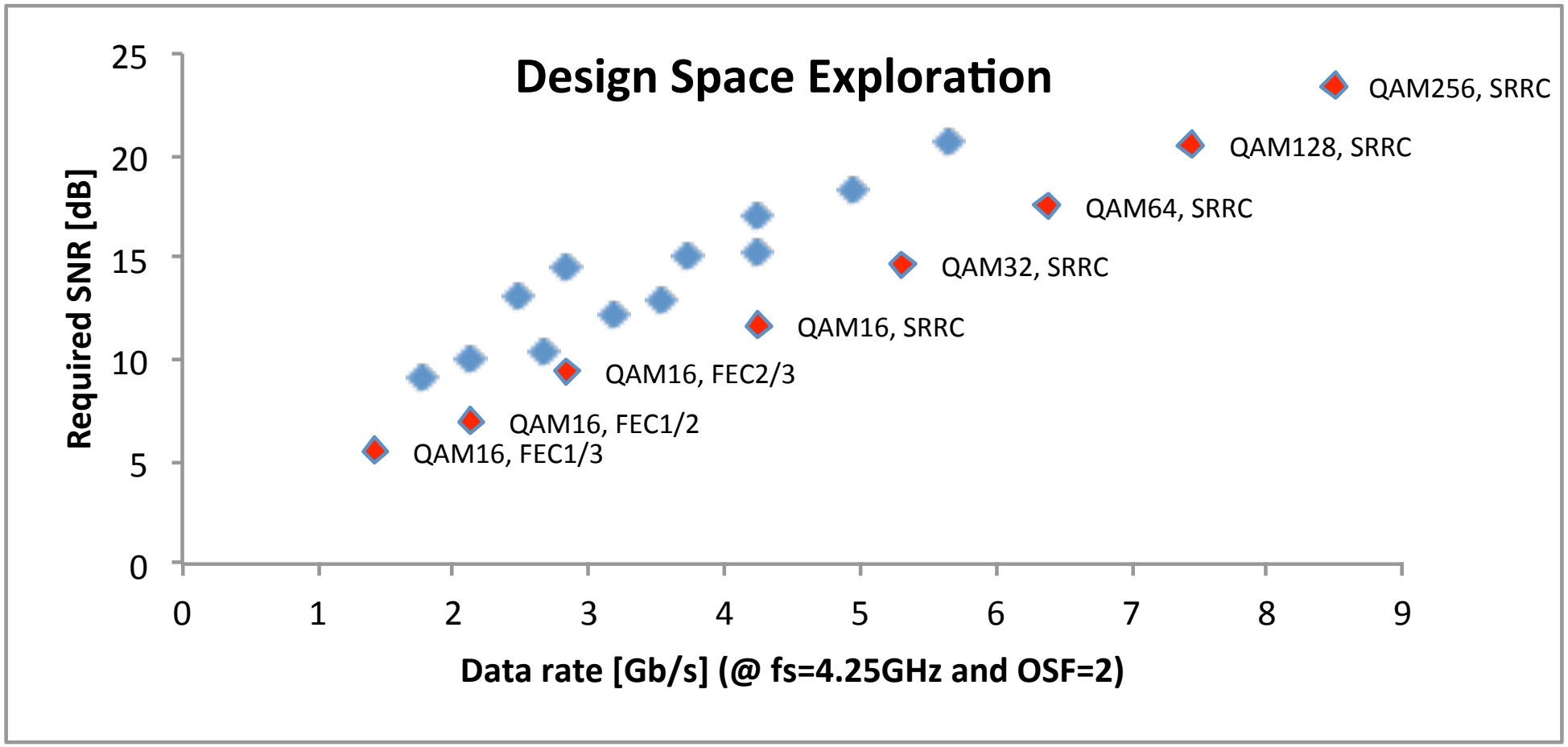
```
                Trellis code:(7, [171 133])
              Code rate (k/n): 1/2
       Generator Polynomials:[171 133]
                   In octal: [1111001, 1011011]
       Constraint length (M): 7
Length of the shift register (m): 6
        No. of modulo-2 adders: 2
```



Pareto Optimal Solutions

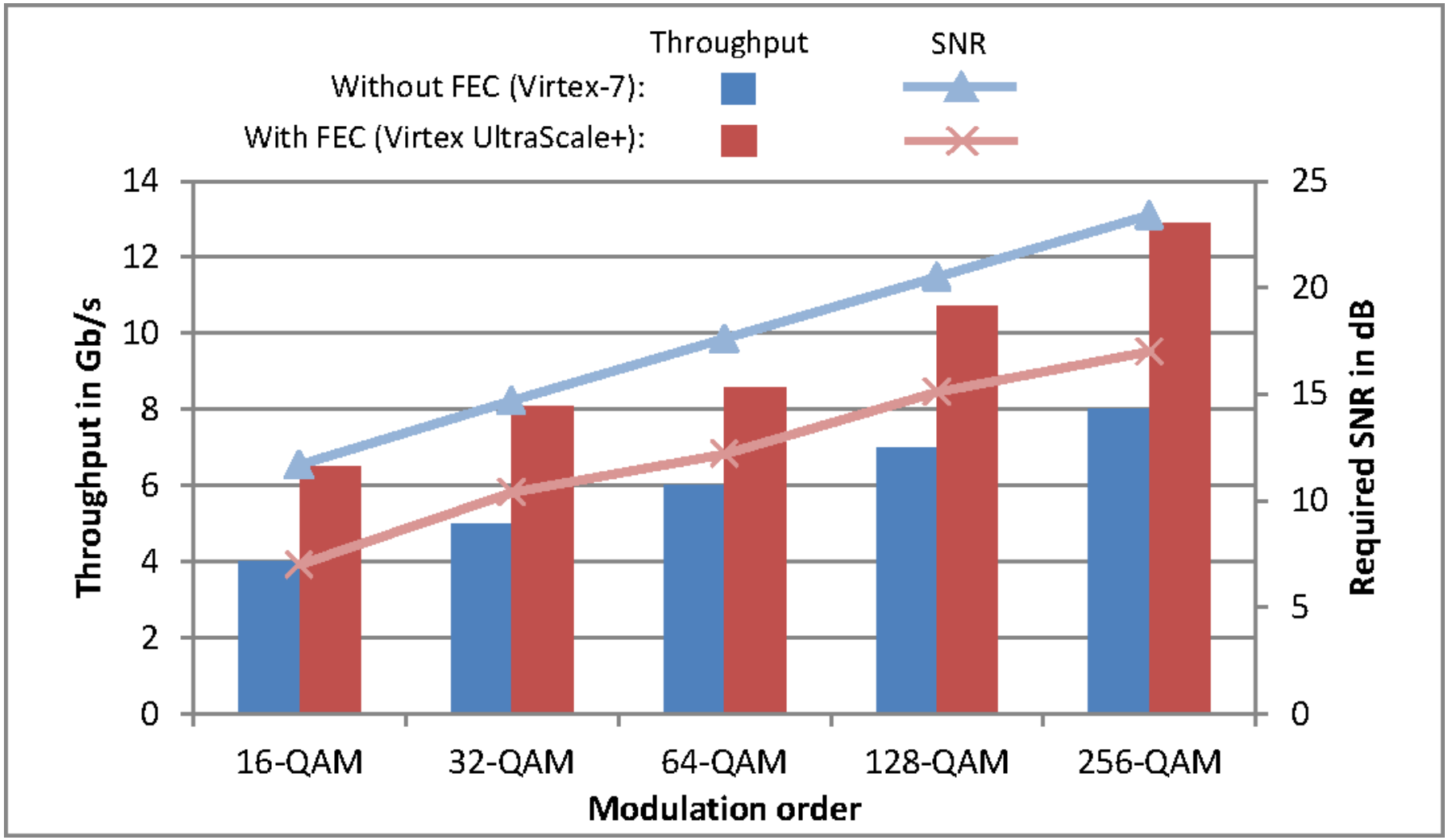


Pareto Optimal Solutions



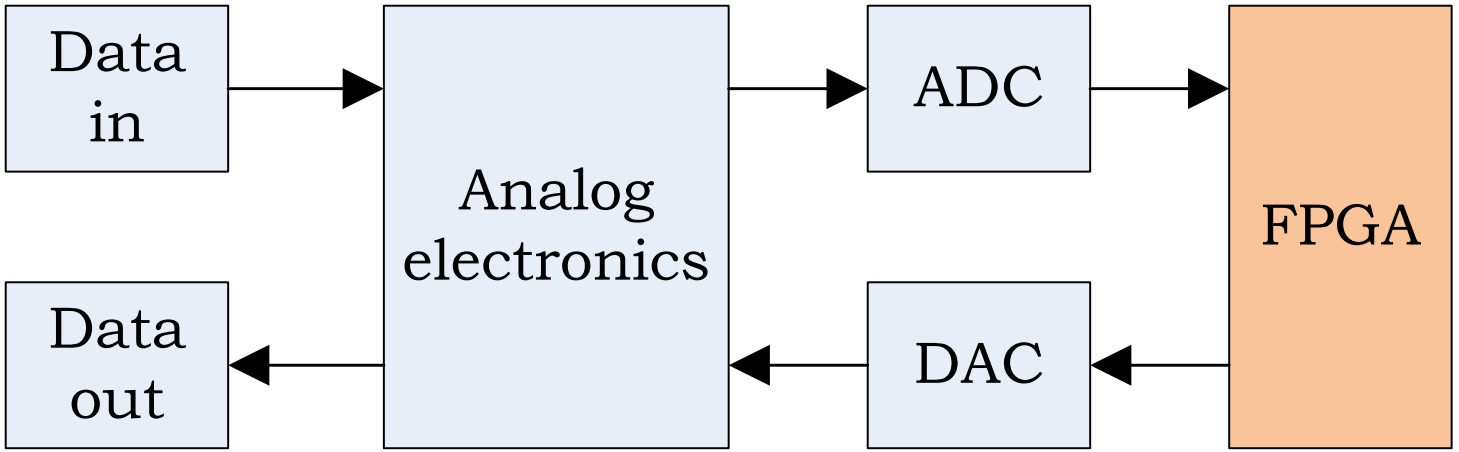
Performance optimization – FPGA

- Throughput with 16-parallel I/Os



Summary

- Channelization
  - Combined FFT - MMCs
- Performance optimization in Transmission chain
  - Filter
- QAM modulator
  - Different modulation orders
- Forward Error Correction (FEC)



Thank you for your attention!

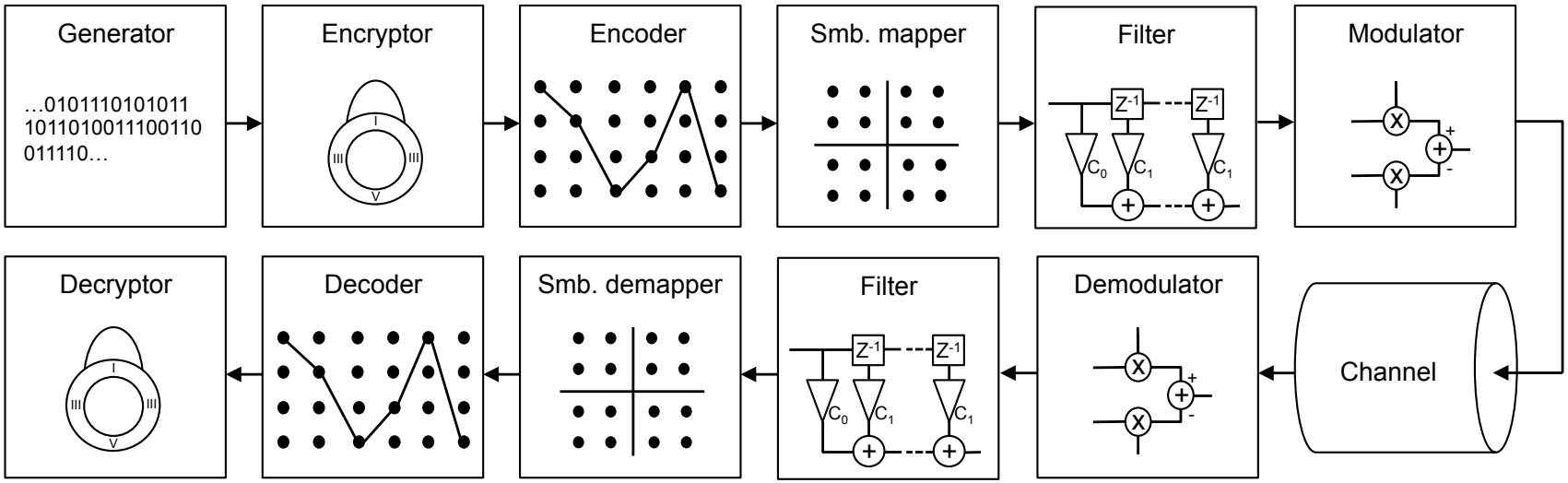
Any questions?

Combined FFT : Virtex-7

LUTs	7%
Registers	6%
Memory	6%
DSPs	24%
Latency	133576 ns
Clk	10.164 ns
Acheivable frequency	98.38 MHz

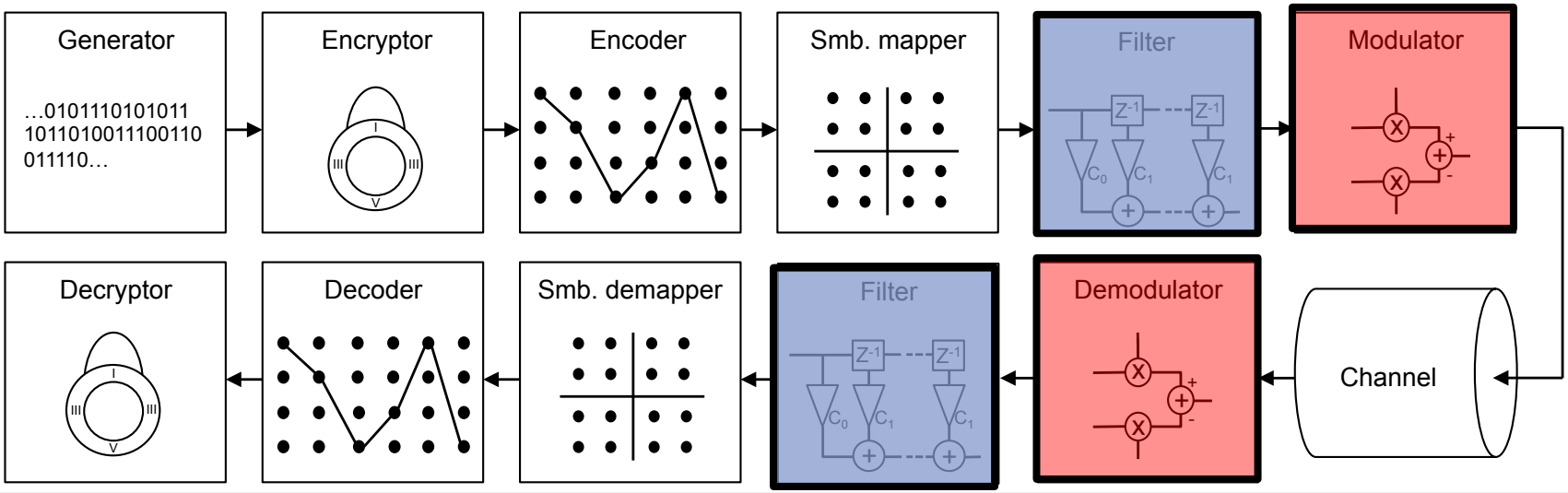
Motivation

- Software Defined Ratio
- Channelization
  - Frequency wall
- FPGA



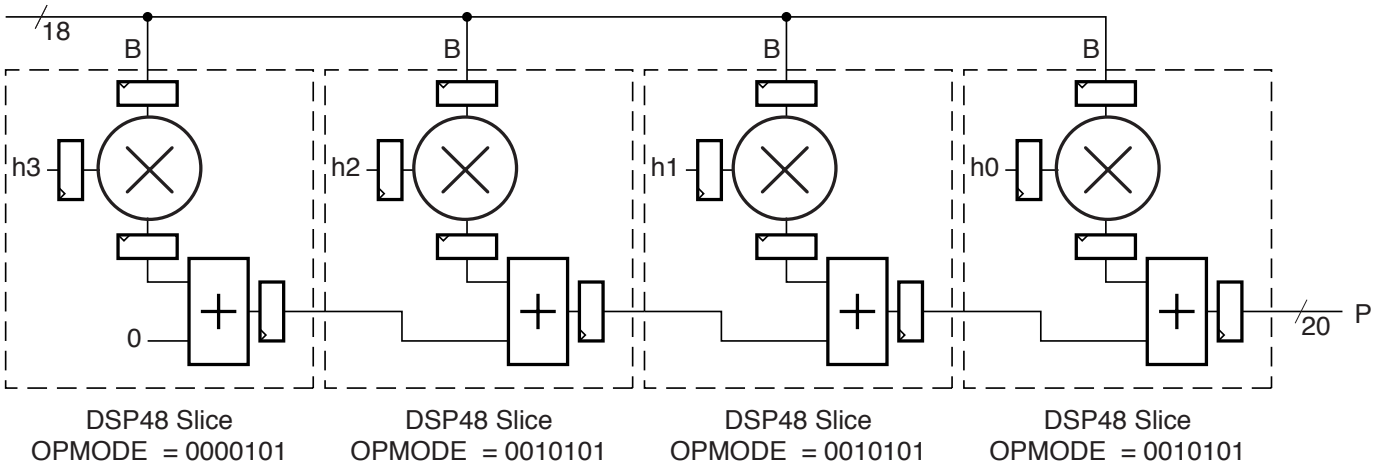
Motivation

- Software Defined Ratio
- Channelization
  - Frequency wall
- FPGA
  - Performance optimization
    - Filter
    - Modulator

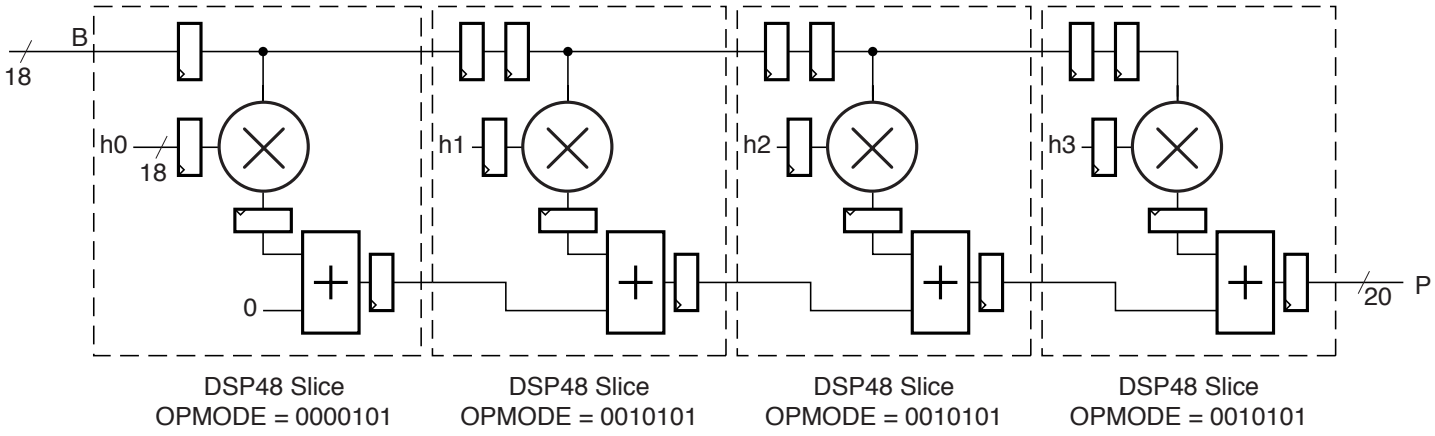


Filter Optimization – Time Domain

Transposed Filter



Systolic Filter



Filter types

Transposed Filter

- Low latency
- High fanout of input signal – limits performance

Systolic Filter

- Higher performance
- Higher latency

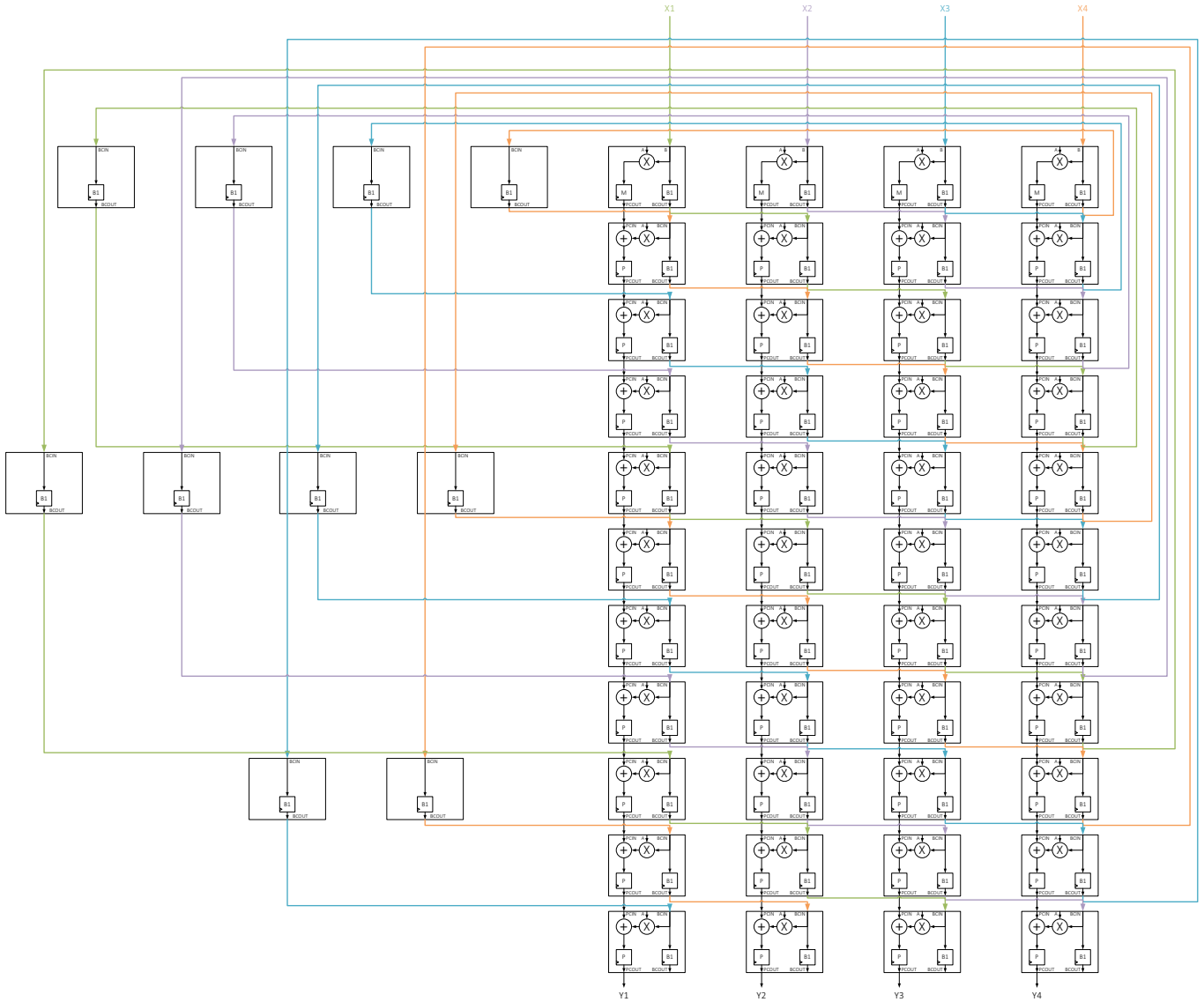
Filter type	Features	Frequency (MHz)
Transposed Filter	Non-symmetric	571.102
Systolic Filter	Symmetric	610.128
	Non-symmetric	663.129

Parallelized Systolic Filter

- Cascaded DSP48E1 slices
- Pipelining
- Novel filter architecture with parallel filter strips
  - Scalability through parameterizable generic design
    - N Filter taps
    - P Parallel strips
  - Achievable performance
    - P*f_clk
  - Requires P times N DSP slices

Parallelized Systolic Filter

Parallel strips (P) : 4



Filter taps (N) : 11

Filter Optimization in Time Domain

Filter type	Features	Frequency (MHz)
Transposed Filter	Non-symmetric	571.10
Systolic Filter	Symmetric	610.13
	Non-symmetric	663.123

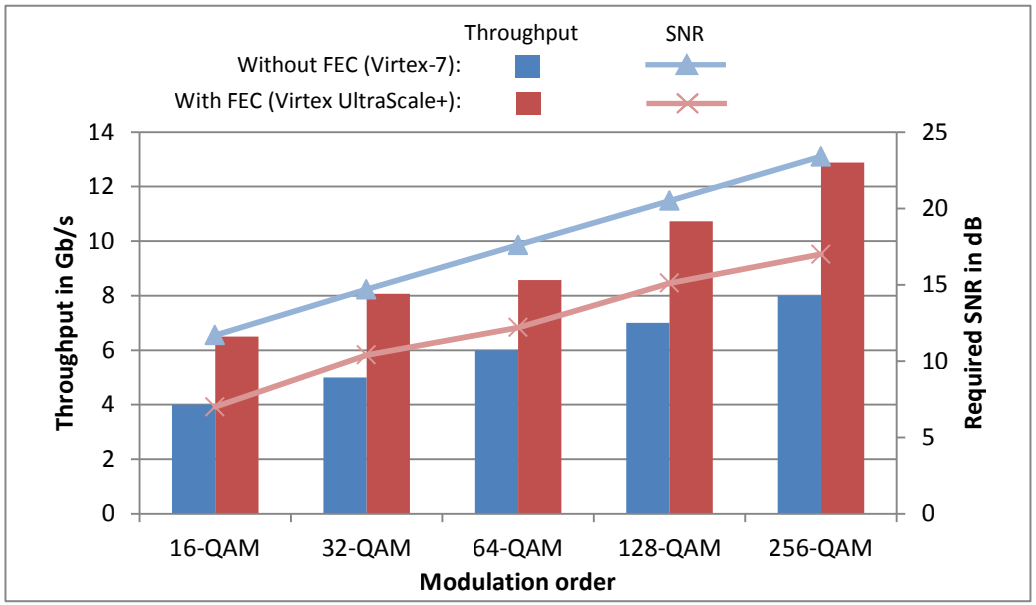
System Performance			
	Systolic Filter	Optimized Systolic Filter	Parallelized Systolic Filter (Degree of parallelism:4)
Clk (ns)	1.51	1.44	1.16
Frequency (MHz)	663.13	695.10	4*865.05

Outlook

- Channelization
  - Poly-phase filter banks
  - Optimized time-domain techniques
- Virtual FPGAs??

High-speed QAM: Throughput measurements

- Throughput with 16-parallel I/Os



- Throughput with 32-parallel I/Os

QAM Order	Max.Freq (MHz)	Through-put (Gb/s)	LUTs	Registers	DSPs	BRAM
16	168.55	10.79	121917	144613	6272	-
32	112.37	8.99	122073	145007	6272	-
64	134.39	12.90	121831	144799	6272	32
128	130.02	14.56	121864	144992	6272	32
256	146.16	18.71	121896	145184	6272	32

Motivation

- Global Communication
  - Video on demand
- Physics Experiments
  - Particle detectors
- Current limitations
  - Frequency wall
  - Clock frequencies < 1 GHz in current FPGAs
- Counterclaim
  - Higher BW utilization
  - Efficient Modulation techniques
  - Exploiting the inherent parallelism and flexibility of FPGAs
  - Optimizations on architecture level
  - Providing guidelines for future FPGAs (or custom FPGAs)

Optimization techniques

- Time domain
  - Filter types
    - Transposed FIR Filter
    - Systolic FIR Filter
    - Modified Systolic Filter
  - Implementation optimizations
    - Cascaded DSP48E1 slices
    - Pipelining
    - Different ways of sin/cos modulation
- Mixed time-/frequency domain
  - Parts of processing chain in time domain, other parts in frequency domain

Future Scope

- Integrate the parallelized filter into the QAM system
- Implement and evaluate the ViSA-COM concept
- Integrate into heterogeneous platform through shared memory
- Modeling of specialized hard macros for future communication targeted FPGAs

Publications

- Published:
  - K. Siozos, P. Figuli, H. Sidiropoulos, C. Tradowsky, K. Maragos, G. Shalina, D. Soudris, J. Becker, **"TEAChER: TEach AdvanCEd Reconfigurable Architectures and Tools" (Nominated as Best Paper Candidate)** *In Applied Reconfigurable Computing,* Band 9040, S. 103-114, 2015
  - G. Shalina, T. Bruckschloegl, P. Figuli, C. Tradowsky, G. Almeida, J. Becker, **"Bringing Accuracy to Open Virtual Platforms (OVP): A Safari from High-Level Tools to Low-Level Microarchitectures"** *In IJCA Proceedings on International Conference on Innovations In Intelligent Instrumentation, Optimization and Electrical Sciences*, Band ICIIIOES, S. 22-27, 2013
  - E. Sotiriou-Xanthopoulos. G. Shalina, P. Figuli, K. Siozios, G. Economakos, J. Becker, **"A Power Estimation Technique for Cycle-Accurate Higher-Abstraction SystemC-based CPU Models"** *In International Conference on Embedded Computer Systems: Architectures, Modeling and Simulation*, SAMOS 2015.
- Submitted:
  - G. Shalina, P. Figuli, J. Becker, **"Parametric Design Space Exploration for Optimizing QAM based High-speed Communication"** In *International Conference on Communications in China*, ICCC 2015.
- Planned:
  - G: Shalina, P. Figuli, J. Becker, **"Performance Driven Optimizations in FPGA Based QAM Systems using ViSA-COM"**