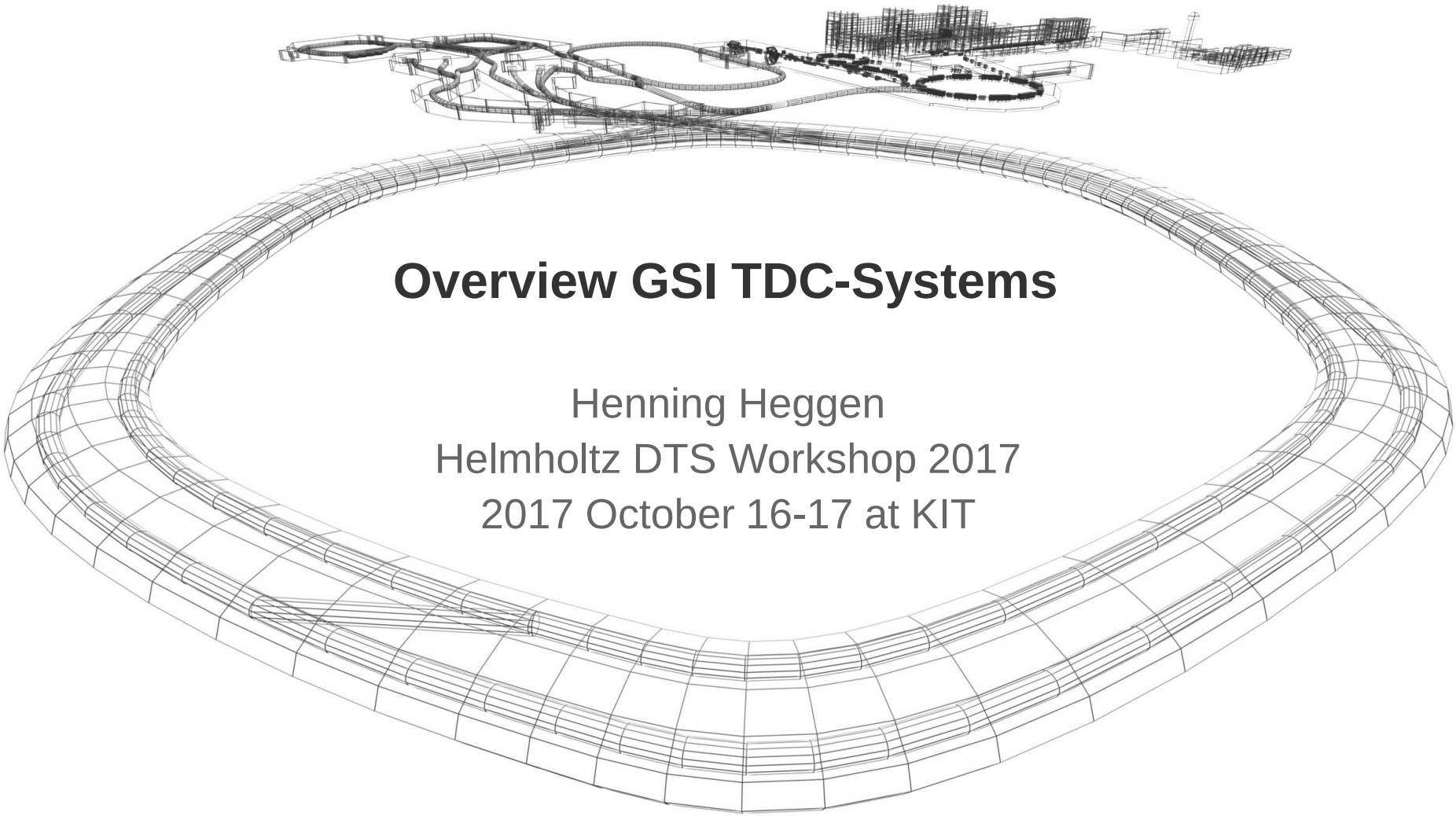


Overview GSI TDC-Systems

Henning Heggen

Helmholtz DTS Workshop 2017

2017 October 16-17 at KIT

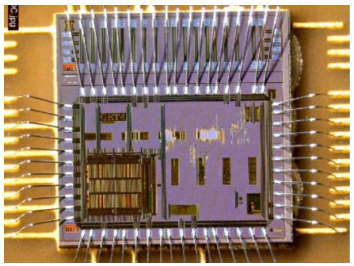
TDC Concepts

ASIC

- Radiation tolerance
- Low power
- Small solution size
- Fast / low dead time

FPGA TDC

- Flexibility
- Tailored to needs
- Off-the-shelf components (availability)

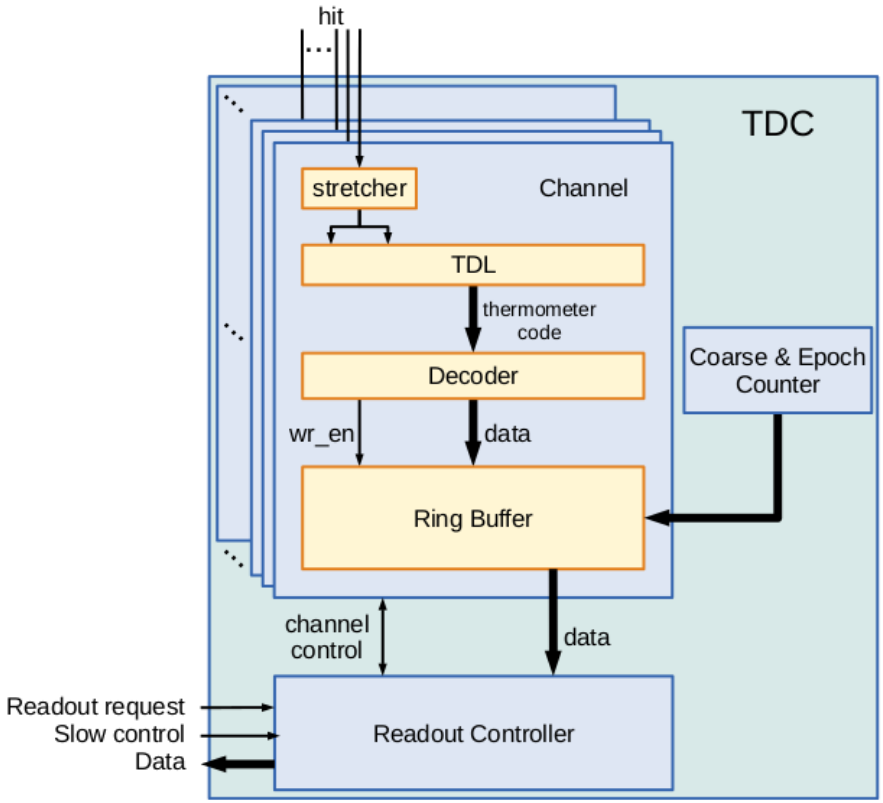


No clear winner

Matter of taste / particular needs

FPGA TDC - Architecture

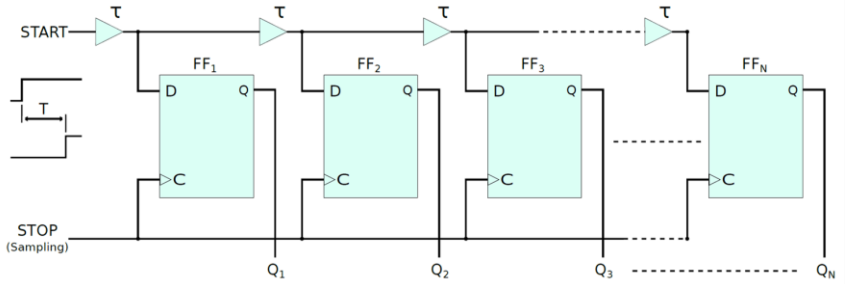
- Edge-to-pulse input stage (stretcher)
- Tapped Delay Line (TDL) as fine time interpolator
- Decoder for time information: thermometer code → binary
- Run-time counter (coarse and epoch counter) for continuous measurement range
- Ring buffer for hit history in triggered readout



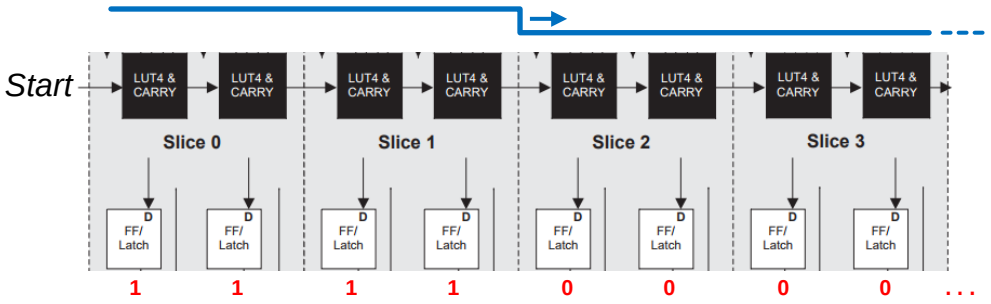
Schematic view of the TDC arcitecture [1]

Tapped Delay Line

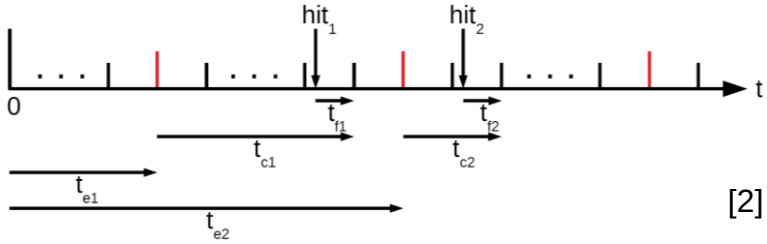
- Look-up table (LUT) and carry chain as delay element
  - Shortest delay element (bin) in FPGA
  - Placed manually
- Start signal (pulse edge) propagates along delay line and is latched at every LUT
- Propagation is stopped by common stop signal
  - 200 MHz clock for min. skew
- Time information composed out of fine time from delay line and run-time counter values



Tapped Delay Line method with common stop signal [1]



Programmable Function Unit (PFU) of FPGA

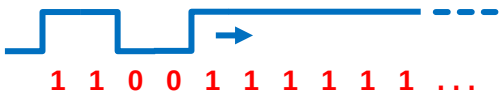


[2]

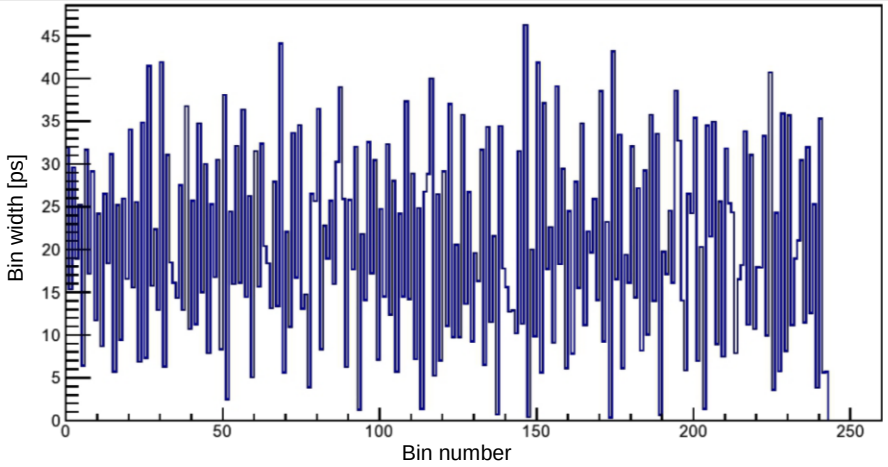
$$\Delta t = \left(t_{e2} + t_{c2} - t_{f2}\right) - \left(t_{e1} + t_{c1} - t_{f1}\right)$$

Bin Widths / Non-Linearity

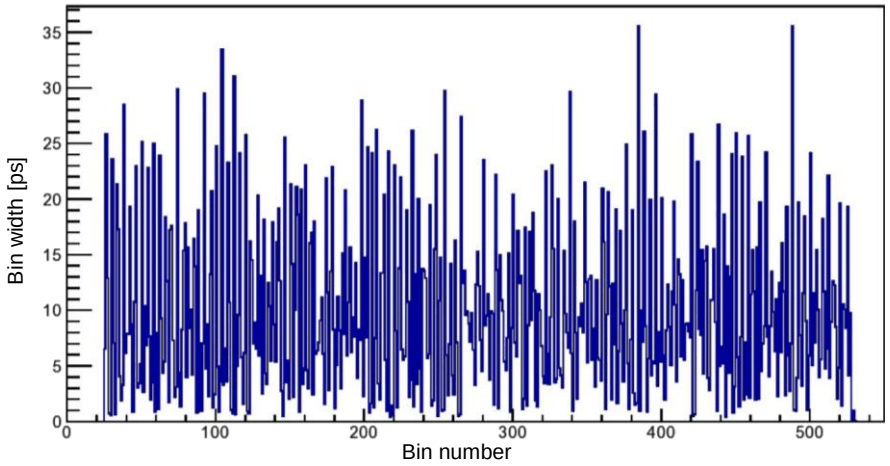
- Delay elements (bins) very non-uniform
  - Avg. bin width: 20 ps
  - Max. bin width: 50 ps
- Improvement through Wave Union Launcher [3]:
  - Send multiple transitions to delay line per hit signal
  - Trade-off: Precision vs. number of CH / dead time
- For two transitions
  - Avg. bin width: 10ps
  - Max. bin width: 35 ps
  - But non-linearity even worse



Wave union TDC: One hit, two (or more) transitions



Bin width histogram ("box diagram") of TDC with single transition [2]

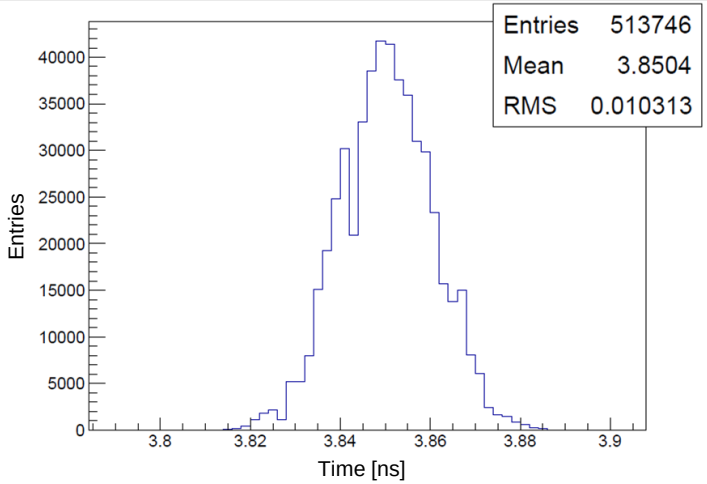


Bin width histogram of TDC with two transitions [2]

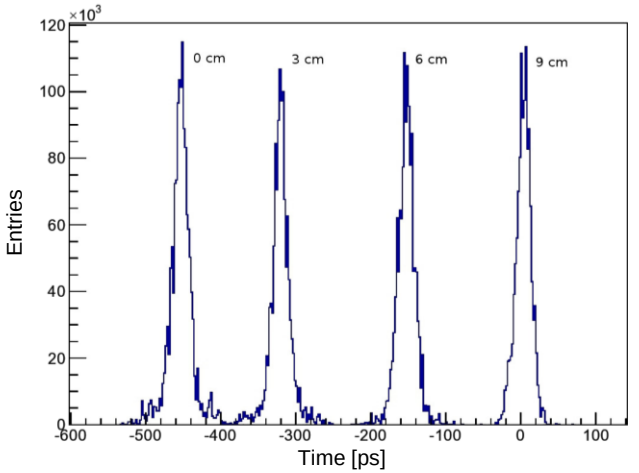
$$\text{Bin width}_n = T_{clock} * N_{bin} / N_{tot}$$

FPGA TDC Performance

- Precision (calibrated): 10 ps (between two channels w/o fitting or cuts of the data)
- Min. pulse width: 500 ps (for 100% efficiency)
- Dead time: T_d = 30 ns
- Up to 64 CH per FPGA (Lattice ECP3 150k)
- TDC can be configured for time-difference (ToF) or pulse width / time over threshold (ToT) measurements



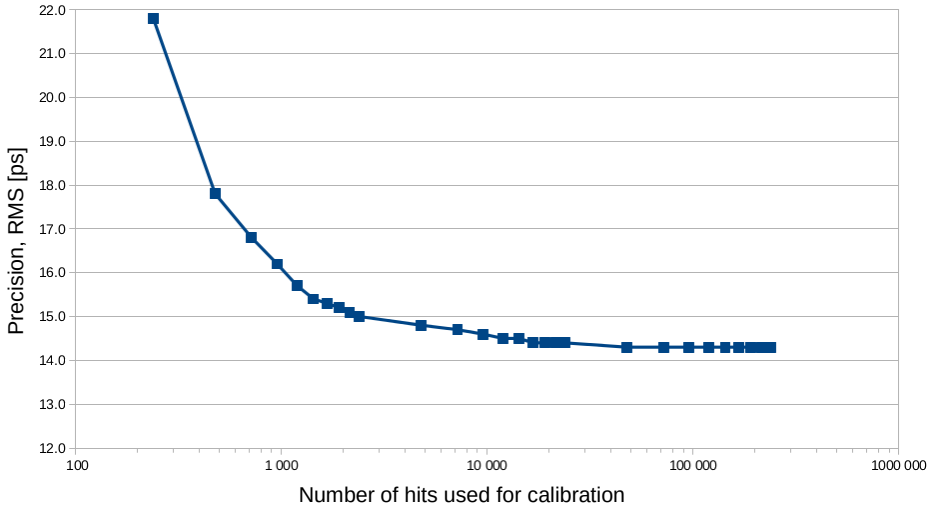
Time difference between two TDC channels for coincident events [1]



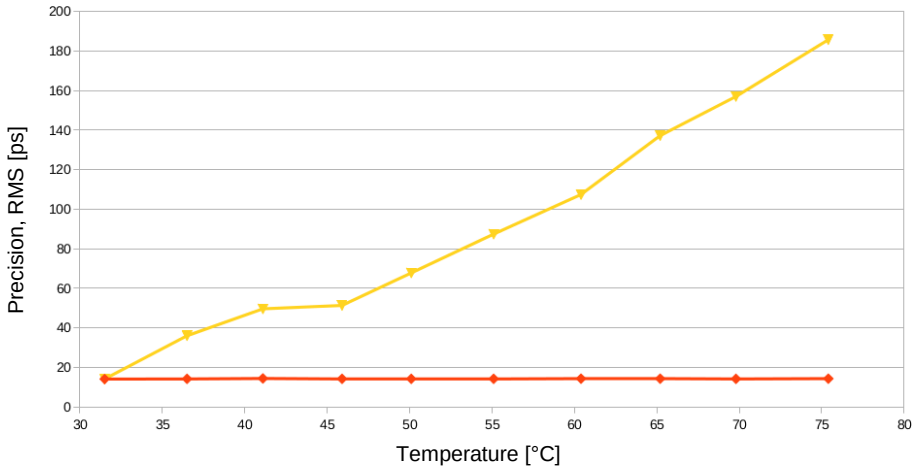
Measurement of signal delay for different cable lengths [1]

FPGA TDC Calibration

- Due to intrinsic non-linearity of delay line, calibration is necessary for best results
- Look-up table with bin widths calculated from set of random hits (“box diagram”)
  - $BW_n = T_{clock} * N_{bin} / N_{tot}$
- Delay line (bin widths) temperature dependent
- Calibration needs to be updated with temperature changes

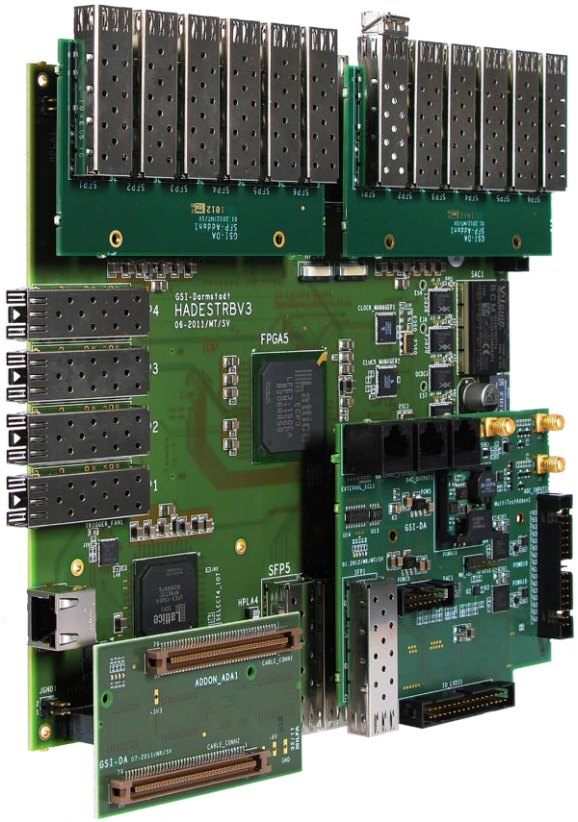


Precision vs. number of hits used for calibration [2]



Temperature dependence of precision with & w/o recalibration [2]

TDC Hardware – TRB Platform



- Platform for TDC measurements incl. data readout & analysis tools
- Central FPGA as trigger system & GbE controller
- 4 peripheral FPGAs with up to 256 TDC channels total
- Flexible with many add-ons & front-ends
  - Hubs to connect multiple TRBs
  - NIM/ECL input
  - ADC
  - Standard 100mil pins (LVDS in)
  - Adapters for various front-ends (FEEs)

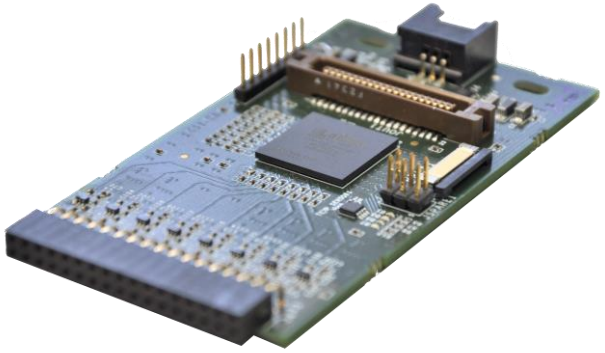
trb.gsi.de

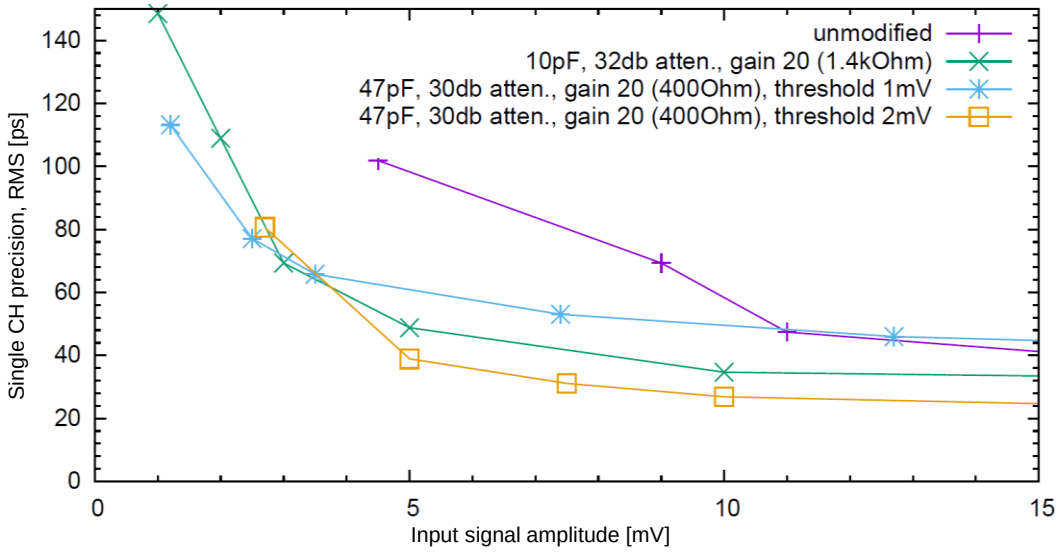
TDC Hardware – Front-Ends

PADIWA

Pre-amplifying & discriminating FEE

- 16 CH
- Amplification: 20-30 (depending on amplitude)
- Timing precision: ~30ps RMS
- Dynamic range: ~250
- Up to16 PADIWA per TRB

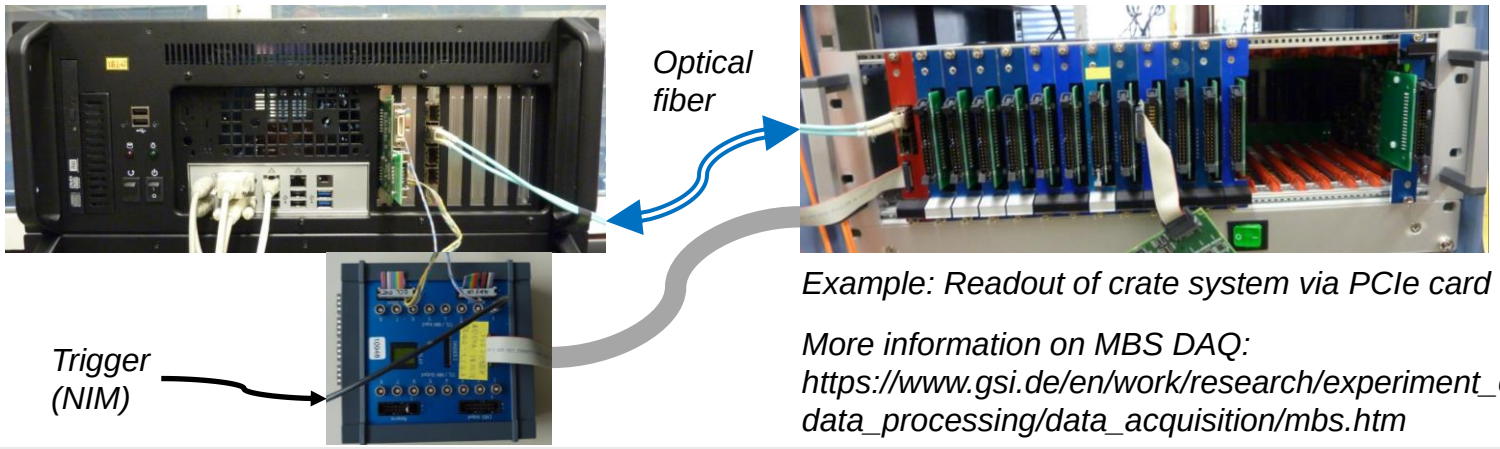




TRB-PADIWA timing performance

TDC Hardware – MBS DAQ System

- 2 Gb/s optical interface via PCIe card
  - Up to 4 optical readouts per PCIe card with 200 MB/s each
  - Slow control over same interface
- 19” crate system with up to 19 modules (smaller backplanes available)
- System is scalable and well extendable (VME readout included)
- Various front-end modules
  - 10 ps FPGA TDC System
  - 50/100 MHz 16 CH ADC modules (500 MHz planned)
  - 128 CH ~300 ps RMS TDC module coming soon



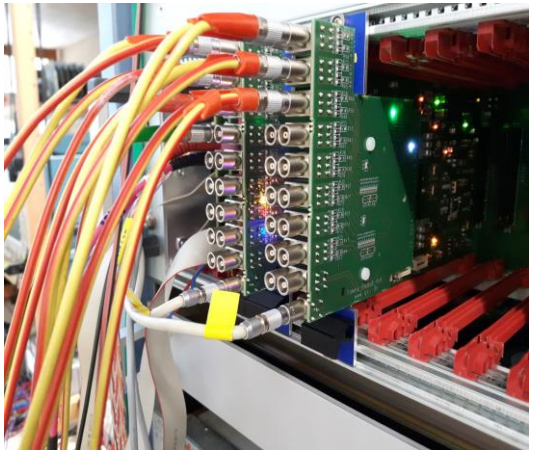
Example: Readout of crate system via PCIe card

More information on MBS DAQ: https://www.gsi.de/en/work/research/experiment_electronics/data_processing/data_acquisition/mbs.htm

TDC Hardware – TAMEX Front-End

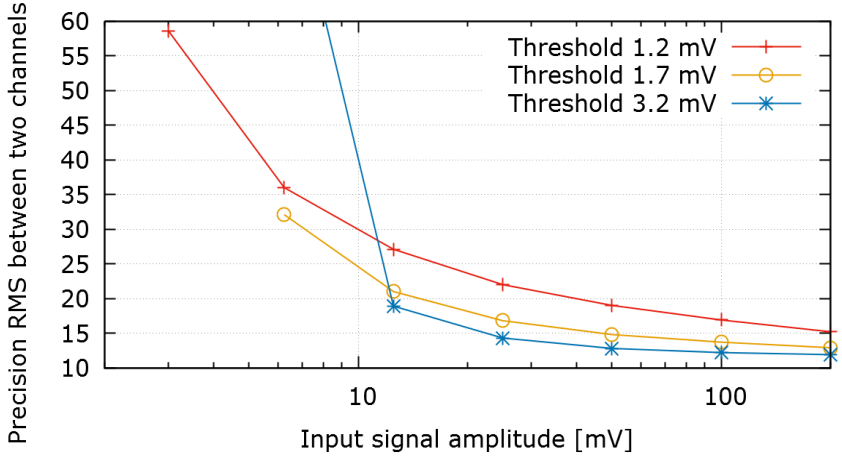
- TAMEX FPGA TDC system

TAMEX TDC module for 19” crate



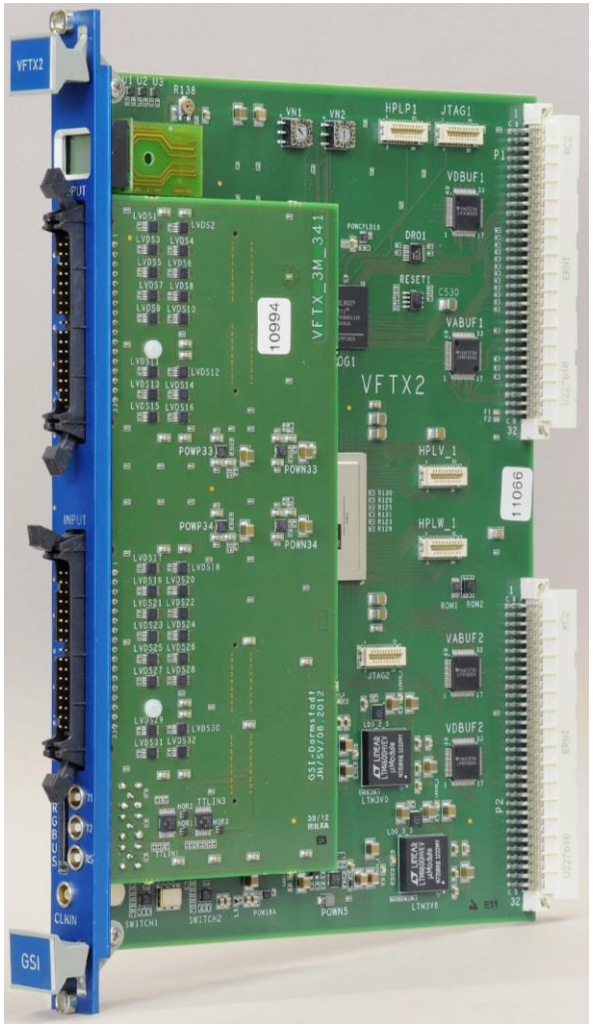
Modules with PADI discriminator front-ends in crate

- Up to 32 channels per FPGA / module (LVDS)
- Pre-amplifying & discriminating front-end with the PADI ASIC [4]
  - 16 CH leading & trailing edge
  - Channel dead time: T_d = 20ns
  - Amplification: ~200
  - Accepts signals down to few mV
  - External clock for synchronization



TAMEX-PADI timing performance

TDC Hardware – VME



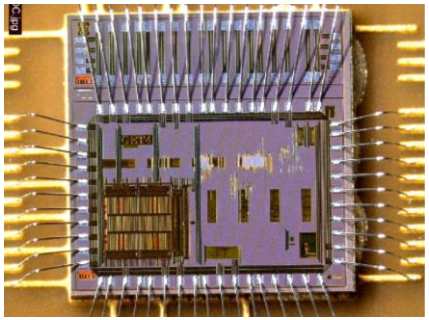
VFTX – VME FPGA TDC X=10ps

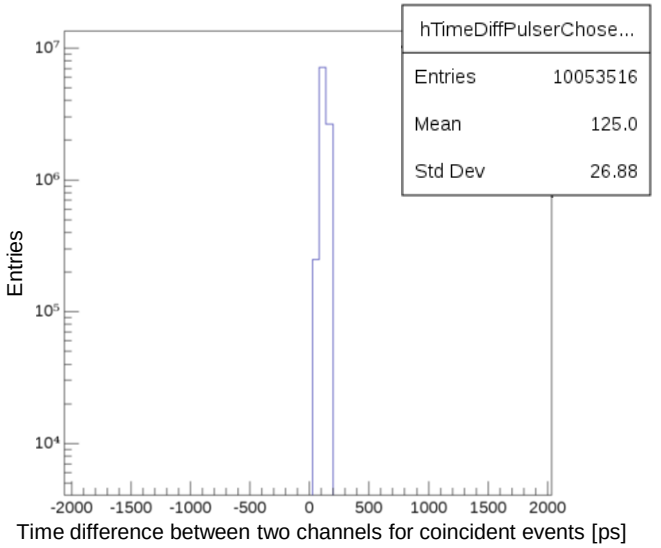
- Inputs: LVDS, ECL, NIM
- Different TDC implementations available:
  - 16 CH, 7 ps RMS leading or trailing edge
  - 32 CH, 10 ps RMS leading or trailing edge
  - 16 CH, 10 ps RMS leading and trailing edge (ToT)
- Channel dead time:
  - 10 ps designs: T_d = 40 ns
  - 7 ps design: T_d = 300 ns
- Synchronization of multiple modules via external 200 MHz clock

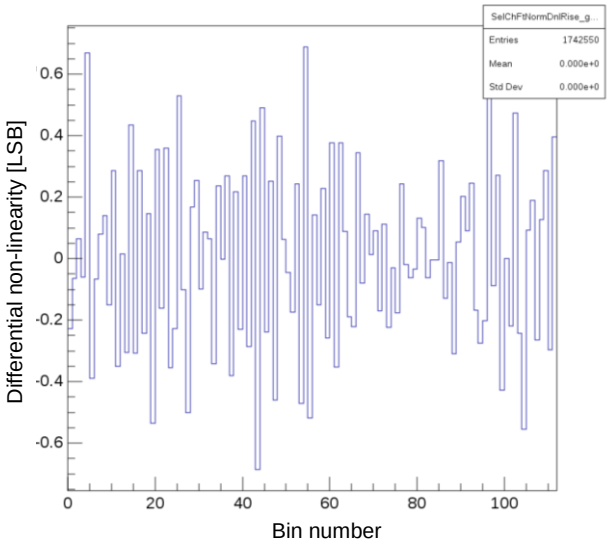
GET4 TDC ASIC

GET4 – **G**SI **E**vent driven **T**DC **4** CH

- 4 CH LVDS in
- Delay line with 55 ps binning
- Diff. non-linearity: better than +/- 1 LSB
- Precision: ~26 ps (w/o calibration)
- Dead time: 3.2 ns
- Min. pulse width: 500 ps
- Leading edge & ToT measurement
- Free-streaming
- Radiation hardened







More information:
https://wiki.gsi.de/pub/EE/GeT4/get4.pdf

Questions?

Thank you for your attention!

Contacts:
General / TDC: Henning Heggen – h.heggen@gsi.de
TRB Platform: Michael Traxler – m.traxler@gsi.de
MBS DAQ System: Nikolaus Kurz – n.kurz@gsi.de
GET4 ASIC: Holger Flemming – h.flemming@gsi.de

References

[1] C. Ugur *et al* 2016 *JINST* **11** C01046
A novel approach for pulse width measurements with a high precision (8 ps RMS) TDC in an FPGA

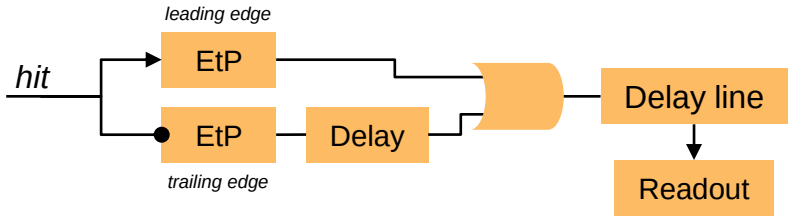
[2] C. Ugur *et al* 2013 *IEEE Nordic Mediterranean Workshop on TDCs*
264 Channel TDC platform applying 65 channel high precision (7.2 ps RMS) FPGA based TDCs

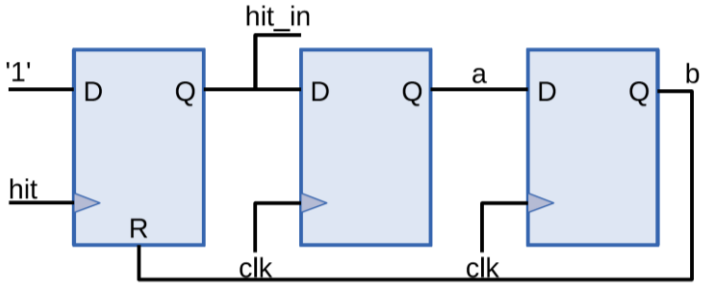
[3] J. Wu and Z. Shi 2008 *IEEE Nucl. Sci. Symp. Conf. Rec.* 3440
The 10-ps Wave Union TDC: Improving FPGA TDC Resolution beyond Its Cell Delay

[4] M. Ciobanu *et al* 2014 *IEEE Transactions on Nucl. Sci.* **61** No. 2 105
PADI, an Ultrafast Preamplifier - Discriminator ASIC for Time-of-Flight Measurements

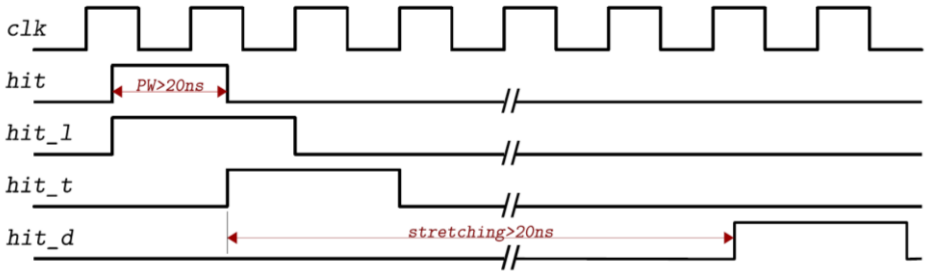
Stretcher & Single CH ToT Measurement

- Delay line requires input signals wider than one clock period
- Semi-asynchronous edge-to-pulse (EtP) stage at every input
- Delay circuit allows serial measurement of both edges of a pulse in same CH
  - More channels but longer dead time: 30ns → 70ns





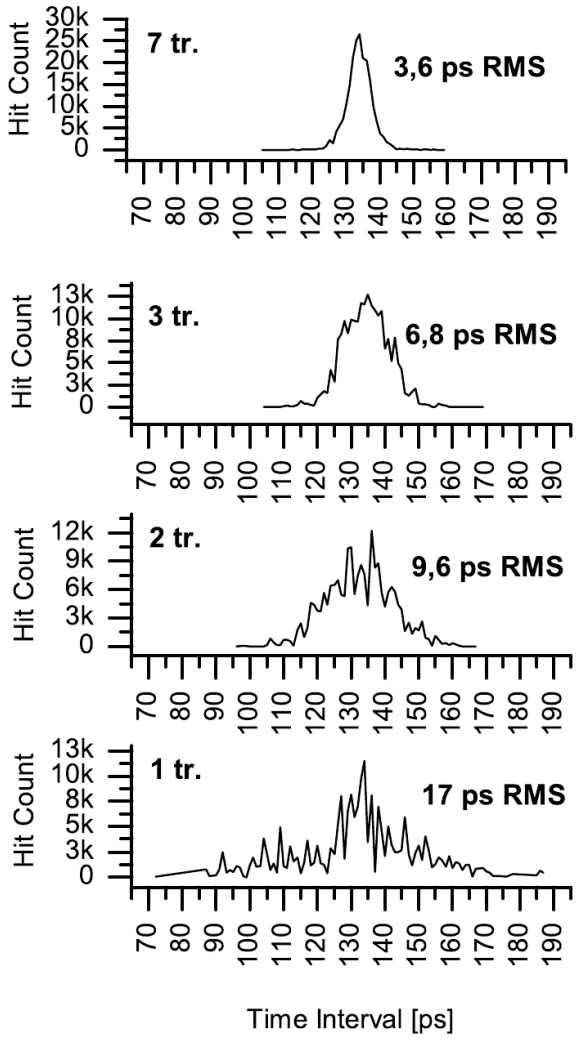
Semi-asynchronous pulse stretcher [1]



Timing diagram of the ToT measurement with stretcher [1]

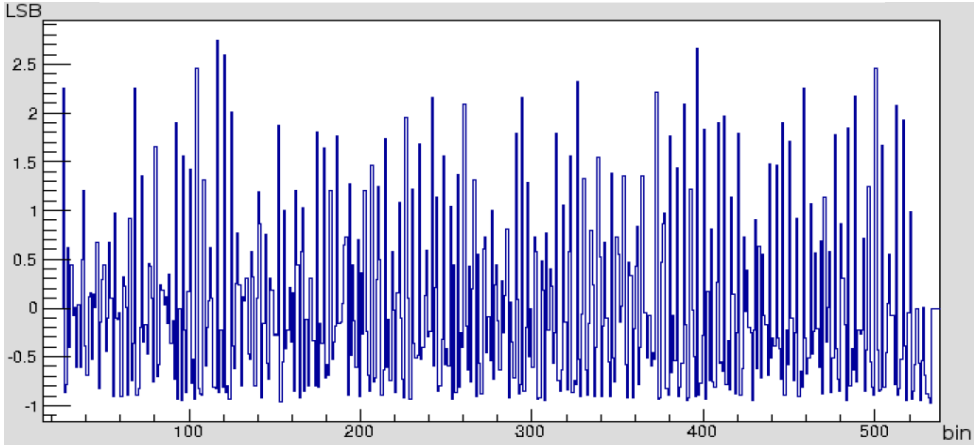
FPGA TDC Potential

- FPGA TDCs can be very precise
- But everything comes at a price
- Trade-off:
  - Precision
  - Number of CH (FPGA resources)
  - Channel dead time (conversion time)

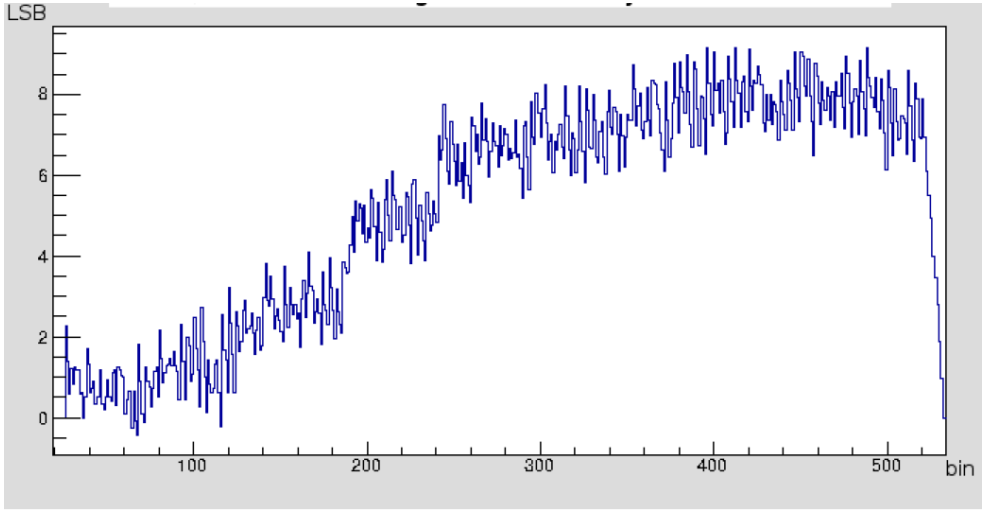


Measured precision for different TDC implementations on VIRTEX4 FPGA

FPGA TDC Non-Linearity

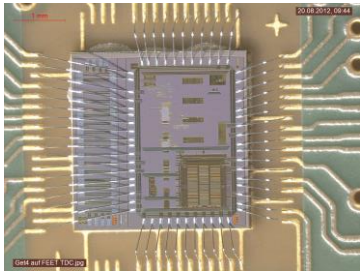


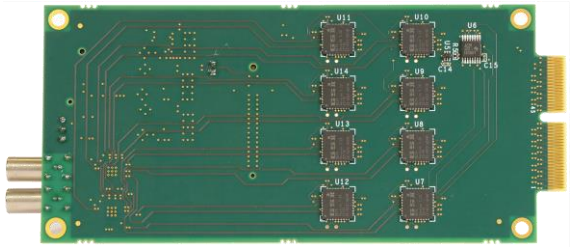
Differential non-linearity of the FPGA TDC [2]



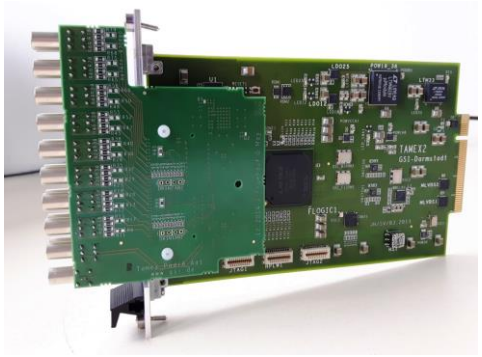
Integral non-linearity of the FPGA TDC [2]

TDC – ASIC vs. FPGA-TDC





GET4 ASIC (GSI EE-ASIC)



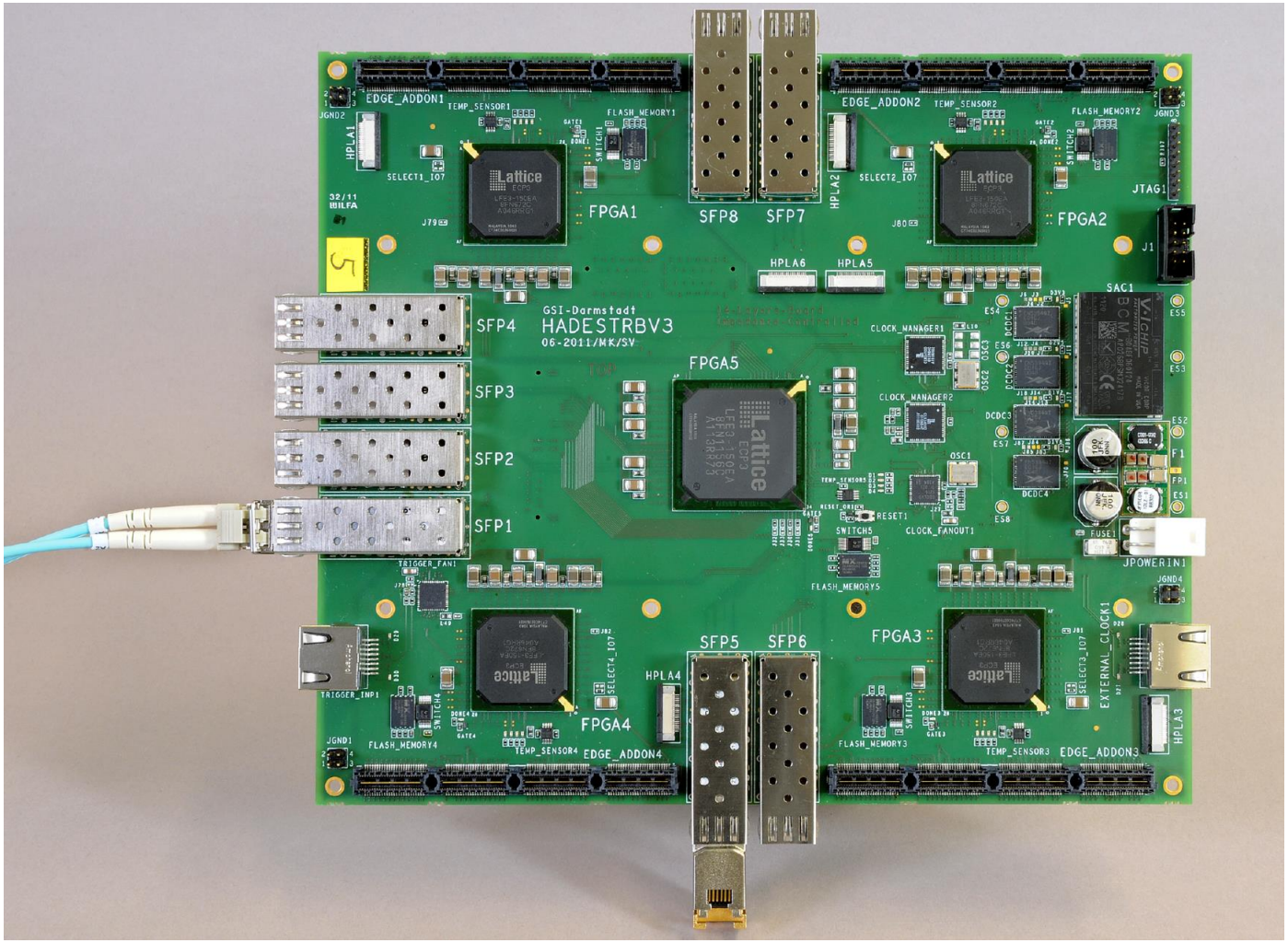
ASIC

- Radiation tolerance
- Power consumption
- Self-calibrated
- Dead time 3.2ns
- Price
- Availability can be an issue
- Flexibility

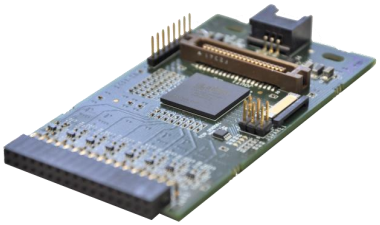
FPGA-TDC

- High precision
- Flexibility/ Firmware updates
- Availability
- Price
- Power consumption
- Calibration necessary
- Dead time 20ns (or higher)

TRB3


EDGE_ADDON1
EDGE_ADDON2
EDGE_ADDON3
EDGE_ADDON4
FPGA1
FPGA2
FPGA3
FPGA4
FPGA5
SFP1
SFP2
SFP3
SFP4
SFP5
SFP6
SFP7
SFP8
GSI-Darmstadt
HADESTRBV3
06-2011/MK/SV
JTAG1
JPOWERIN1
EXTERNAL_CLOCK1
TRIGGER_FAN1
TRIGGER_INP1
FLASH_MEMORY1
FLASH_MEMORY2
FLASH_MEMORY3
FLASH_MEMORY4
FLASH_MEMORY5
TEMP_SENSOR1
TEMP_SENSOR2
TEMP_SENSOR3
TEMP_SENSOR4
CLOCK_MANAGER1
CLOCK_MANAGER2
CLOCK_FANOUT1
SAC1
RESET1
SWITCH5
FUSE1
HPLA1
HPLA2
HPLA3
HPLA4
HPLA5
HPLA6

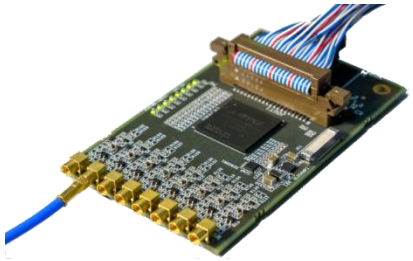
TDC Hardware – Front-Ends



PADIWA

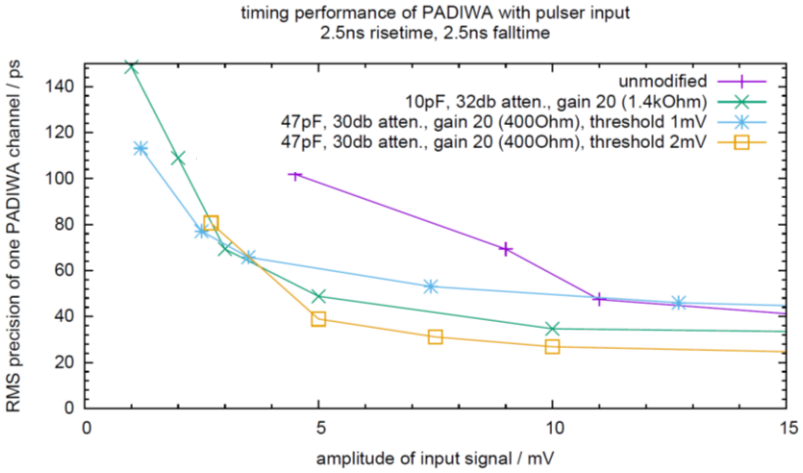
Pre-amplifying & discriminating FEE

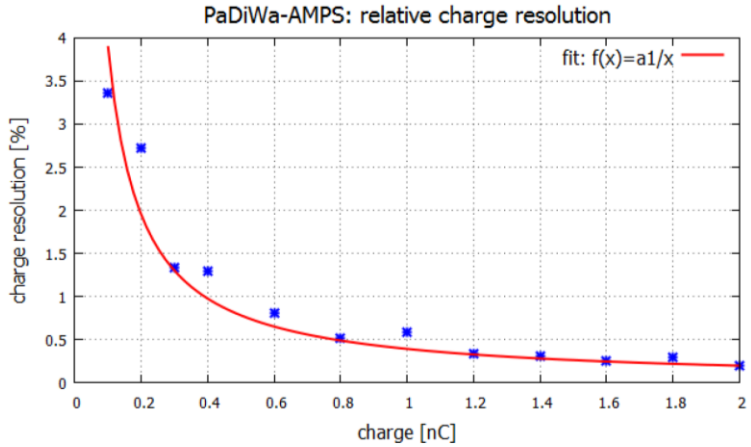
- 16 CH
- Timing precision: ~30ps RMS
- Amplification: 20-30 (depending on amplitude)
- Dynamic range: ~250



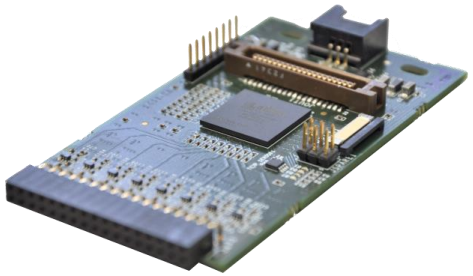
PADIWA-AMPS

- PADIWA + Charge Integrator
- Charge measurement by ToT
- 8 CH
- Rel. charge resolution up to 0.5%

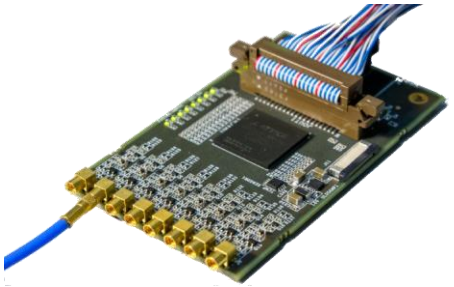




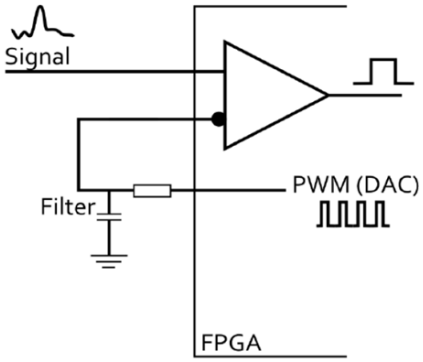
TDC Hardware – Front-Ends

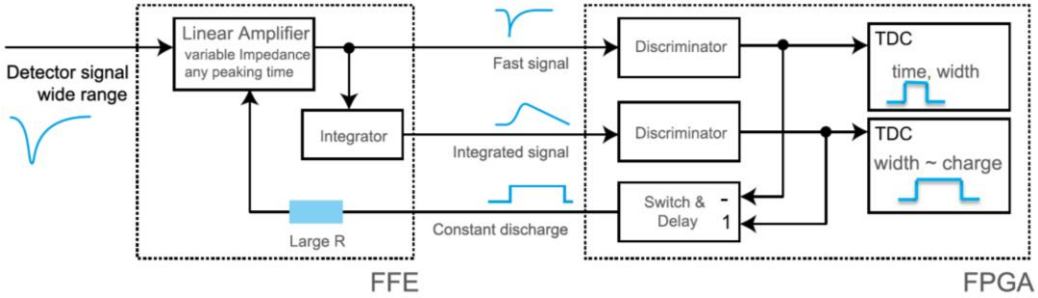


PADIWA
Pre-amplifying & discriminating FEE (16 CH)

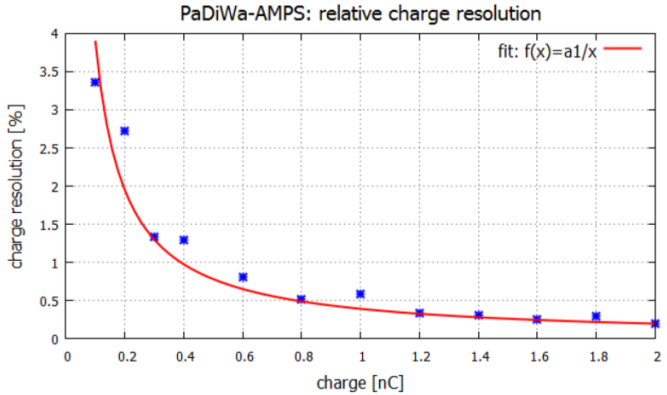


PADIWA-AMPS
Charge-integrating FEE for charge measurements by ToT (8 CH)





- Timing precision: ~25ps
- Amplification: ~20-30 (depending on amplitude)
- Dynamic range: ~250



Precision, Resolution, Accuracy?