PAUL SCHERRER INSTITUT

PSI

SLS2 BPM & Feedback Team :: Paul Scherrer Institut

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RFSoC-based digital signal processing for SLS2.0 multi-bunch feedback system

I.FAST Workshop 2024 on Bunch-by-Bunch Feedback Systems and Related Beam Dynamics,

4th March 2024, KIT, KARA, Karlsruhe, Germany

Introduction: Accelerator Feedbacks and Measurement Systems Group

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Goran Marinkovic
Engineer (electronics/informatics), since 2005

Pedro Baeta
Engineer (electronics), since 2020

Outline

- Introduction
- RF System-on-Chip (RFSoC)
- SLS 2.0 Multi-bunch Feedback (MBFB)
- Status & Outlook

Introduction: SLS Upgrade – The SLS 2.0

Swiss Light Source (SLS) Upgrade, the SLS 2.0 project

- Replacement of the SLS storage ring, providing up to 60-fold higher brightness for hard X-rays.
- Modernization of aging systems, including the bunch-by-bunch feedback:
  - RFSoC as platform to implement the SLS 2.0 multi-bunch feedback (MBFB) .
- 1st SLS 2.0 beam is planned for 1/2025 [1] .

Figure 1 - Interior view of the Swiss Light Source (SLS) In user operation since 2001.

Introduction: Multi-bunch Feedback Upgrade

- **SLS 1.0 MBFB system:**
- PSI-design, commissioned in 2006
- Stabilize beam and avoid beam loss due to coupled bunch-instabilities (ion instabilities, resistive wall impedance, cavity HOM, etc.)
- **Diagnostic tool:**
  - Coupled Bunch Mode (CBM) spectrum display (find source of beam instabilities)

- **SLS 2.0 MBFB system:**
- **1st Milestone:**
  - Replacement of the old VME-based ADC/FPGA/DAC MBFB system* with RFSoC-based solution [1].
- **2nd Milestone:**
  - Replace analog down/upconverter for BPM/kicker signals with digital solution.
  - **Advanced Diagnostic tools:**
    - Add Excitation-damping measurement
    - Add Parasitic (X/Y/S) tune measurement
    - Other ideas (vertical emittance control/feedback, …)

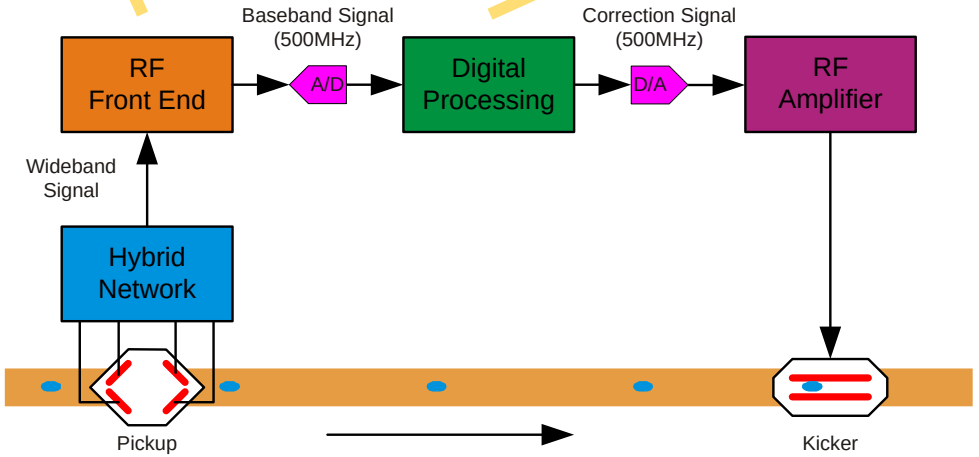
Introduction: SLS 1.0 Multi-bunch Feedback

SLS 1.0 MBFB system:

- **PSI Design***
- **RF frond-end:**
  - Commercial analog front-end with down-converter (from 1.5± 0.25 GHz to baseband).
- **Digital back-end:**
  - 500 MS/s 8-bit VME-based ADC and DAC cards with MBFB algorithm deployed on a Xilinx Virtex 2.
- **Analog DAC signal-conditioning:**
  - For the longitudinal MBFB plane, an analog up-converter transforms the baseband (0-250 MHz) DAC signal to 1.25-1.5 GHz for the power amplifier of the longitudinal kickers.

I-tech RFFE

VME-based ADC/DAC cads with FPGA



Functional block diagram of the SLS1.0 MBFB
*M. Dehler, P. Pollet, G. Marinkovic et al. [2]

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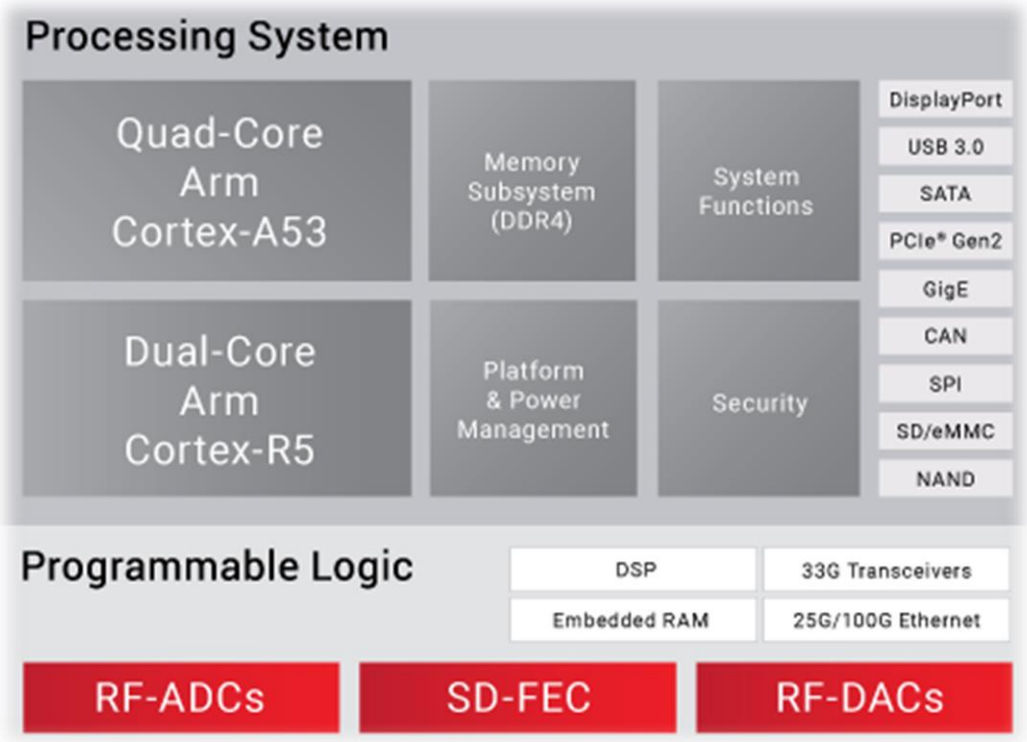
RF System-on-Chip (RFSoC Gen1)



Zynq® UltraScale+™ RFSoC Gen1 [3]

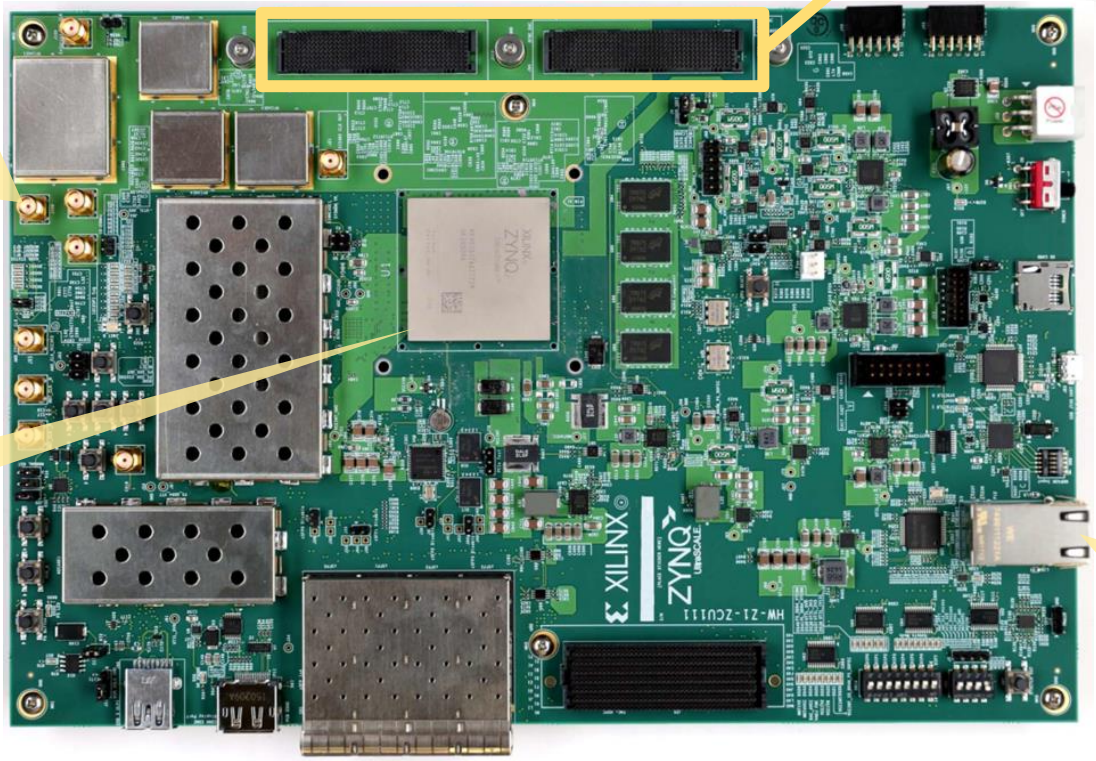
- **Integrates:**
  - Multiple CPUs
  - Resourceful FPGA Fabric
  - GHz-range ADCs and DACs
  - Various data storage and communication interfaces
- **Low ADC to DAC Latency**
  - 8xADCs (12-bit up to 4.0 Gs/s): ~46-101 ns
  - 8xDACs (14-bit up to 6.5 Gs/s): ~24-116 ns
  - Loop-back latency: ~70-217 ns
  - Stable and reproducible
    - (i.e. after a power cycle).*
- **Stable temporal sample alignment among ADCs and DACs**
  - Multi-tile synchronization (MTS) mode.

*with suitable firmware & software design.

ZCU111 Evaluation Kit

FMC-XM-500

RF-FMC connector



Machine reference clock input (f_{RF} = ~500 MHz) synchronizes data converters and programmable logic (PL)*

Add-on card breaks down the RFSoC ADCs/DACs inputs/outputs to SMA connectors

Zynq® UltraScale+™ RFSoC Gen1 XCZU28DR

Ethernet for communication with control system network

Xilinx/AMD ZCU111 Evaluation Kit featuring the RFSoC Gen1 (XCZU28DR)

*Adaptation of the ZCU111 evaluation board

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SLS2.0 MBFB : Hardware – Milestone 1

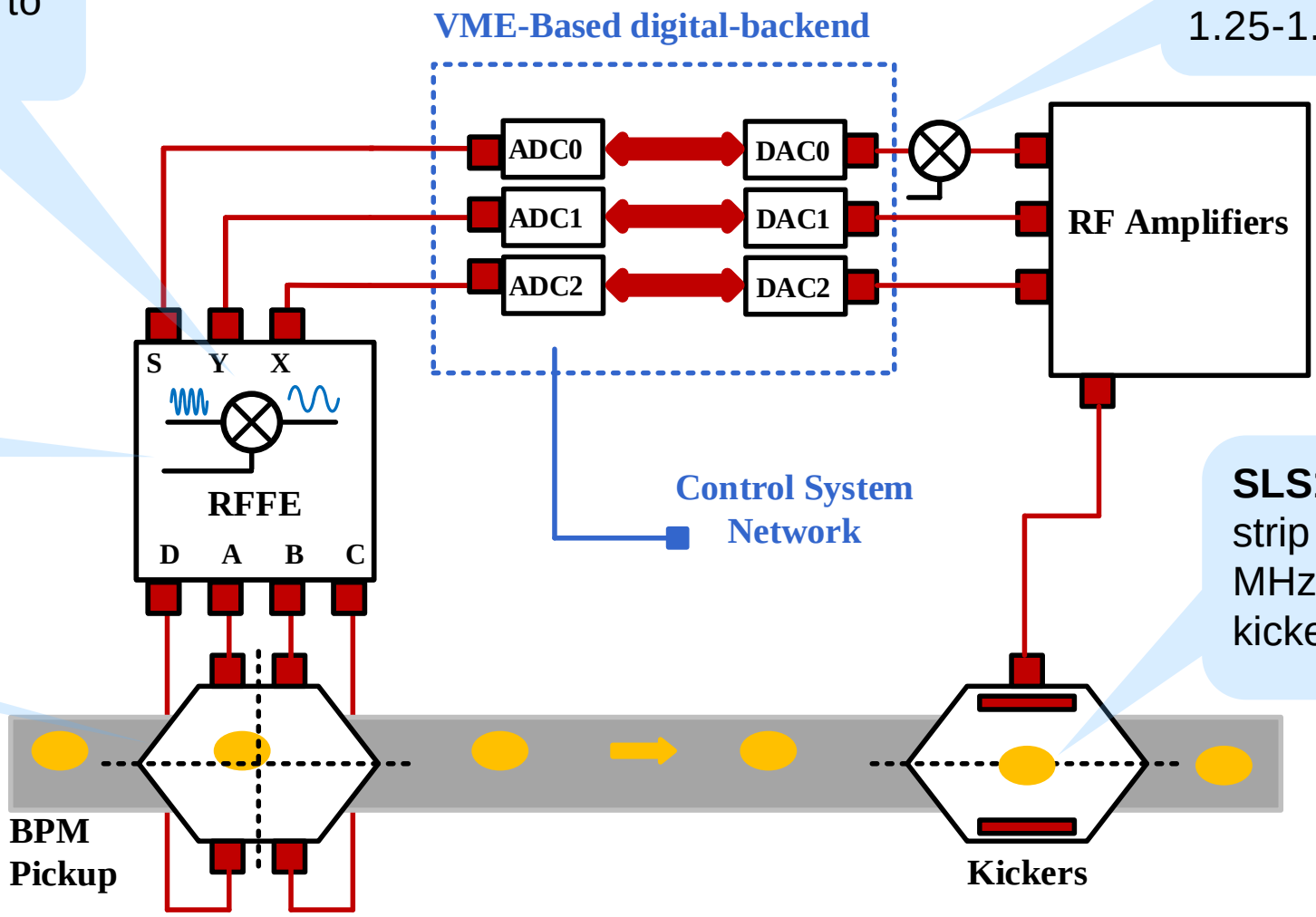
Down-converter: 1.5± 0.25 GHz to baseband

Up-converting mixer: baseband (0-250 MHz) to 1.25-1.5 GHz

I-tech RFFE front-end

Button BPM

SLS1.0: 2 transverse strip line kickers (0-250 MHz) & longitudinal kicker (1.25-1.5 GHz)



VME-based ADC/FPGA/DAC hardware of SLS 1.0 MBFB.

SLS2.0 MBFB : Hardware – Milestone 1

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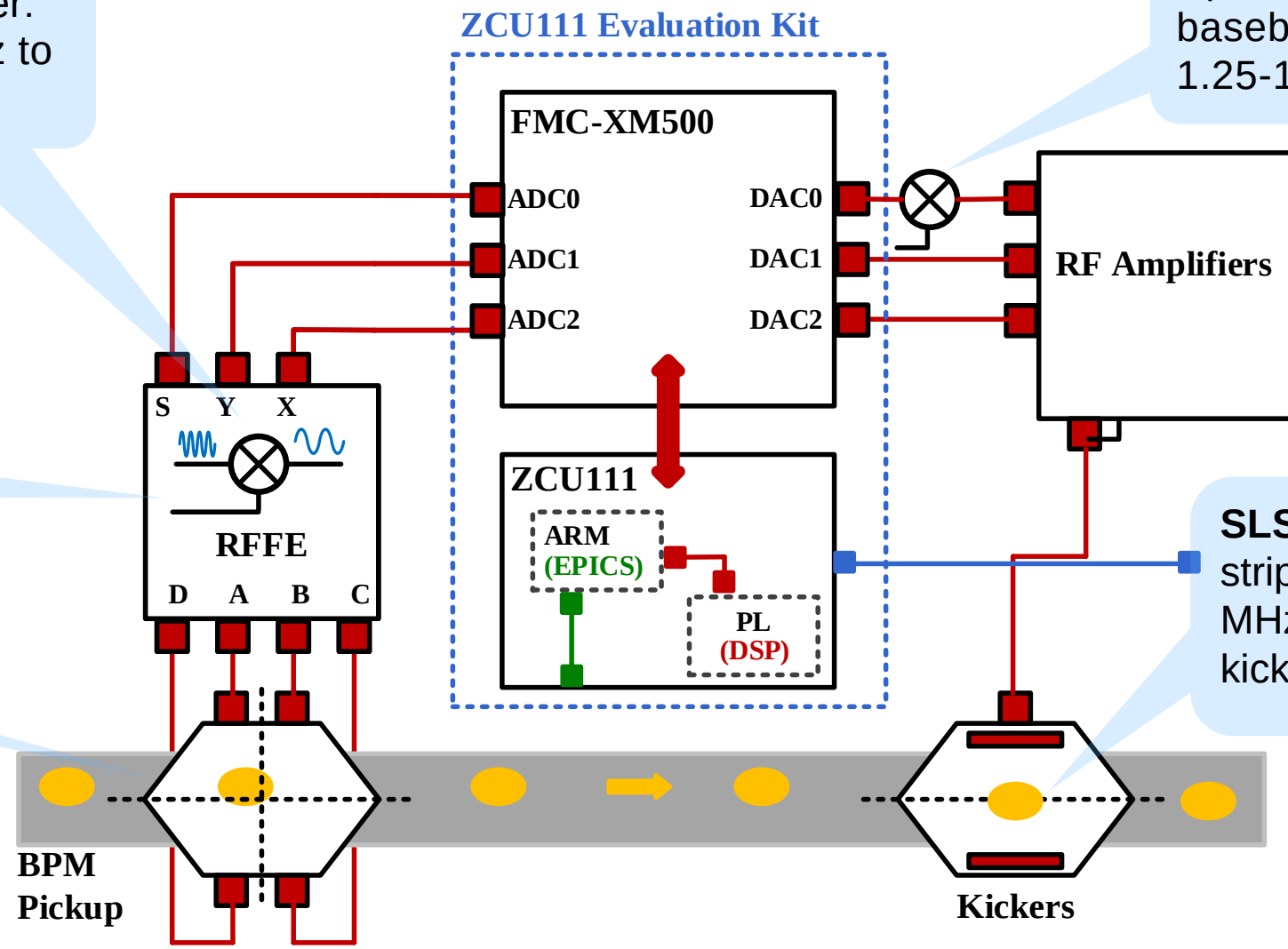
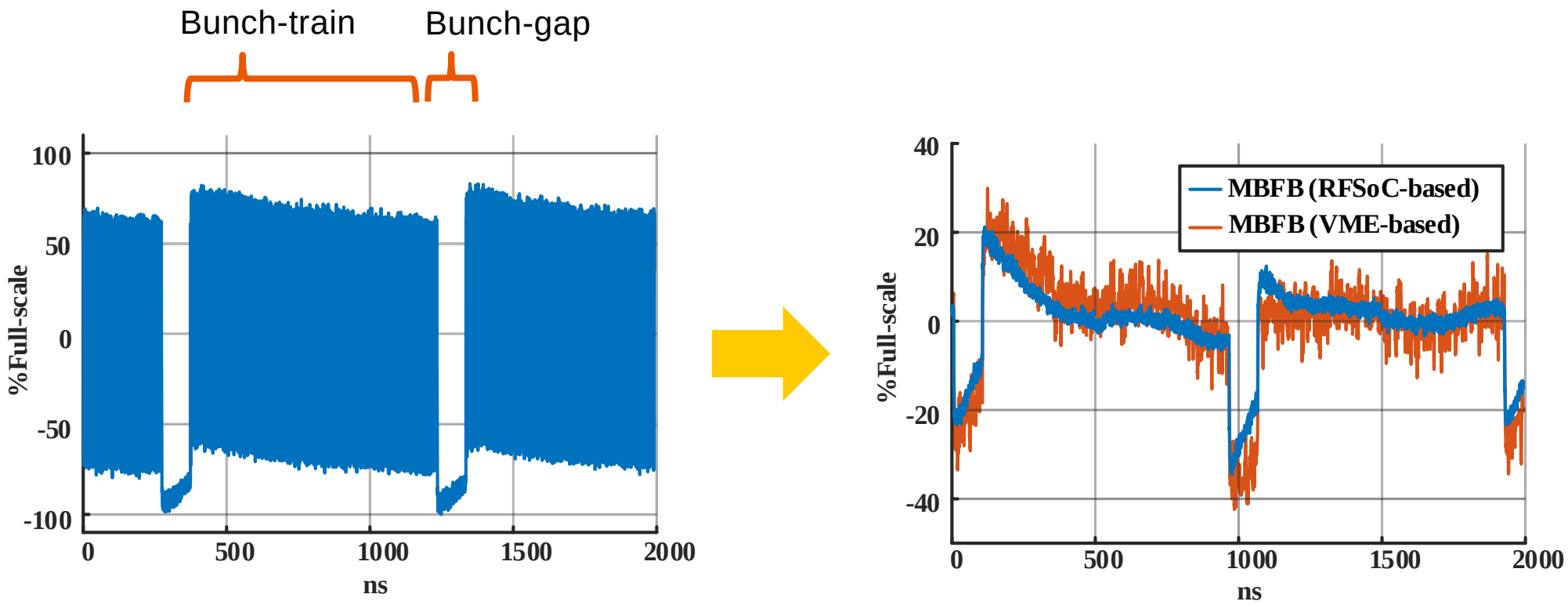


SLS1.0: 2 transverse strip line kickers (0-250 MHz) & longitudinal kicker (1.25-1.5 GHz)

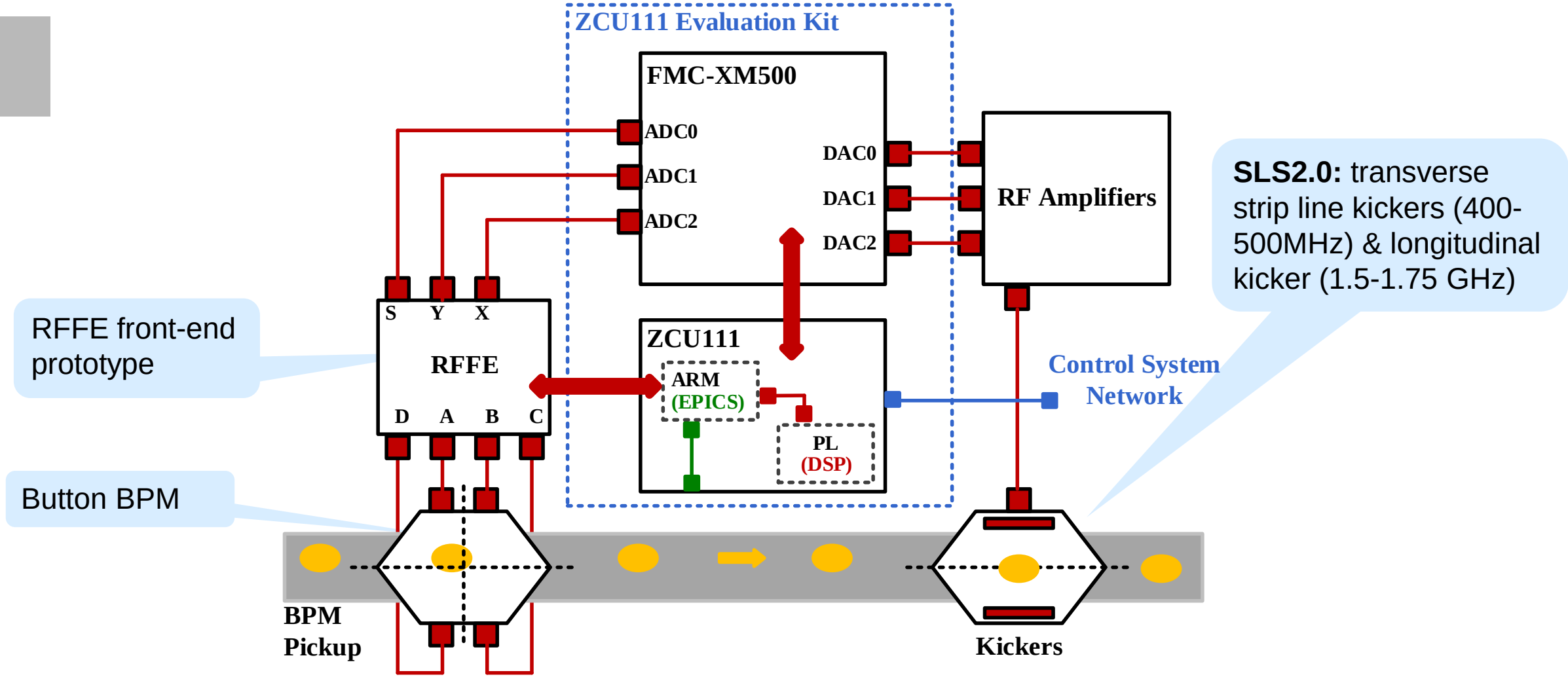
Hardware setup for testing the RFSoC-based MBFB at SLS 1.0.

SLS2.0 MBFB : Hardware – Milestone 1



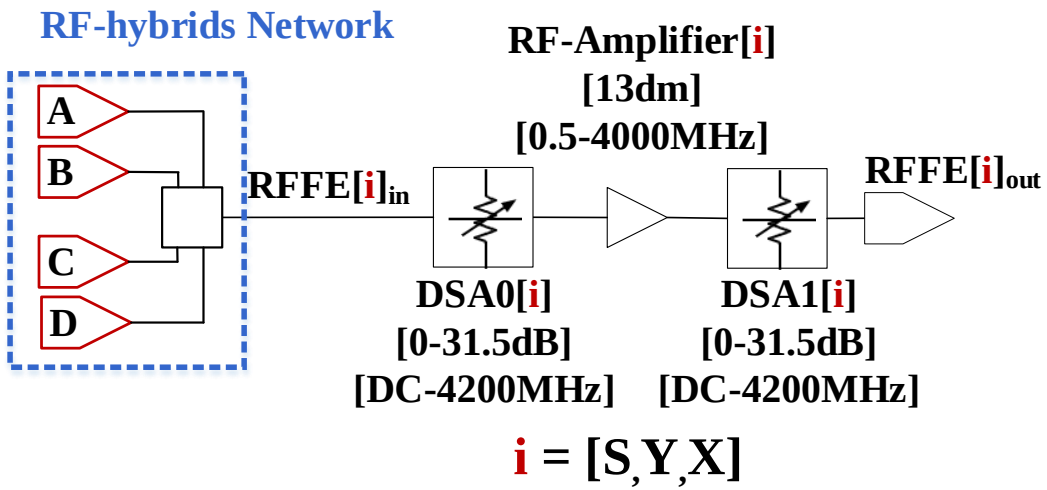
Comparison of the open-loop response (horizontal plane) between the RFSoC and the VMEbus-based MBFB system (Lab Tests).

SLS2.0 MBFB : Hardware – Milestone 2

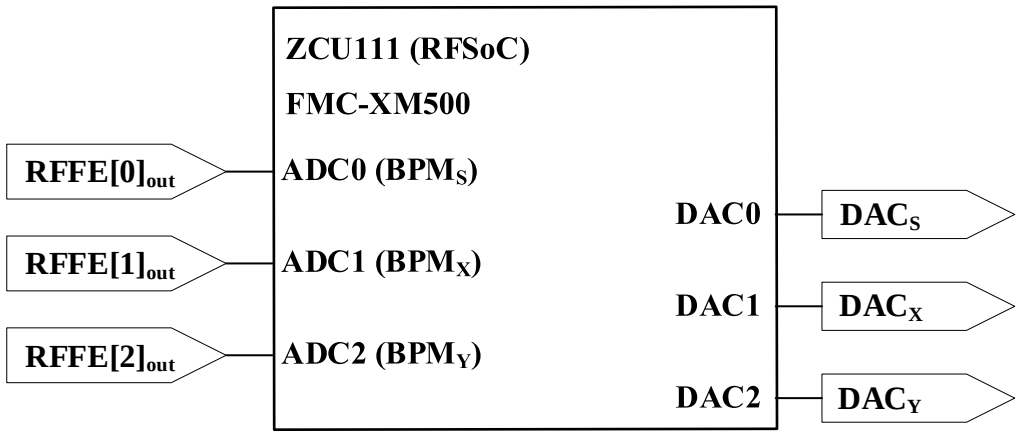


Hardware setup for testing the RFSoC-based MBFB at SLS1.0 with direct sampling.

SLS2.0 MBFB – Hardware for direct sampling

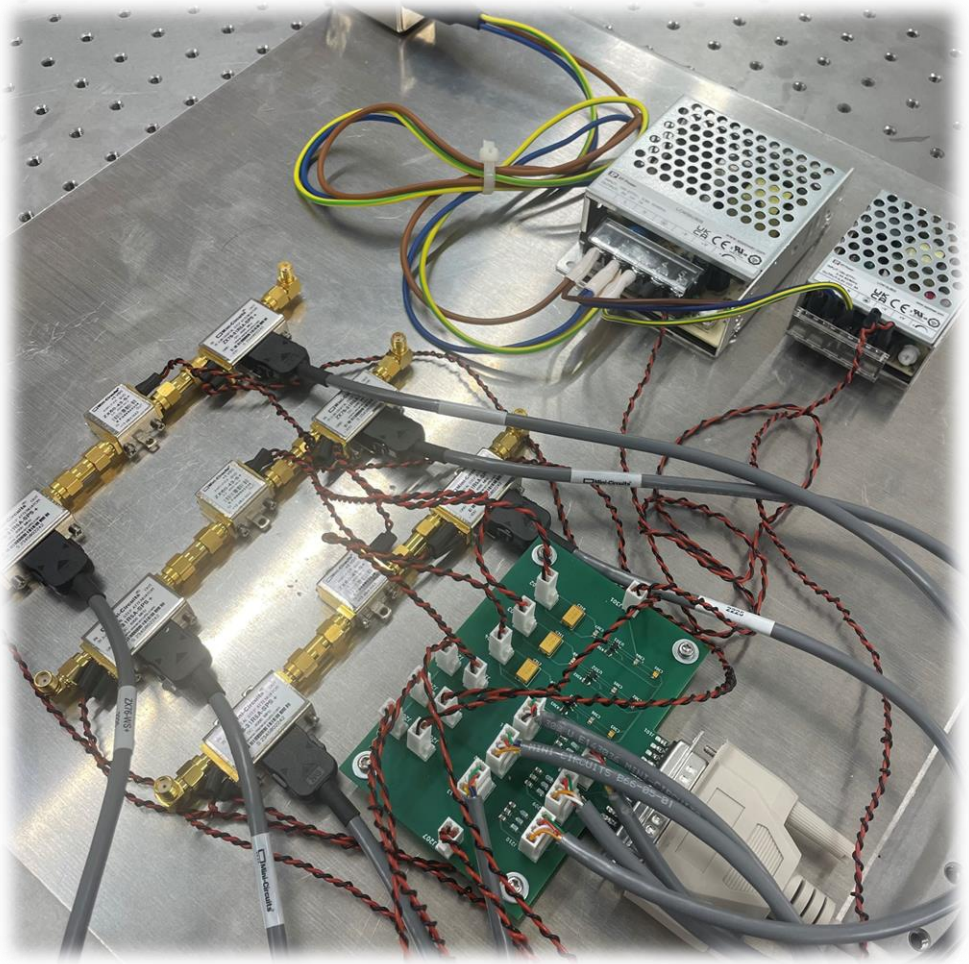


New RF Front-end (Prototype)

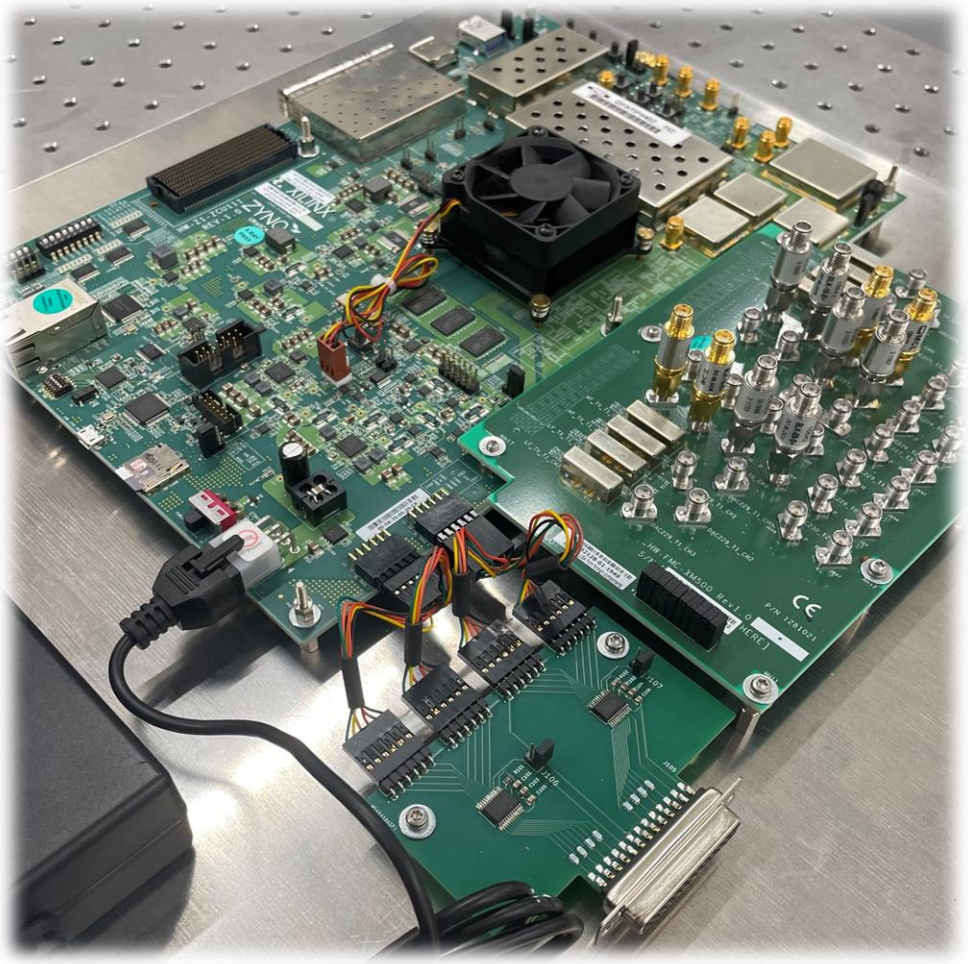


New Digital Back-end (Prototype)

SLS2.0 MBFB: Hardware – Milestone 2



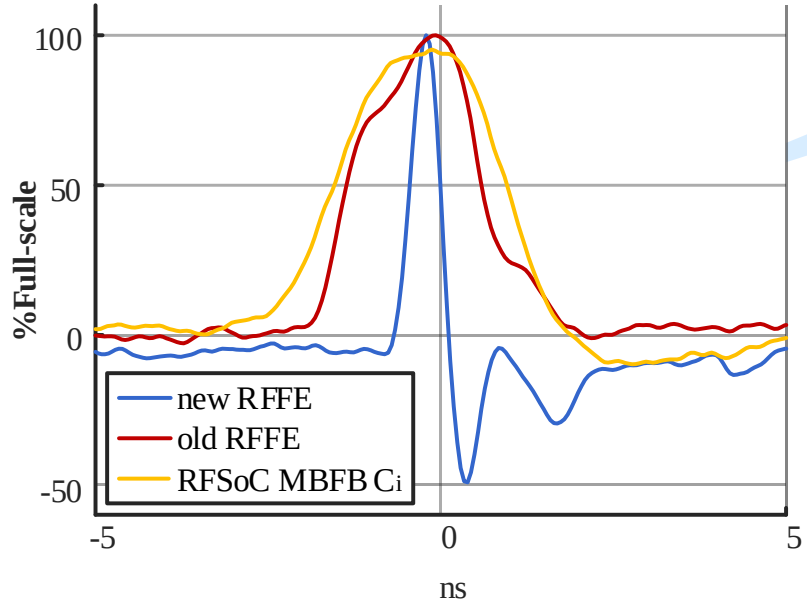
New RF Front-end (Prototype)



New Digital Back-end (Prototype)

SLS2.0 MBFB : Hardware – Milestone 2

Beam test with only one single bunch in SLS 1.0 storage ring



Oscilloscope measurement of signals for MBFB with old & new RFFE:

- Blue: X output of new direct sampling RFFE (optional lowpass removed)
- Red: X output of legacy MBFB (down converting) RFFE
- Yellow: RFSoC DAC output for X MBFB with new direct sampling RFFE

SLS2.0 MBFB: Firmware & Software

ADC/DAC PL data stream 8 samples in parallel @ 500MHz

EEVR trigger the system and provides information for bunch indexing

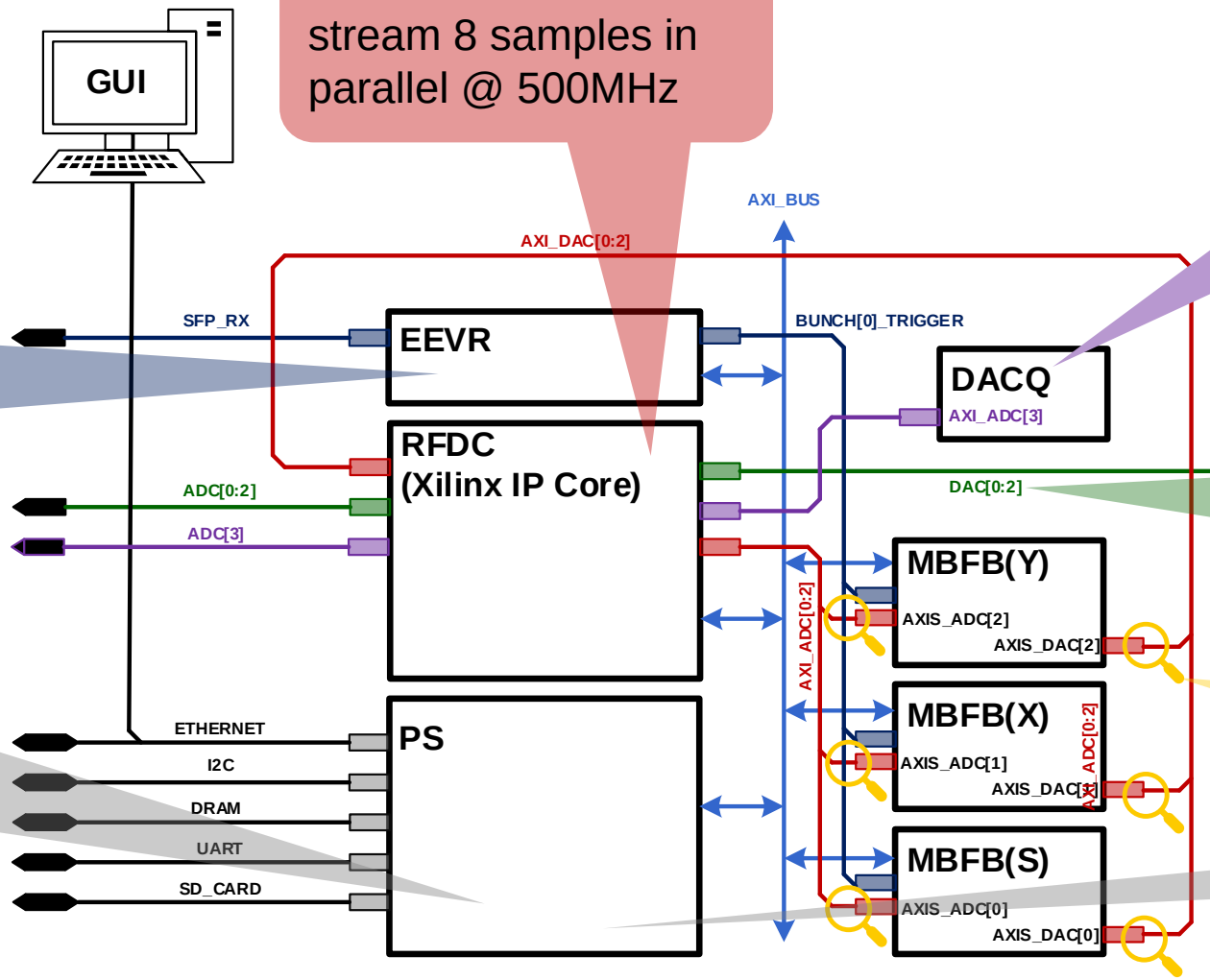
Bunch-charge, Bunch-Arrival time and Couple Bunch Mode Spectrum calculation on the RPU

Sampling scheme increases the effective sampling rate of a single ADC. (By means of Interleaving)

MBFB ADC/DAC clock period = 1/8 of nominal bunch spacing. ($f_S = 8 \times f_{RF} =$ ~4Gs/s)

ADC / DAC data monitors

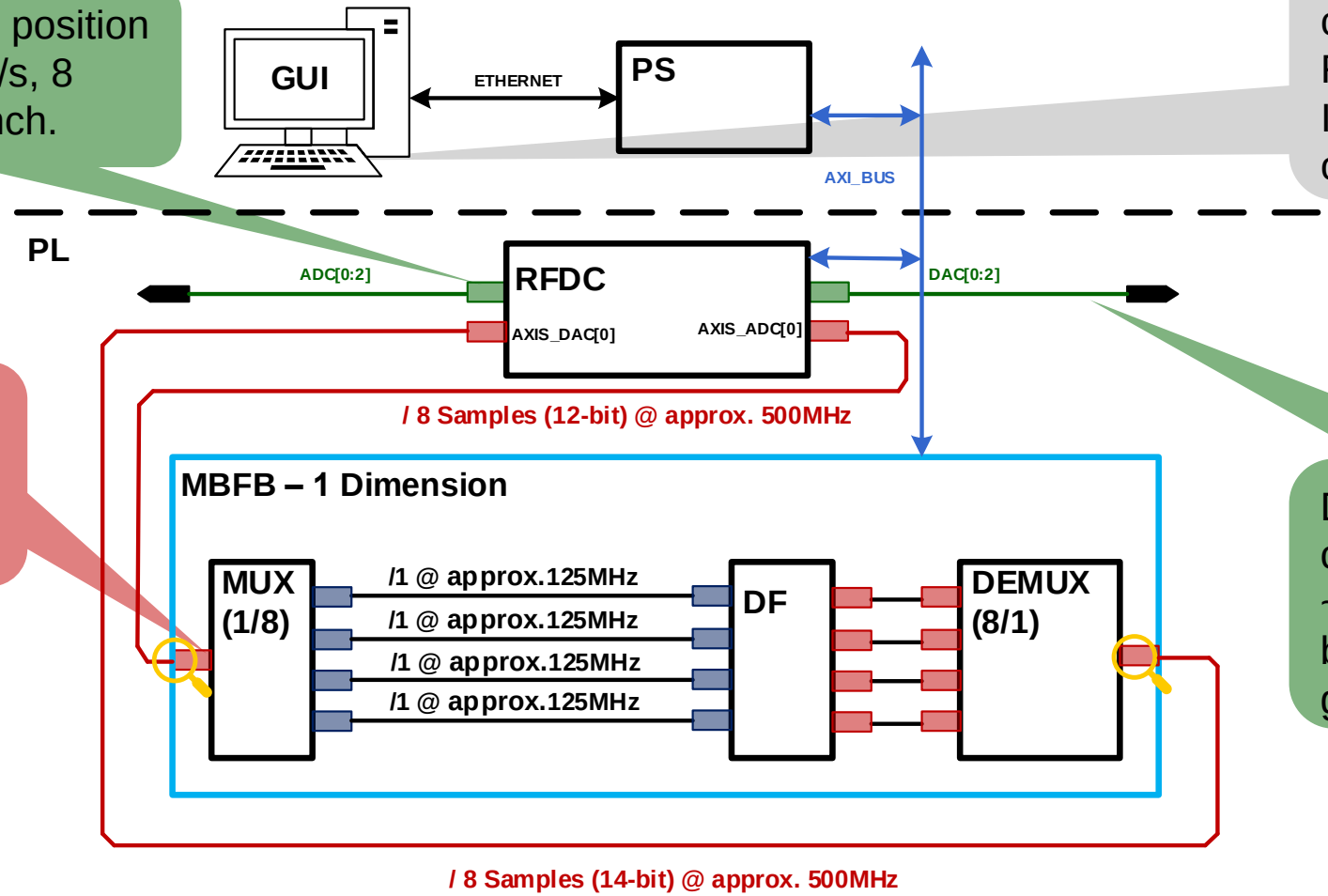
EPICS IOC running on the APU



SLS2.0 MBFB: Firmware & Software

ADC sample the position signals at ~ 4Gs/s, 8 samples per bunch.

User interface configures the MBFB Feedback via EPICS IOC channels running on RFSoC ARM CPU.

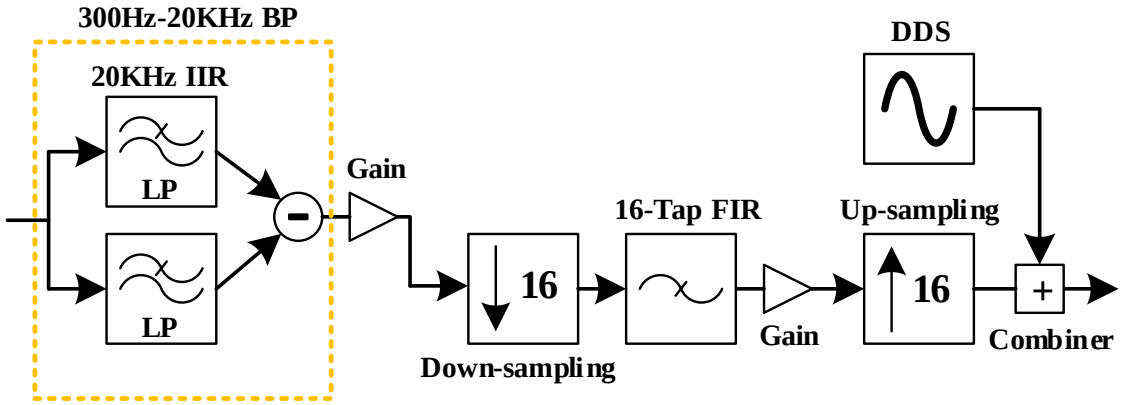


DSP path processes one out of eight samples and has data throughput of 500Ms/s

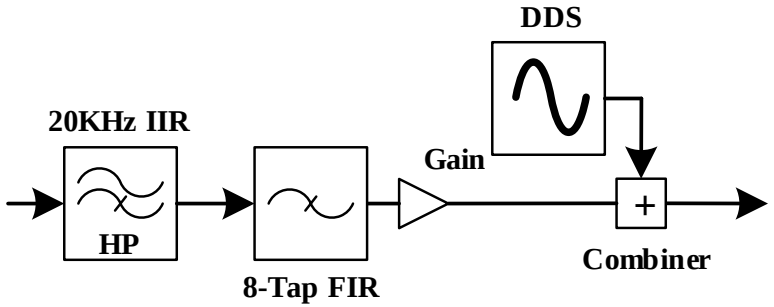
DAC generates the correction signals at ~4Gs/s, 8 samples per bunch, thus time granularity of 250ps

High-level block diagram of 1 dimension of the MBFB.

SLS2.0 MBFB: Firmware & Software

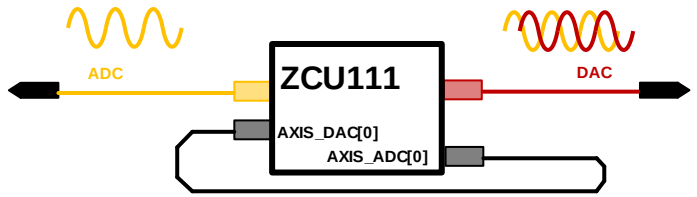


Digital Filter - Longitudinal dimension - S



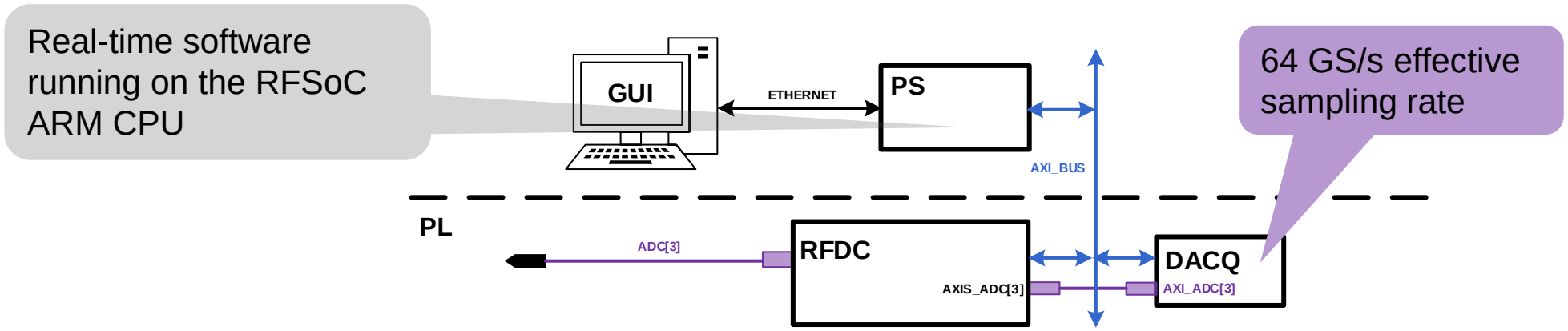
Digital Filter - Transverse dimensions – X and Y

Digital back-end latency



- ADC to DAC latency: 128.5 ns
- Long. MBFB Latency: 16’438 us
  - Total: 16.566 ms
- Trans. MBFB: Latency: 328ns
  - Total: 456.5 ns

SLS2.0 MBFB: Bunch-charge & Bunch-phase

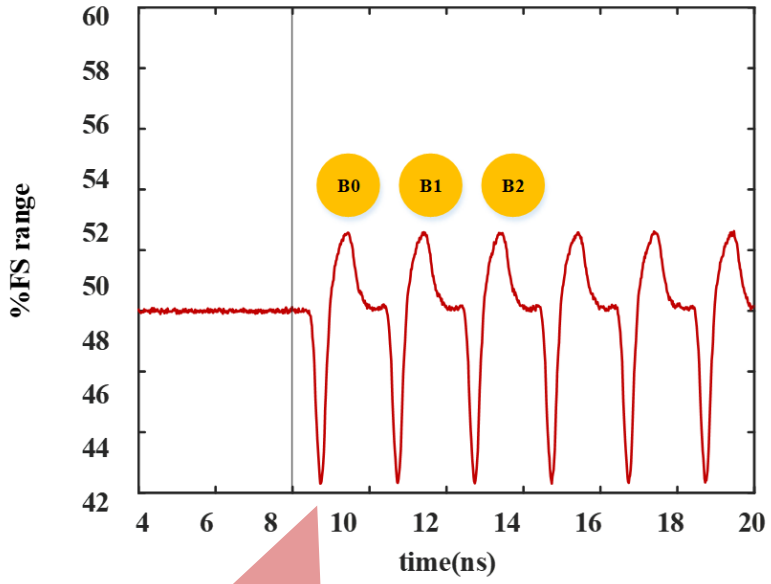


Bunch-phase (bunch arrival-time):

- **Proof of principle:**
  - Measurement of bunch-phase in real-time with RFSoC (C-code)
  - Statistics of the measurements (moving average and root mean square error)
- **Planned final solution:**
  - Accelerate the phase measurement in FPGA logic for bunch-by-bunch feedback
  - Close feedback loop: directly drive longitudinal kicker with 32 GSPS RFSoC DAC waveform (4 GSPS with 8x interleaving)
- **Backup solution:**
  - Use old SLS 1.0 analog down-converter & up-converter with RFSoC (Implemented)

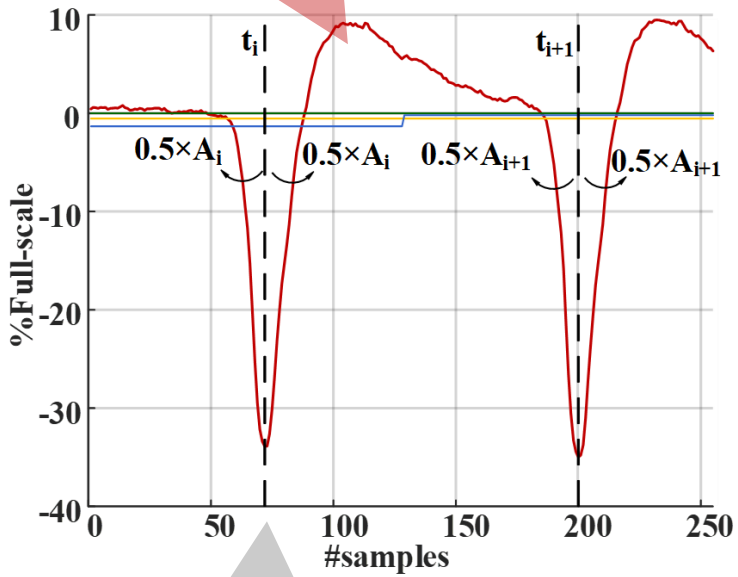
SLS2.0 MBFB: Bunch-charge & Bunch-phase

Timing event from EEVR used for bunch indexing



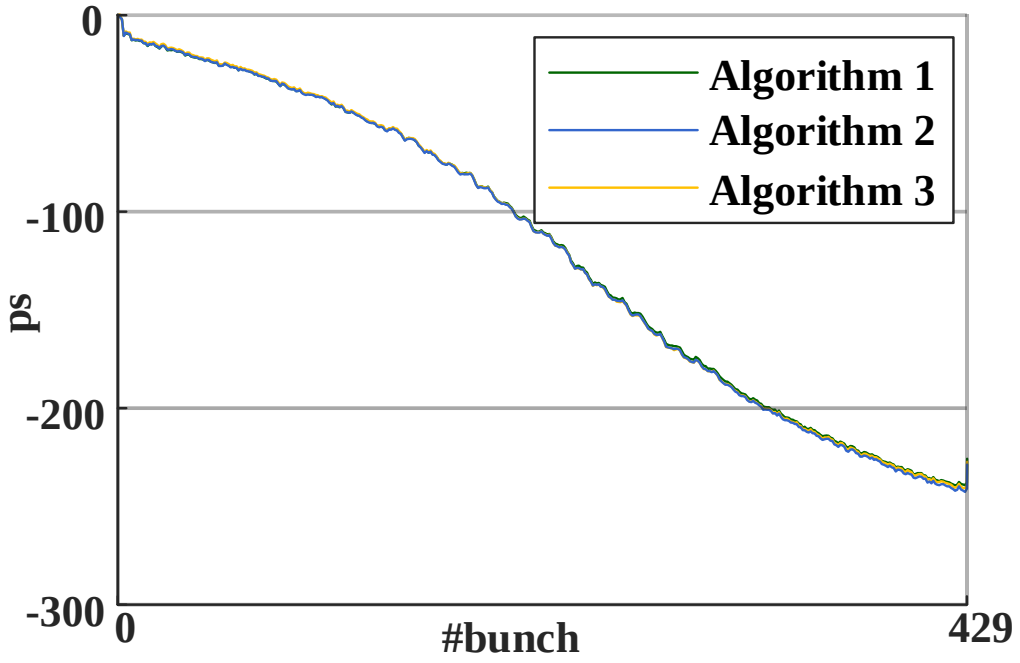
BPM sum signal (S) sampled by RFSoC ADCs and used for bunch charge & arrival time calculation

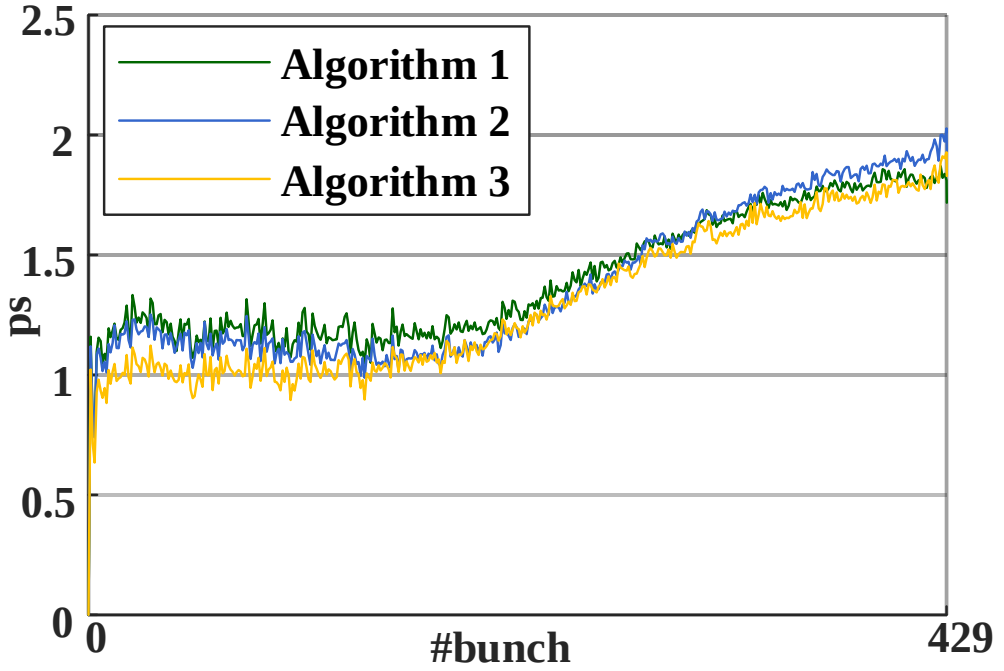
Area Ai below negative pulse and the dynamic baseline ∝ bunch-charge



The time t_i which splits A_i in half is an estimate for bunch arrival-time.

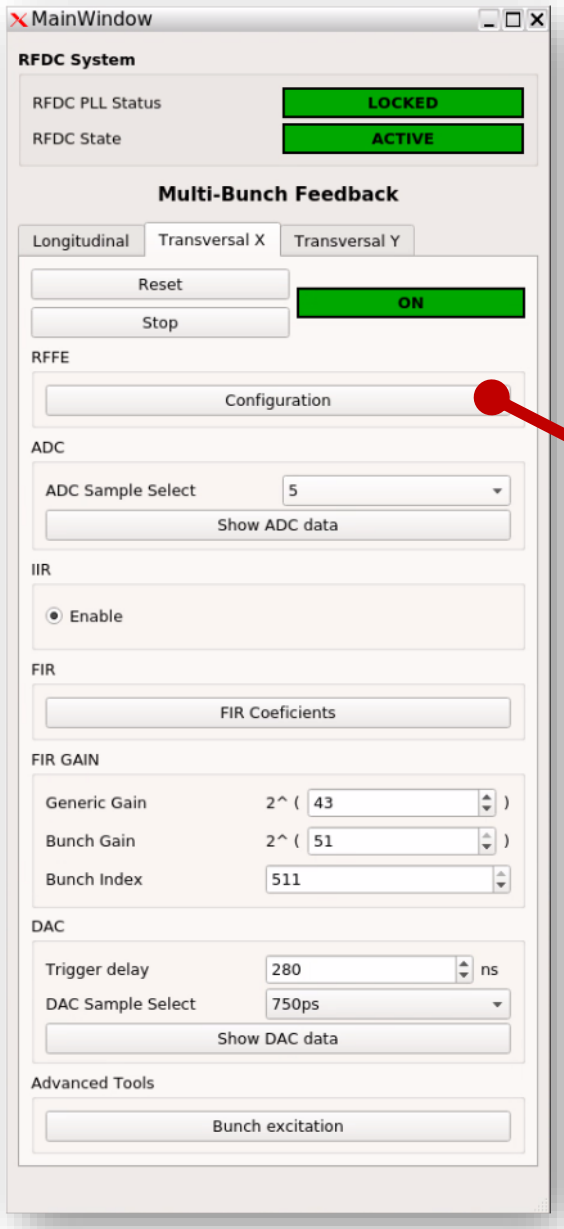
SLS2.0 MBFB: Bunch-charge & Bunch-phase

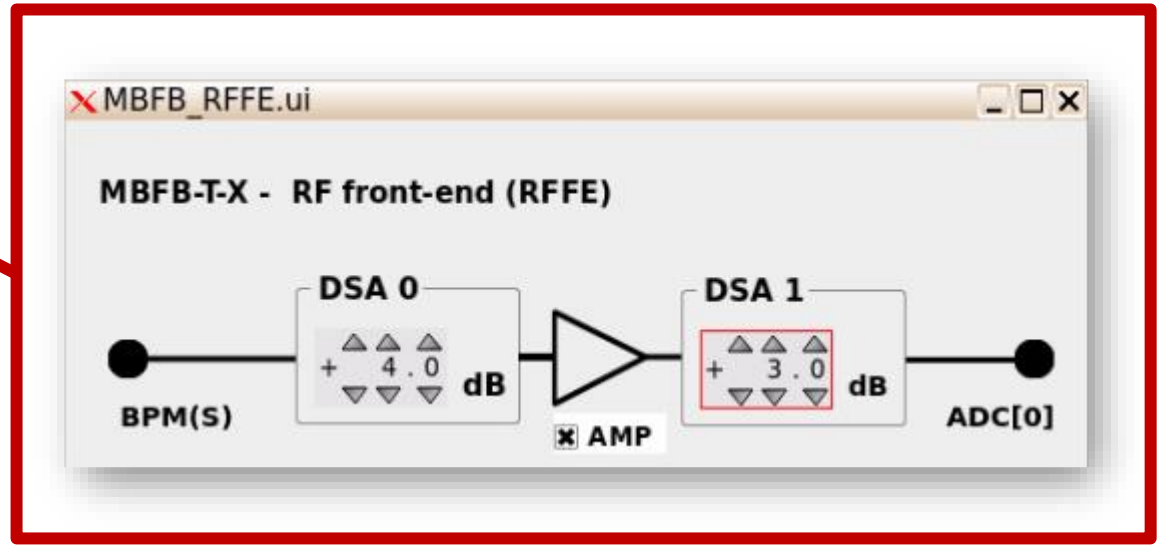




Bunch arrival-time measurement and RMS error of the measurements with different algorithms.

SLS2.0 MBFB: Python GUI





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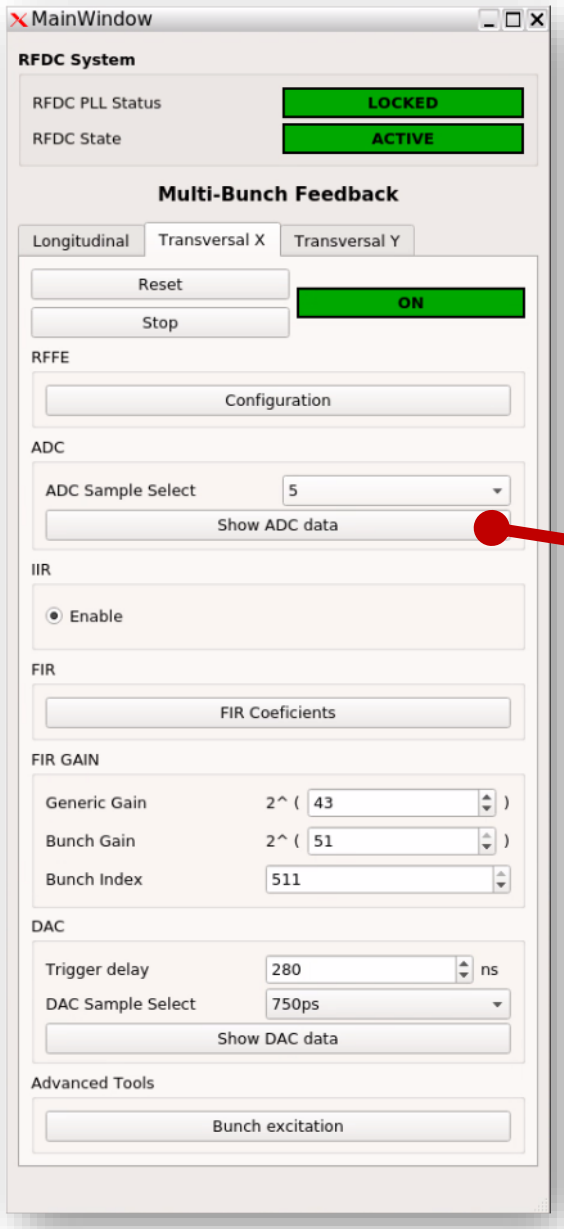

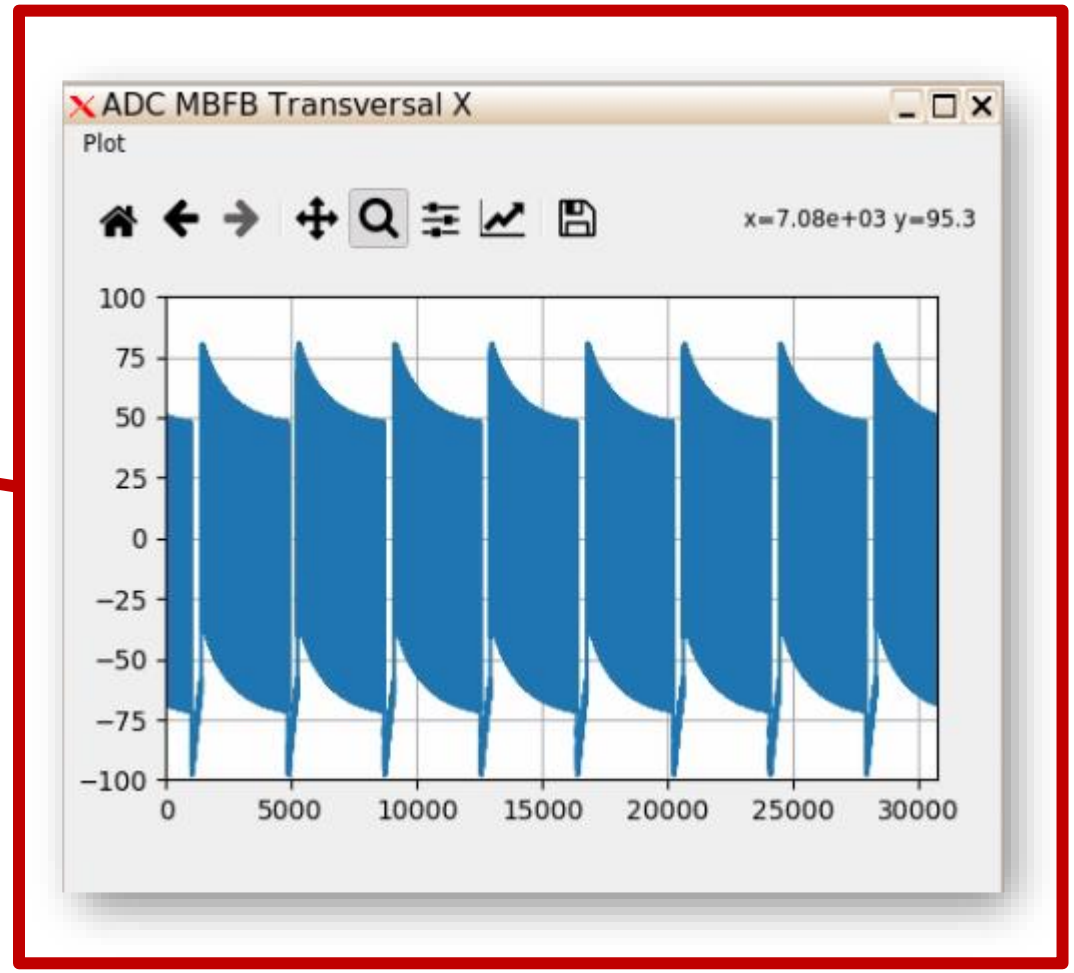

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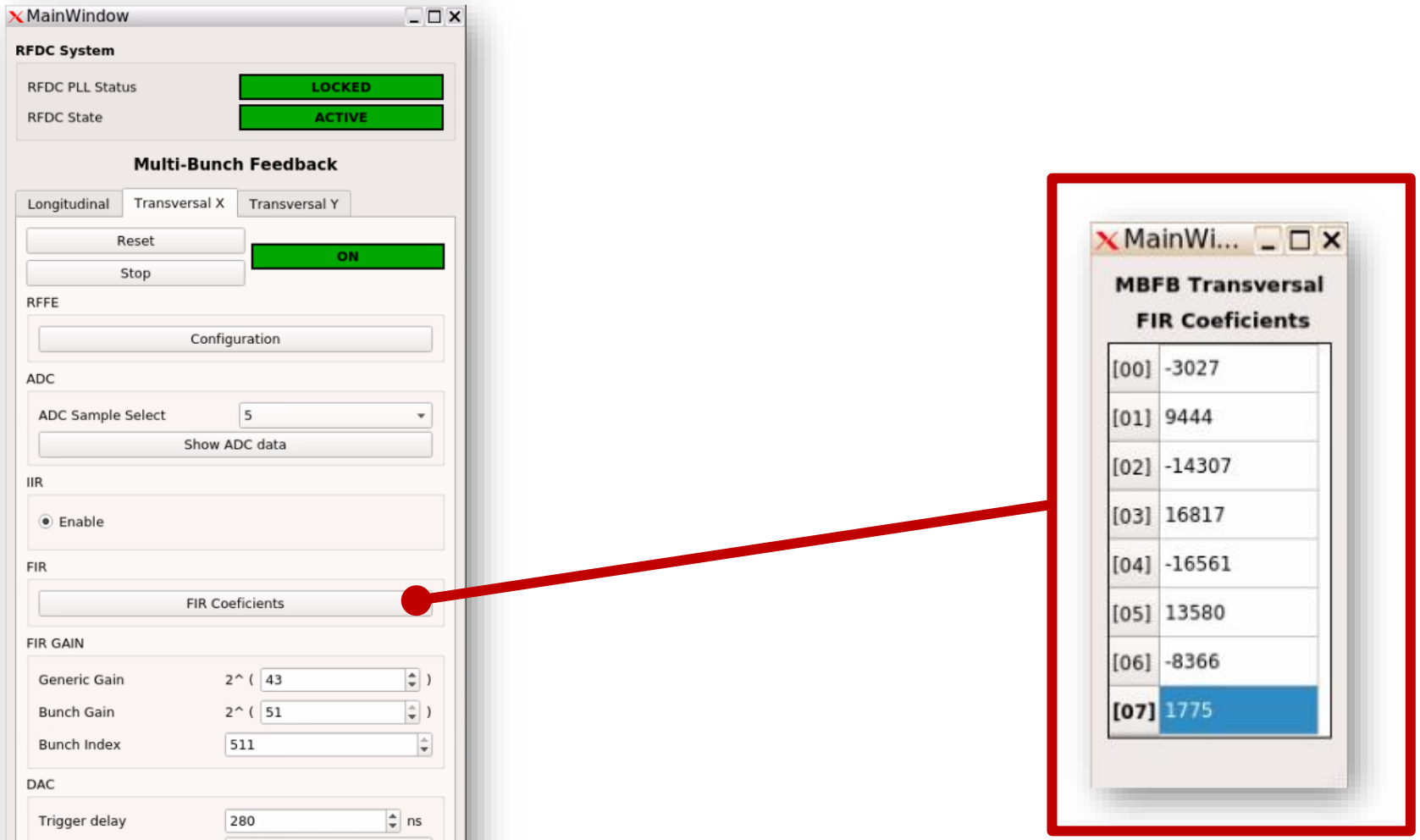
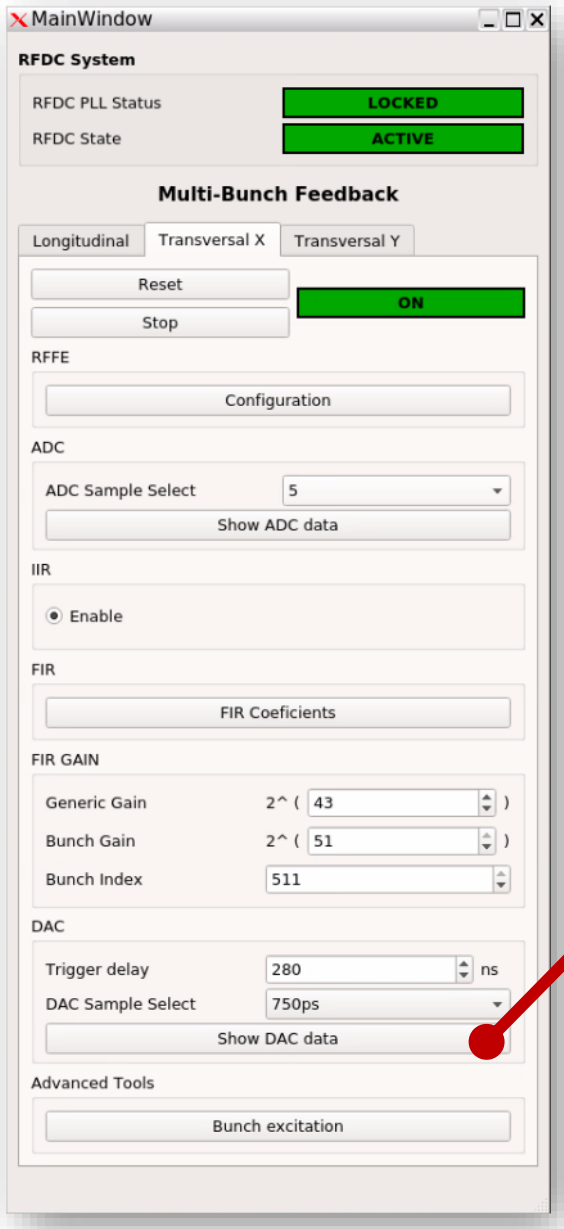
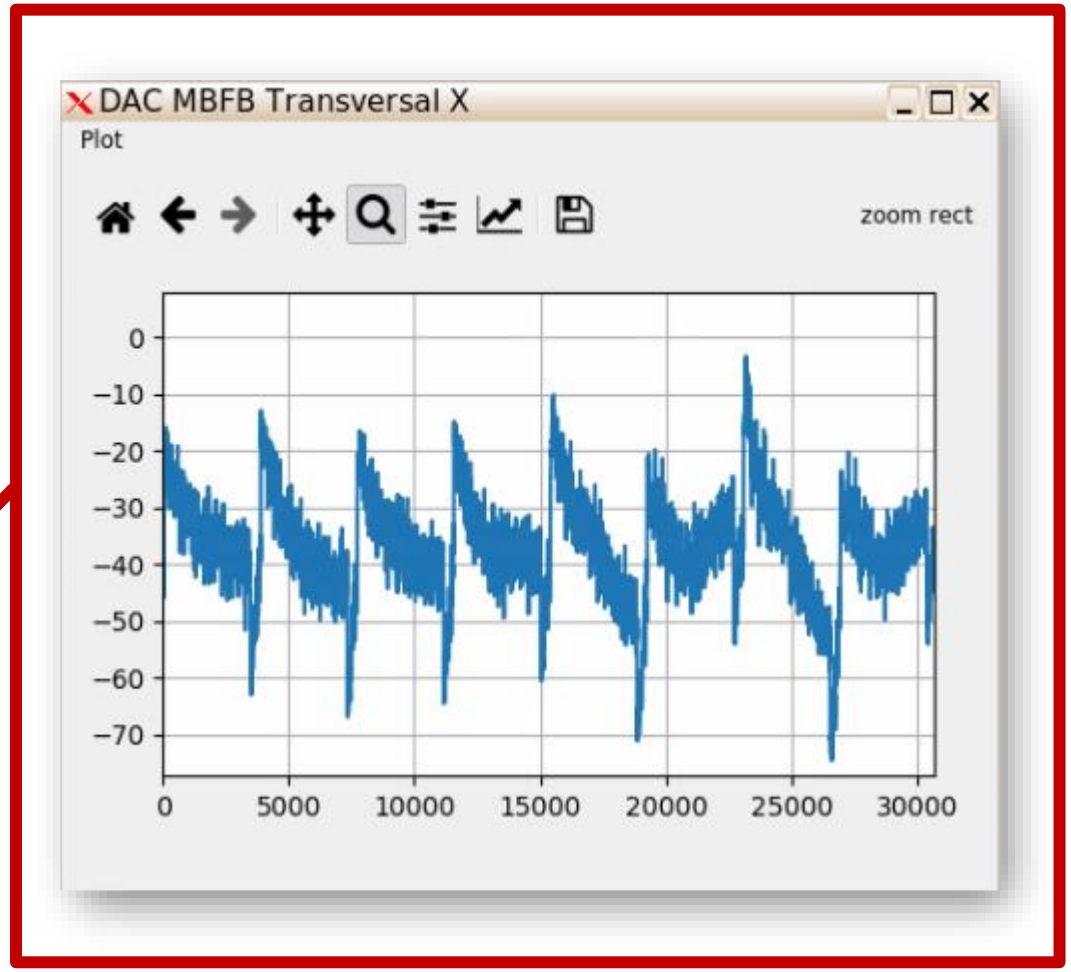
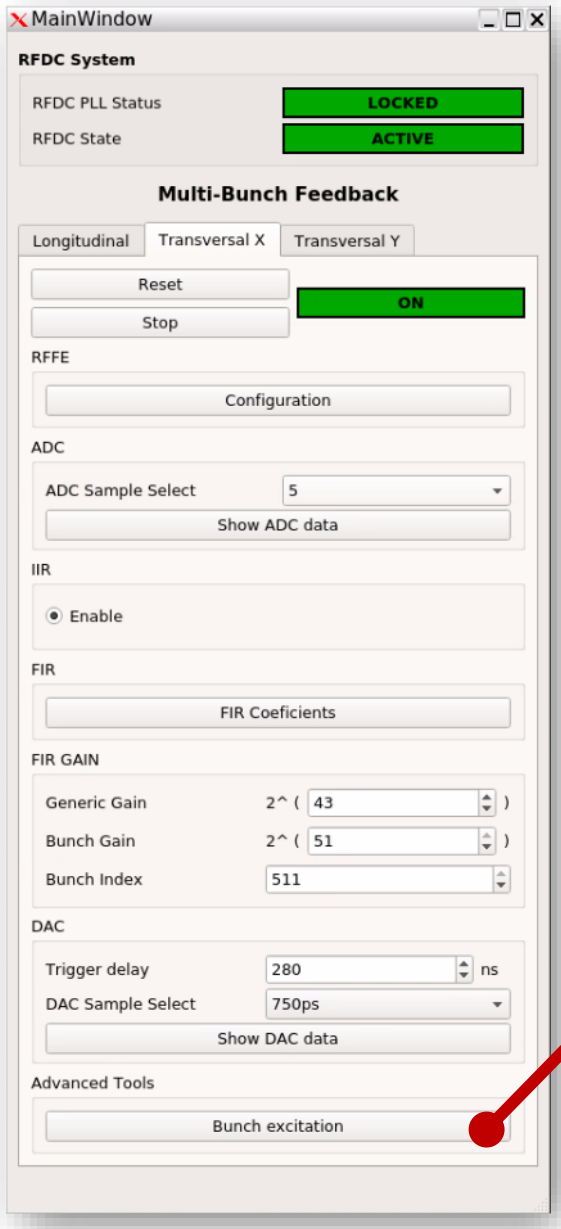


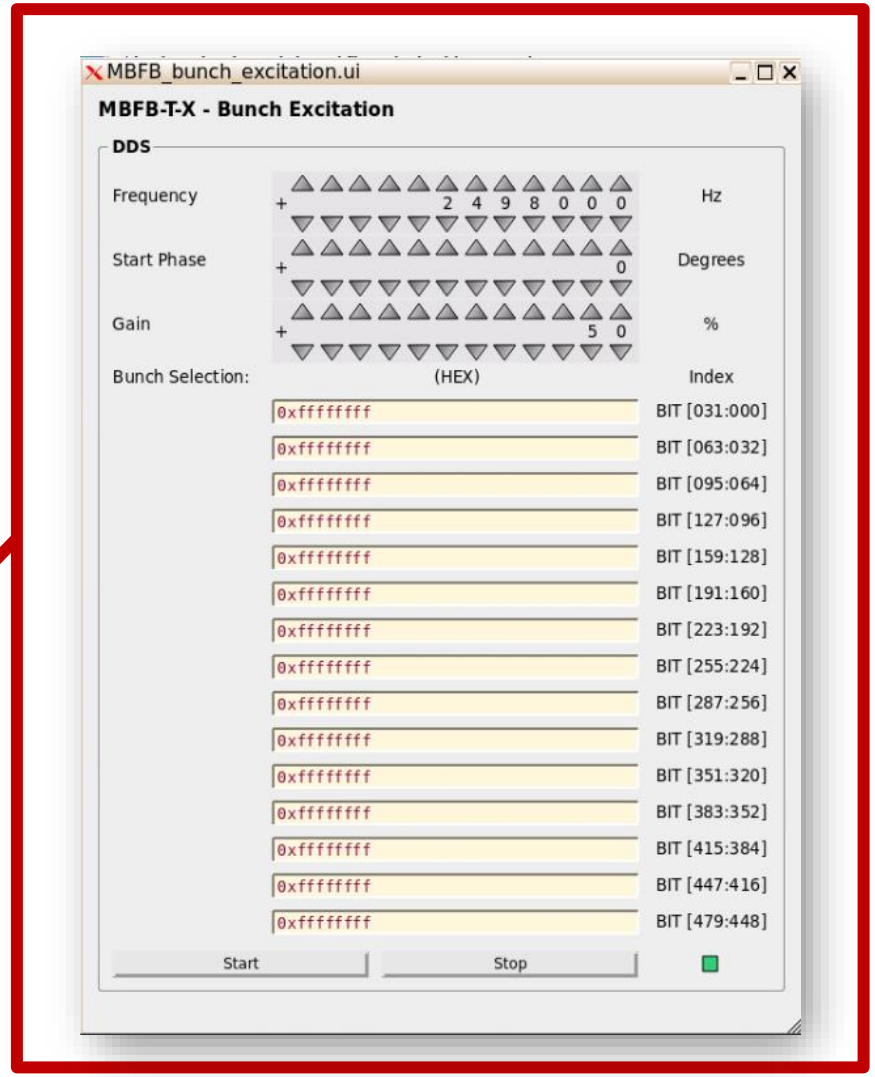
SLS2.0 MBFB: Python GUI





SLS2.0 MBFB: Python GUI





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Status & Outlook

Status:

Transverse MBFB:

- Transverse RFSoC-based bunch-by-bunch feedback demonstrated at SLS1.0
  - Using I-tech RFFE (down-sampling the BPM signals)
  - ADC acquisition at 4GS/s, but only 1 out of 8 samples processed (throughput 500MS/s)

Longitudinal MBFB:

- Longitudinal phase and bunch charge measurement with direct sampling in real-time (C code).

General:

- Tune excitation, coupled bunch mode (CBM) diagnostics

Outlook:

Transverse MBFB:

- Utilize all ADC samples to determine beam position (at 4GS/s)
  - Including digital compensation of phase slippage from 1st to last bunch

Longitudinal MBFB:

- Accelerate direct sampling bunch-phase calculation in HW, replacing SW (C code) with VHDL.
- Replace analog with digital up-converter to drive longitudinal kicker amplifiers.

General:

- Automate the tunning of the feedback.
- Improve diagnostic tools (Tune measurement, excitation/damping measurement, …).

Thank you!

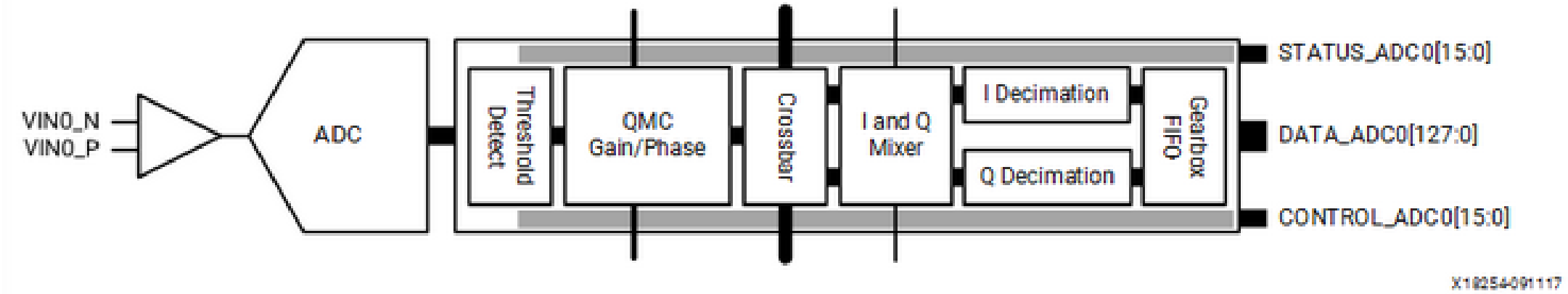
References

- [1] M. Dehler, G. Marinkovic, P. Pollet, and T. Schilcher, “State of the SLS Multi-bunch Feedback”, in Proc. APAC'07, Indore, India, Jan.-Feb. 2007, paper TUPMA014, pp. 118-120.
- [2] A. Streun, “SLS 2.0, the Upgrade of the Swiss Light Source”, in Proc. IPAC'22, Bangkok, Thailand, Jun. 2022, pp. 925-928. doi:10.18429/JACoW-IPAC2022-TUPOST032
- [3] Xilinx, https://www.xilinx.com/products/boards-and-kits/zcu111.html
- [4] P. H. Baeta Neves Diniz Santos, B. Keil, and G. Marinkovic, “RF System-on-Chip for Multi-Bunch and Filling-Pattern Feedbacks”, in Proc. IBIC'22, Kraków, Poland, Sep. 2022, pp. 379-382. doi:10.18429/JACoW-IBIC2022-WE2C4
- [5] P. H. Baeta Neves Diniz Santos, B. Keil, and G. Marinkovic, “Status of the RFSoC-based Signal Processing for Multi-Bunch and Filling-Pattern Feedbacks in the SLS2.0”, in Proc. IBIC’23in Proc. IBIC'23, Saskatoon, Canada, Sep. 2023, pp. 297-300

Appendix 1: RFSoC ADC Analog Characteristics

Parameter	Comments/Conditions [1]	Min	Typ [2]	Max	Units
Analog Inputs					
Resolution		12	–	–	Bits
Sample Rate	Devices using quad ADC tile channel	0.5	–	2.058	GS/s
	Devices using dual ADC tile channel	1	–	4.096	GS/s
Full-scale Input	Input 100Ω on-die termination [3]	–	1	–	V_{PPD}
		–	1	–	dBm
Analog Input Bandwidth	Full-power bandwidth (–3 dB) [3]	–	4	–	GHz
Common mode voltage [4]	AC coupling mode with internal bias	–	1.25	–	V
Crosstalk isolation between channels [5]	F_{IN} = 240 MHz	–	–70	–	dBc
	F_{IN} = 1.9 GHz	–	–70	–	dBc
	F_{IN} = 2.4 GHz	–	–70	–	dBc
	F_{IN} = 3.5 GHz	–	–70	–	dBc

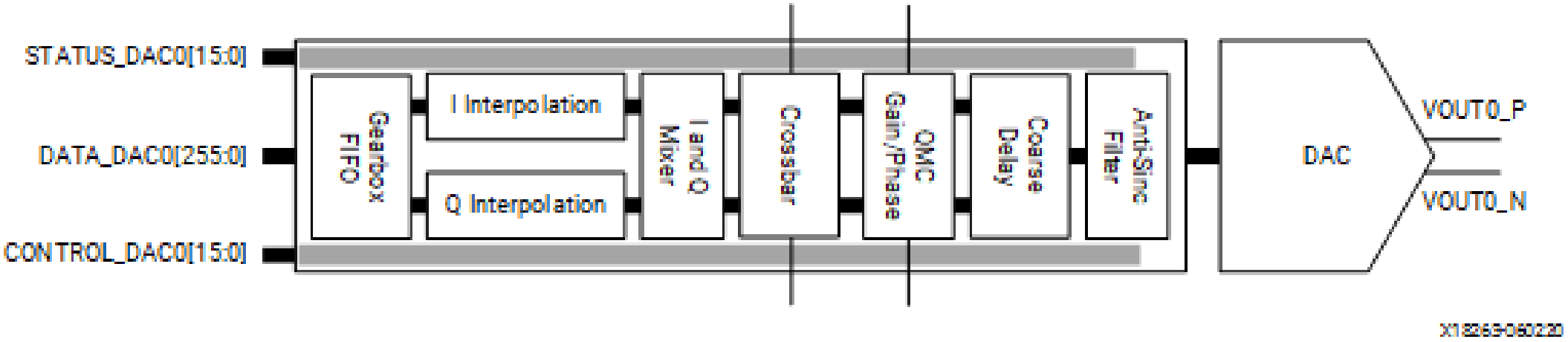
Appendix 2: RF data-converter ADC IP – Processing Path



Appendix 3: RFSoC DAC Analog Characteristics

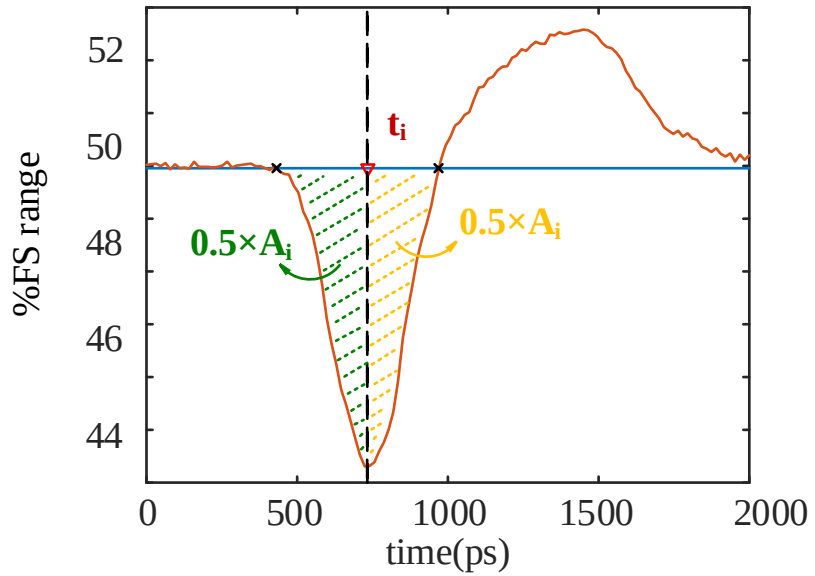
Parameter	Comments/Conditions [1]	Min	Typ [2]	Max	Units
Analog Outputs					
Resolution		14	–	–	Bits
Sample Rate		0.5	–	6.554	GS/s
Maximum Output Power	20 mA mode, V_{DAC_AVTT} = 2.5V, 100Ω termination	–	+1	–	dBm
	32 mA mode, V_{DAC_AVTT} = 3.0V, 100Ω termination	–	+5	–	dBm
Analog Bandwidth	Full power bandwidth (–3 dB)	–	4	–	GHz
On-die Termination	Single-ended on-die termination to external 2.5V/3V V_{DAC_AVTT} [3]	–	50	–	Ω
Crosstalk isolation between channels [4]	F_{OUT} = 240 MHz	–	–70	–	dBc
	F_{OUT} = 1.9 GHz	–	–70	–	dBc
	F_{OUT} = 2.4 GHz	–	–70	–	dBc
	F_{OUT} = 3.5 GHz	–	–70	–	dBc

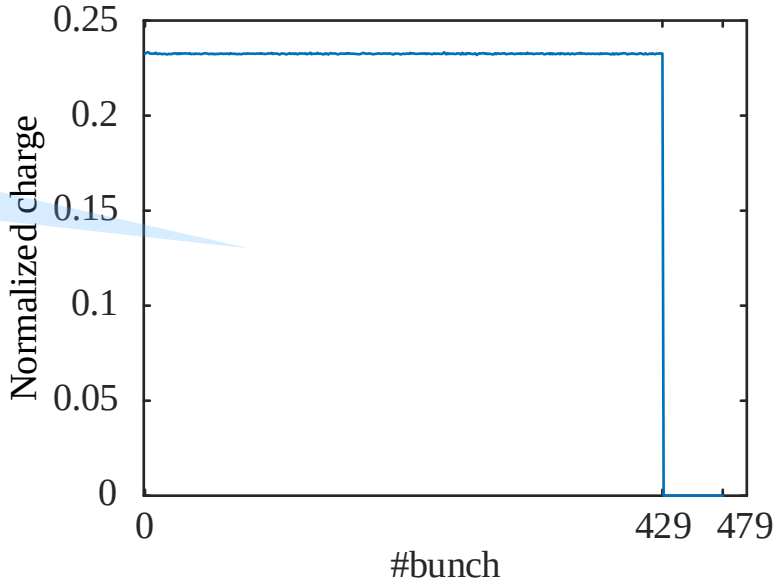
Appendix 4: RF data-converter IP - DAC Processing Path



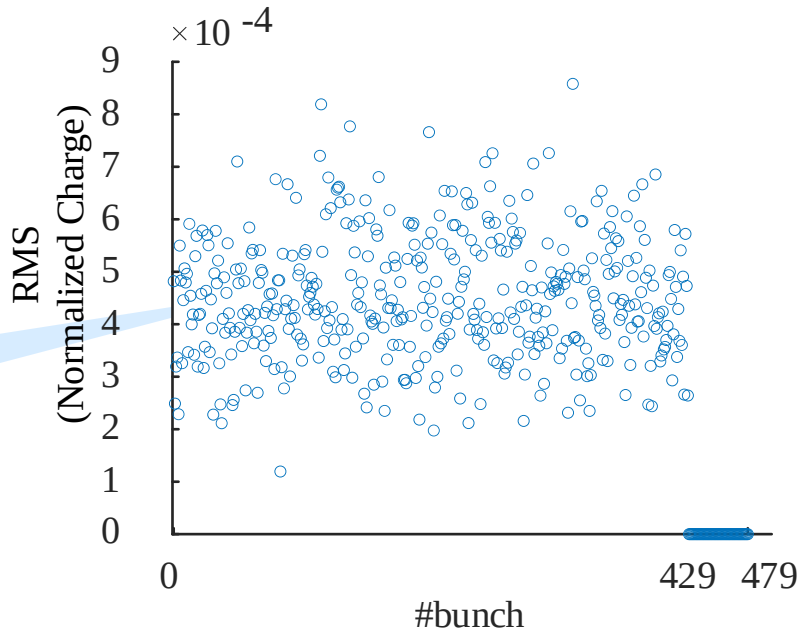
Appendix 5: Bunch charge noise measurement

Bunch charge measurement for an homogeneous filling pattern with bunch gap generated by DAC



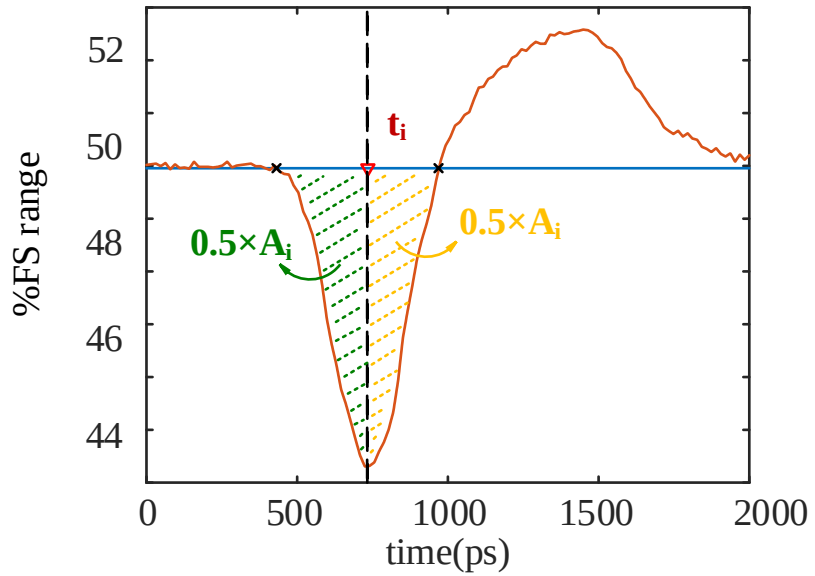


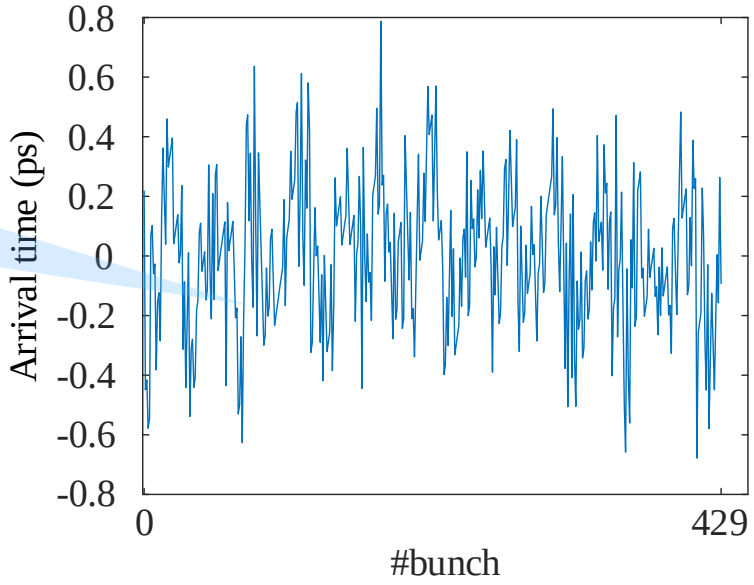
Noise of charge measurement measured with RFSoC, using DAC to simulate BPM signal.



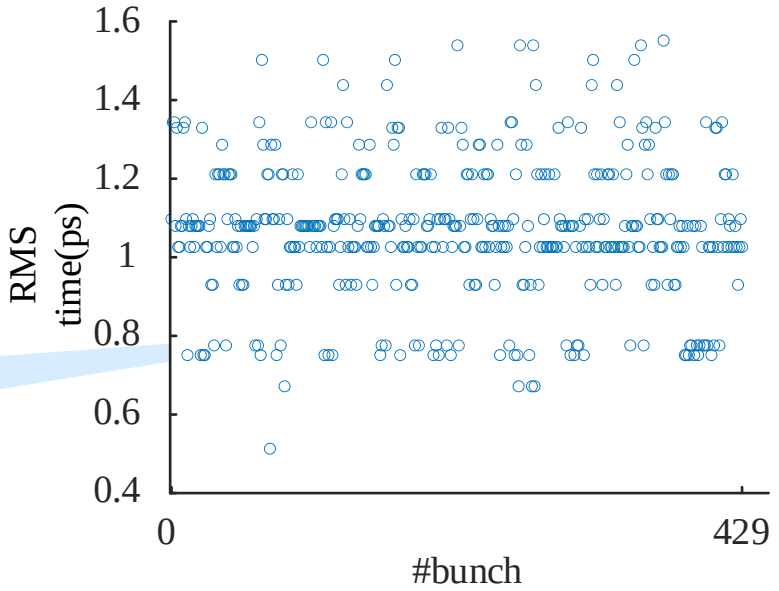
Appendix 6: Bunch arrival time noise measurement

Bunch arrival time measurement for a bunch train with bunch gap and equally spaced bunches (2ns) generated by DAC





Noise of bunch arrival time measured with RFSoC, using DAC to simulate BPM signal.



Appendix 7: Python GUI