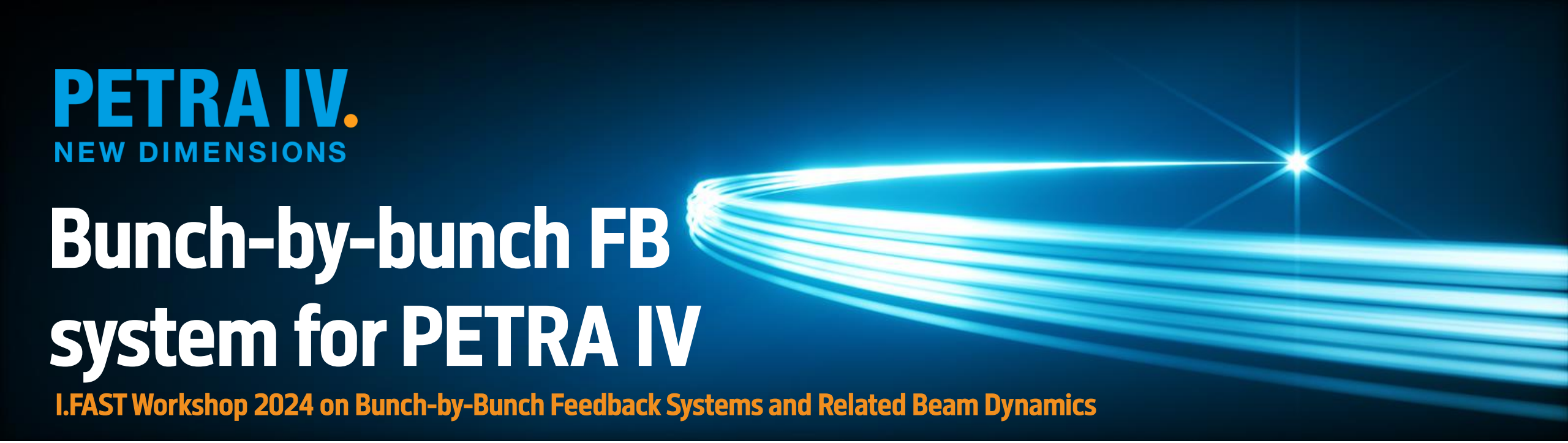


Bunch-by-bunch FB system for PETRA IV

I.FAST Workshop 2024 on Bunch-by-Bunch Feedback Systems and Related Beam Dynamics

Sven Pfeiffer for the WP2.08 / DESY-MSK team
Karlsruhe, 3-6 March 2024

HELMHOLTZ

DESY.

Outline

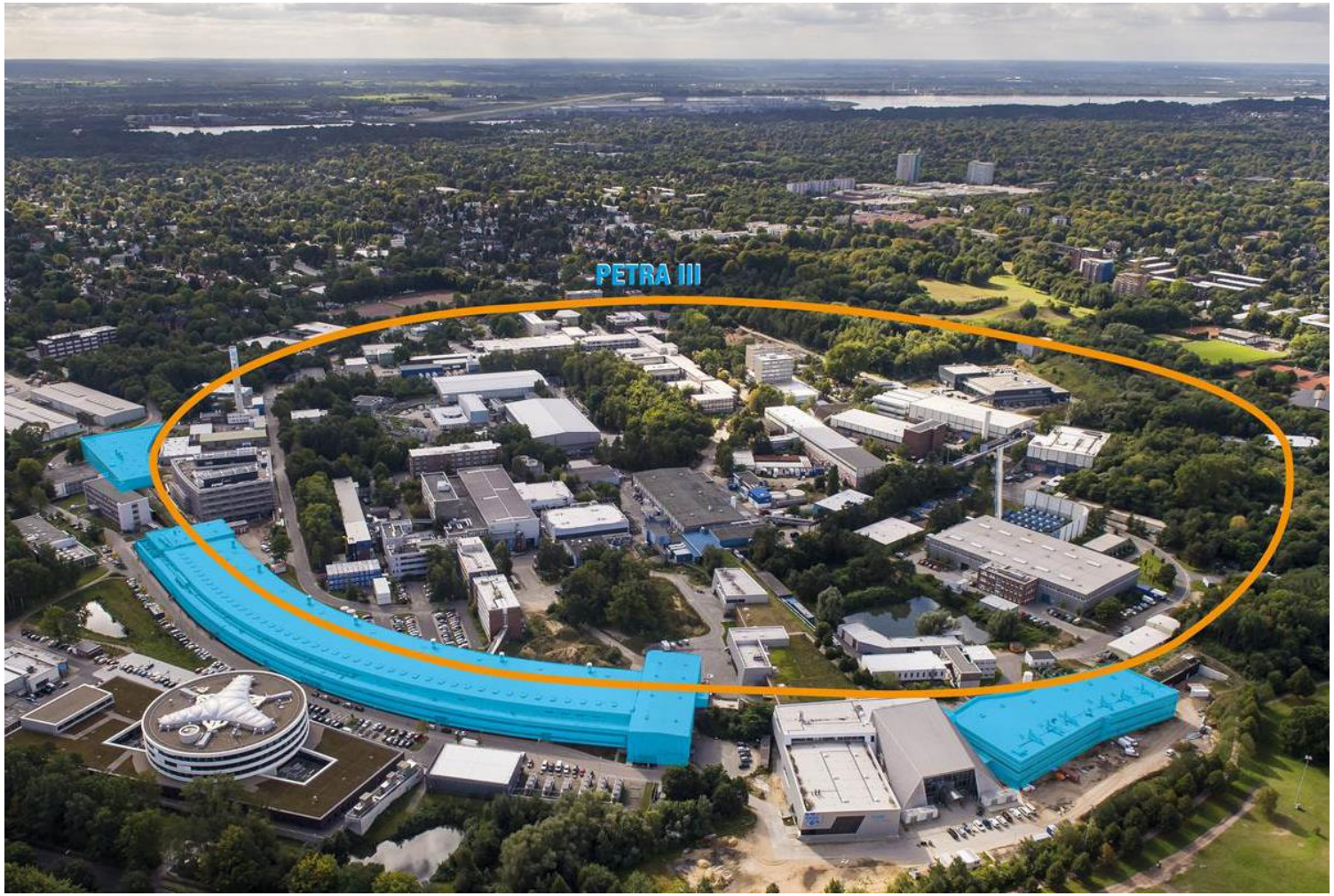
1. Introduction
2. MBFB design status
3. First measurements at PIII
4. PIV MBFB diagnostics / active control
5. Summary

Introduction

PETRA III

2.3km, 6GeV, since 2009 3rd gen. light source

- Brightness 480b@120mA
- Timing 40b@100mA
- Emittance 1300pm rad
- Electronics VME/SEDAC etc
- Control system Tine

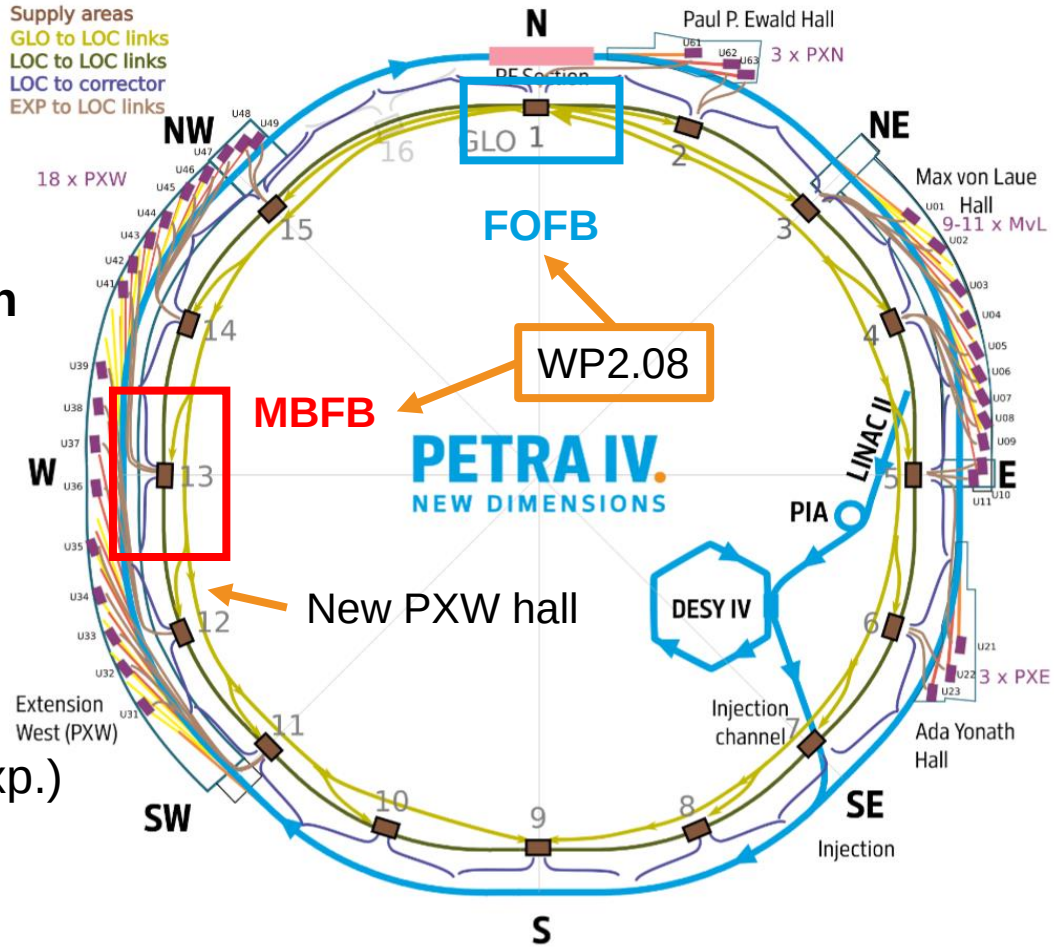


Introduction

PETRA III → PETRA IV upgrade status

2.3km, 6GeV, since 2009 3rd gen. light source → 4th generation

- Brightness* 480b@120mA → 1920b@120mA
- Timing* 40b@100mA → 80b@80mA
- Emittance 1300pm rad → 20pm rad
- Electronics VME/SEDAC etc → MicroTCA.4
- Control system Tine → DOOCS (TANGO at exp.)



* PETRA IV non-baseline values:
- 3840b@200mA
- 80b@200mA

Introduction

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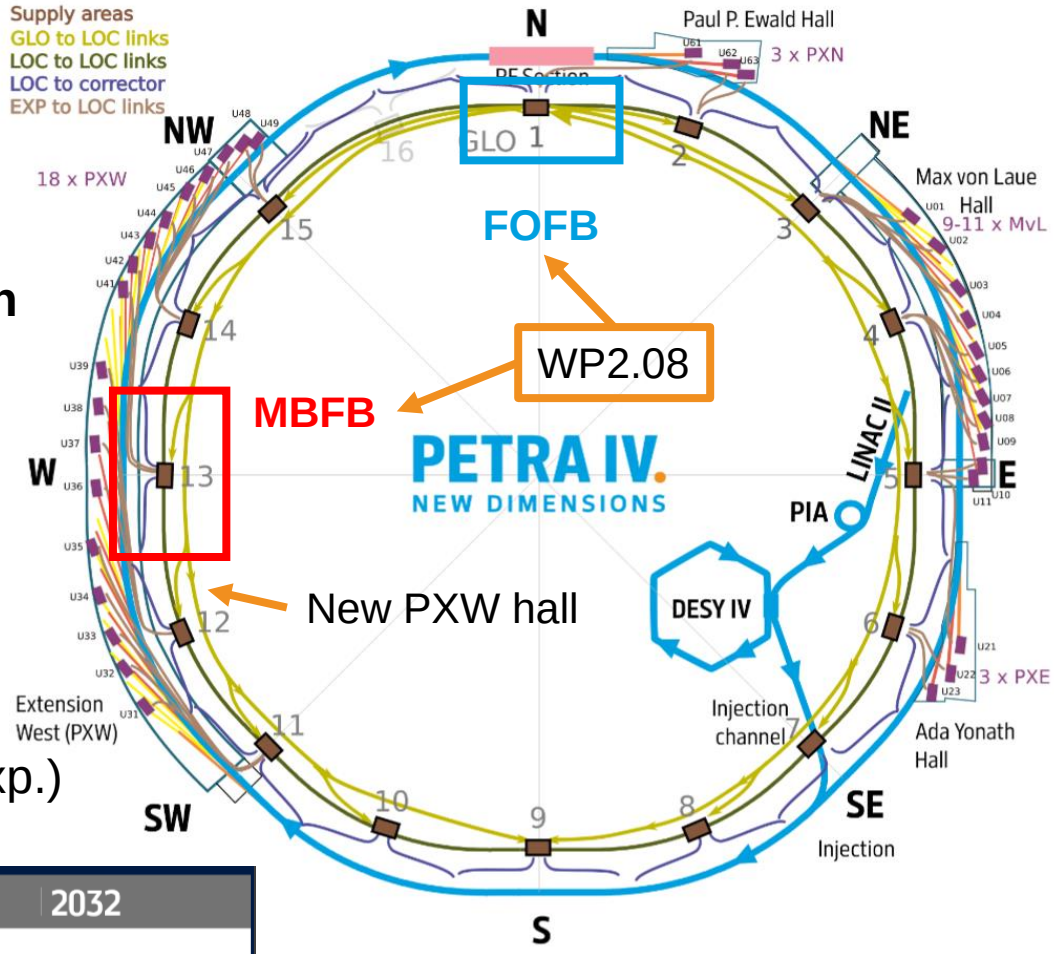
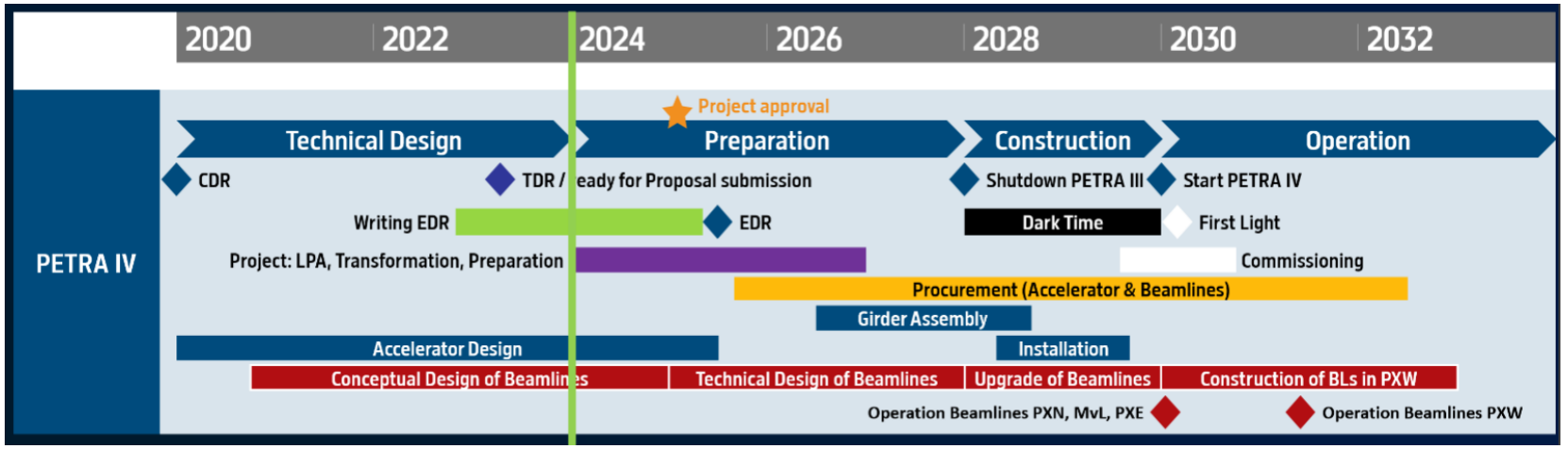




* PETRA IV non-baseline values:
- 3840b@200mA
- 80b@200mA

Introduction

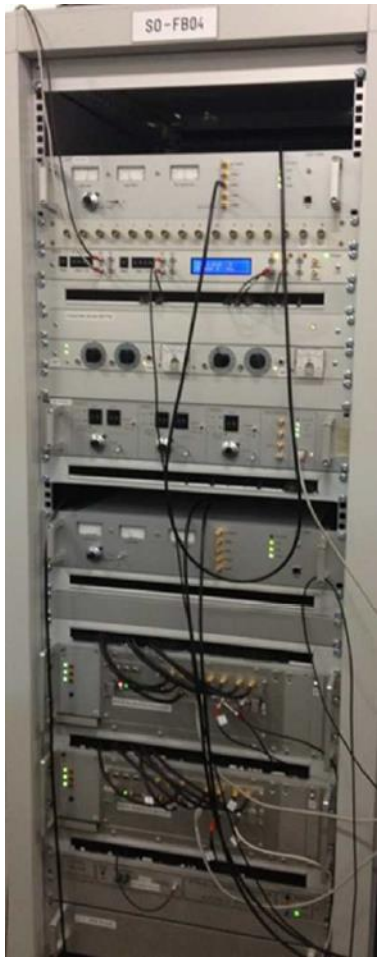
Controls based on MicroTCA

Courtesy: Tim Wilksen

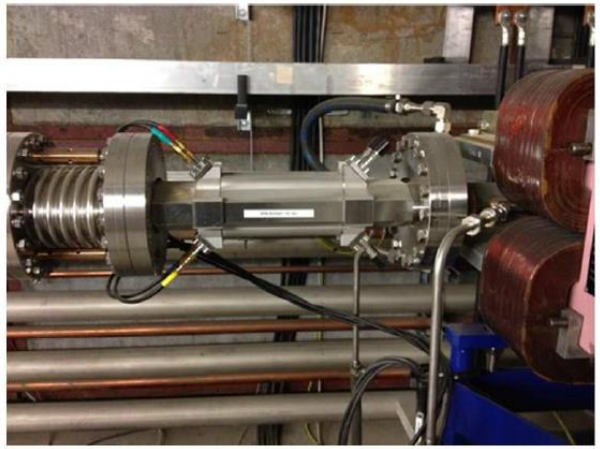
Introduction

Status PETRA III - Transversal and longitudinal MBFB

T-MBFB Rack



Stripline BPM

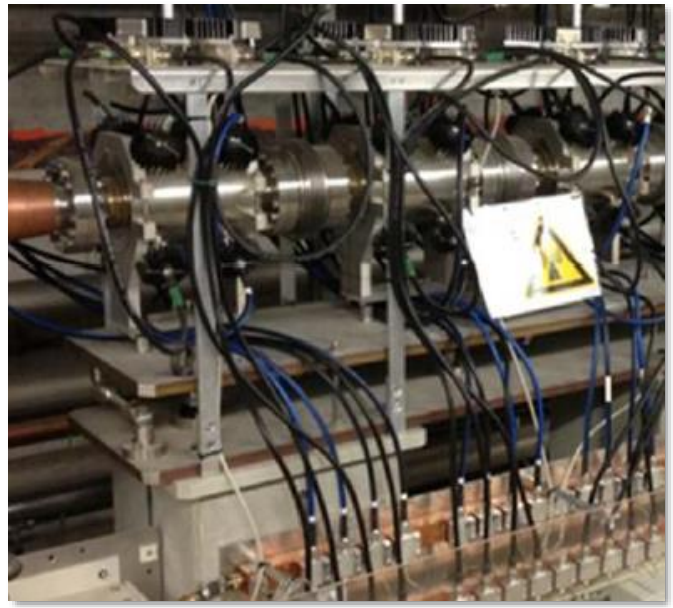


HPAs

Stripline kickers

L-MBFB Rack, HPAs and phase shifters

FB cavities



Introduction

Status PETRA III → Upgrade PETRA IV

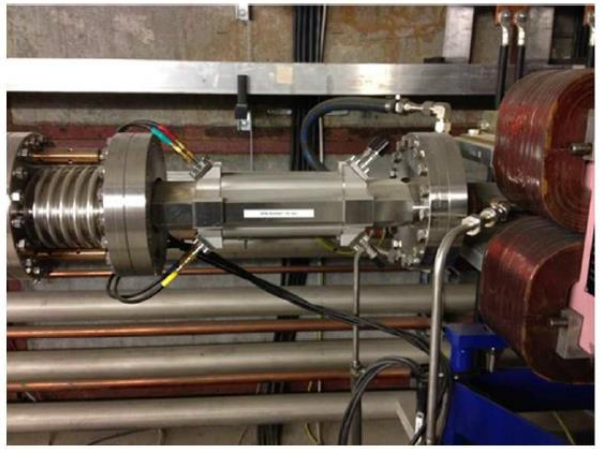
PIV upgrade (diag & FB system)

T-MBFB Rack NEW

HPAs NEW

Stripline kickers NEW

Stripline BPM NEW

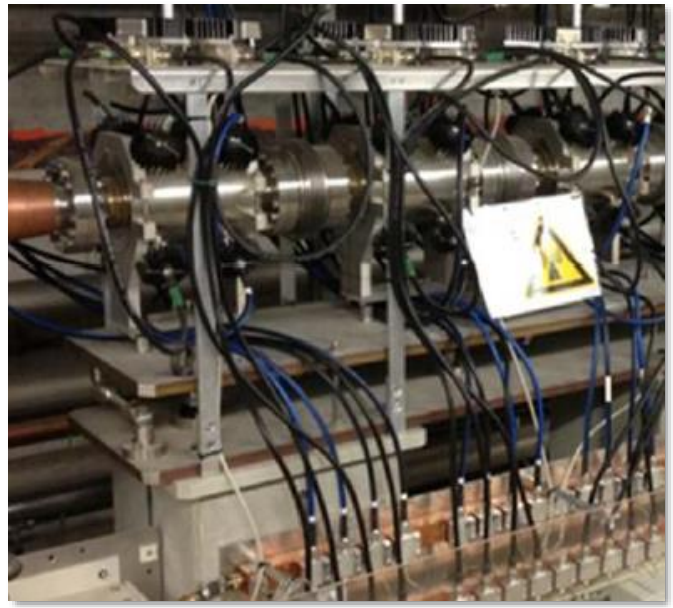


PIV upgrade (diag only)

NEW

L-MBFB Rack, HPAs and phase shifters

FB cavities



Introduction

MBFB upgrade plan for PETRA IV

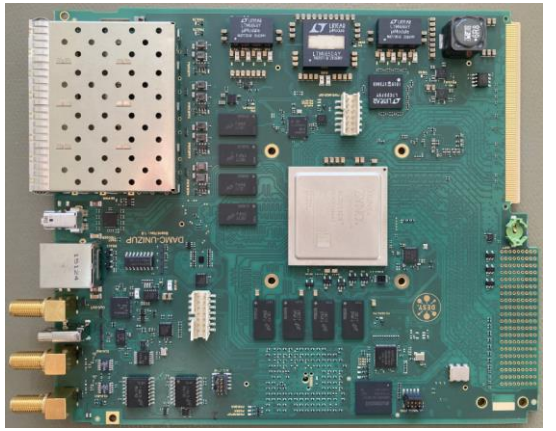
Recommended 2 step
(foreground/background)
ADC calibration mechanism?

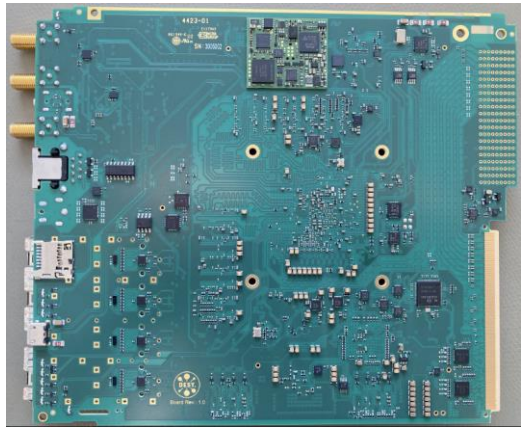
Decided for an in-house development as the MBFB system is a key diagnostics system → Building up of scientific know how

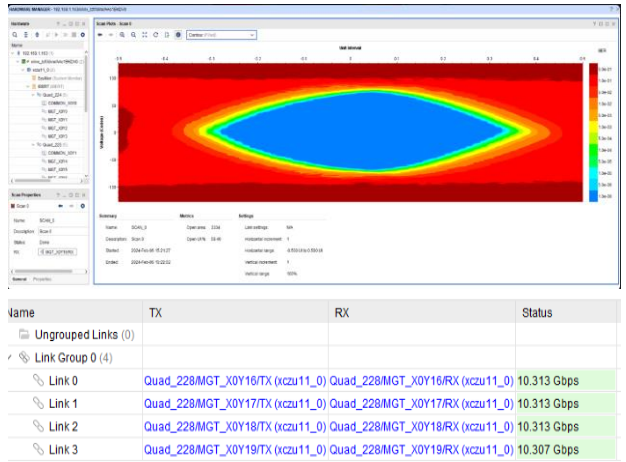
- Processing unit with RFSoC → new board (DAMC-DS5014DR) under design with other int/ext stakeholders (BAC, kicker pulser system, photon diag. (GMD, ToF), SCK-CEN (LLRF), …)
  - Project owner Behzad Boghrati (new at DESY 01/2024)
  - Currently collecting specifications
- New hardware boards licensed to industry (DAMC-FMC2ZUP, **DAMC-UNIZUP**, …, DAMC-DS5014DR)
  - DAMC-UNIZUP (I-Tech BPM) under tests
    - Cost-effective alternative to the DAMC-FMC2ZUP
    - Test results are very good!

Support and developments of systems

- Re-usability of boards, FW, SW
  - Generic FW and SW developments
  - Partly open source (BSP / application core)
- Collaborations using ChimeraTK and FWK
  - DOOCS - OPCUA - Tango - EPICS







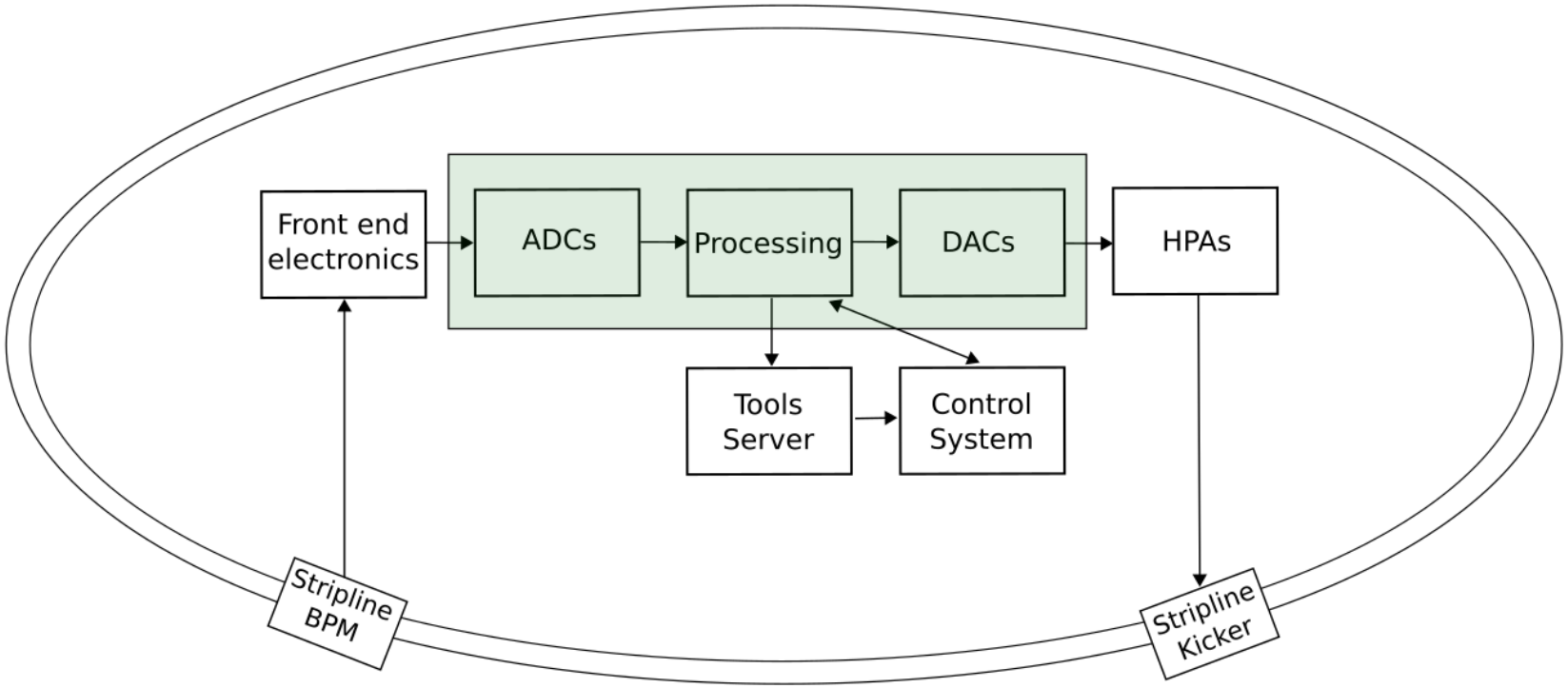
Name	TX	RX	Status
Ungrouped Links (0)			
Link Group 0 (4)			
Link 0	Quad_228/MGT_X0Y16/TX (xczu11_0)	Quad_228/MGT_X0Y16/RX (xczu11_0)	10.313 Gbps
Link 1	Quad_228/MGT_X0Y17/TX (xczu11_0)	Quad_228/MGT_X0Y17/RX (xczu11_0)	10.313 Gbps
Link 2	Quad_228/MGT_X0Y18/TX (xczu11_0)	Quad_228/MGT_X0Y18/RX (xczu11_0)	10.313 Gbps
Link 3	Quad_228/MGT_X0Y19/TX (xczu11_0)	Quad_228/MGT_X0Y19/RX (xczu11_0)	10.307 Gbps

Courtesy: M.Fenner, S.Chystiakov

MBFB design status

Layout of the T-MBFB system

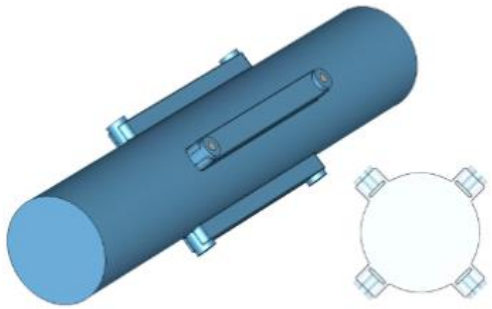
- Stripline BPM
- Front end electronics
- Signal processing
  - ADCs
  - Digital processing
  - DACs
- HPAs and stripline kickers



MBFB design status

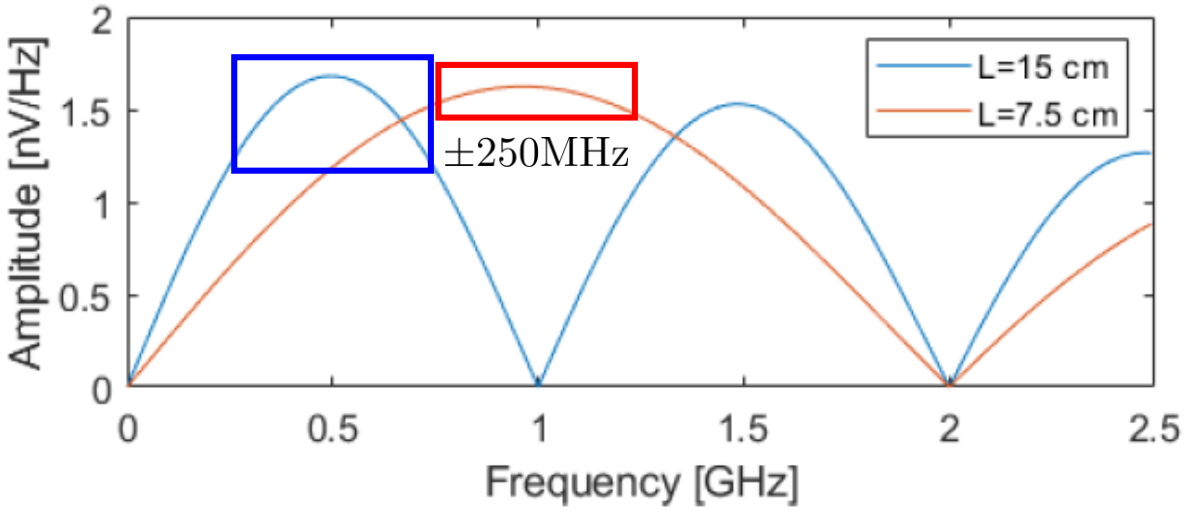
Layout of the T-MBFB system

- **Stripline BPM – design by WP2.05**
- Front end electronics
- Signal processing
  - ADCs
  - Digital processing
  - DACs
- HPAs and stripline kickers



CST model for EM simulations [S. Strokov]

- **Top level requirements***
  - Each bunch requires control, 2ns minimum bunch spacing
  - Each oscillation mode is associated with a frequency from zero to half bunch spacing frequency→ bandwidth: [0 … 250MHz]
  - All modes need negative feedback
    - Phase response need to be flat to few 10 degree
    - Amplitude response should be flat to within 3dB



* Libera WS2015 by G.Rehm

MBFB design status

Layout of the T-MBFB system

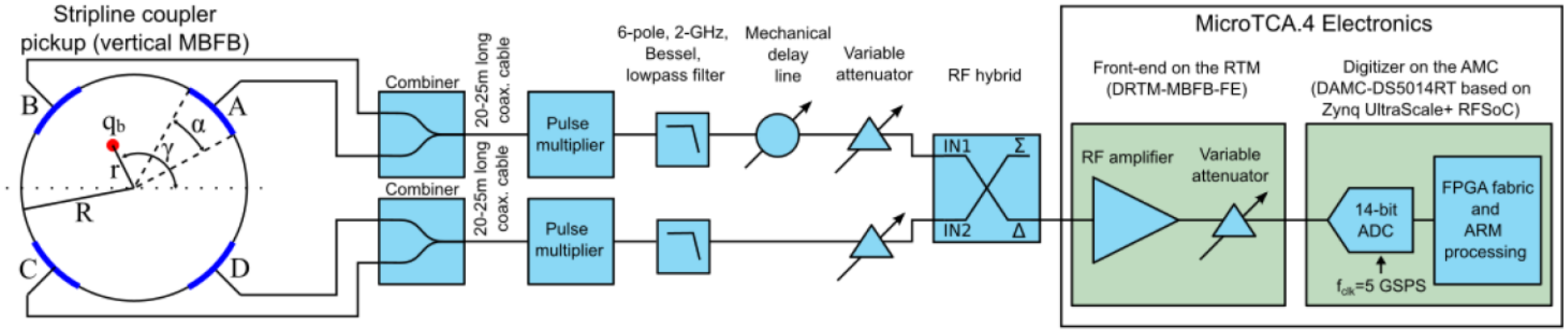
- Stripline BPM
- **Front end electronics**
- Signal processing
  - ADCs
  - Digital processing
  - DACs
- HPAs and stripline kickers

Analog signal preprocessing and signal conditioning

- Combiner and filtering stage
- Gain control for signal conditioning
  - Bunch currents 0.05mA .. 2.5mA (0.4nC … 7.7nC)
- Beam offset compensation

SNR of analog electronics

- Calculated SNR, based on an analog electronics model, is about 70 dB



MBFB design status

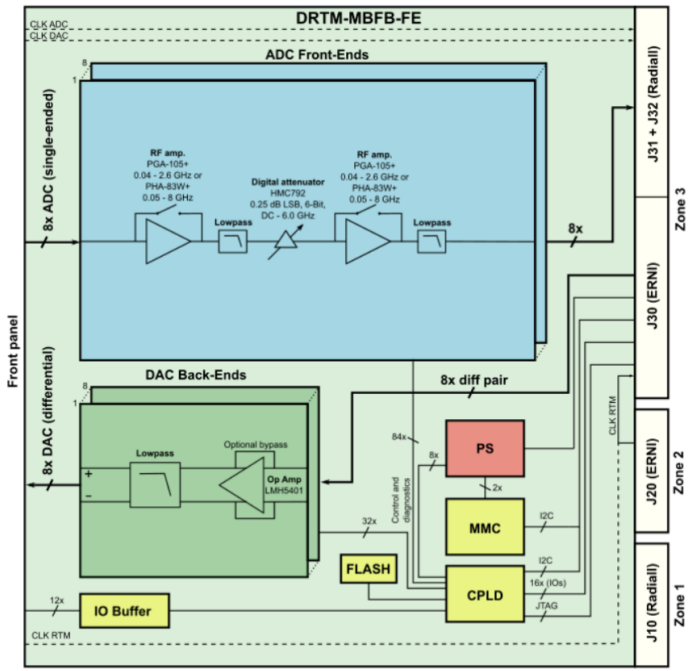
Layout of the T-MBFB system

- Stripline BPM
- Front end electronics
- **Signal processing**
  - ADCs (RTM)
  - Digital processing (AMC)
  - DACs (RTM)
- HPAs and stripline kickers

DRTM-MBFB-FE currently in production

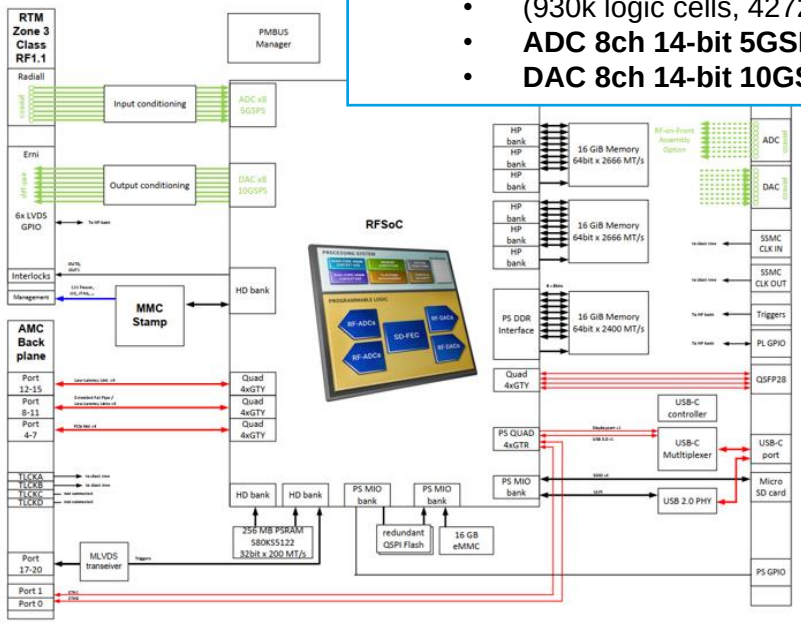
Requirements

- 3 (better 4) ADCs per plane (Δ_R, Δ_F, Σ, (Monitoring))
- Fast data processing for feedback and diagnostics
  - T-MBFB, cleaning of parasitic bunches, emittance control*
  - Bunch resolved position, phase, beam stability, tune
- 8 DACs per plane
  - Fine delay adjustments, dynamic compensations, …



DAMC-DS5014DR

Double-width mid-size AMC board
- ZU47DR **Zynq Ultrascale+ RFSoC** 3rd generation
  - (930k logic cells, 4272 DSP),
  - **ADC 8ch 14-bit 5GSPS, 6GHz analog BW,**
  - **DAC 8ch 14-bit 10GSPS**



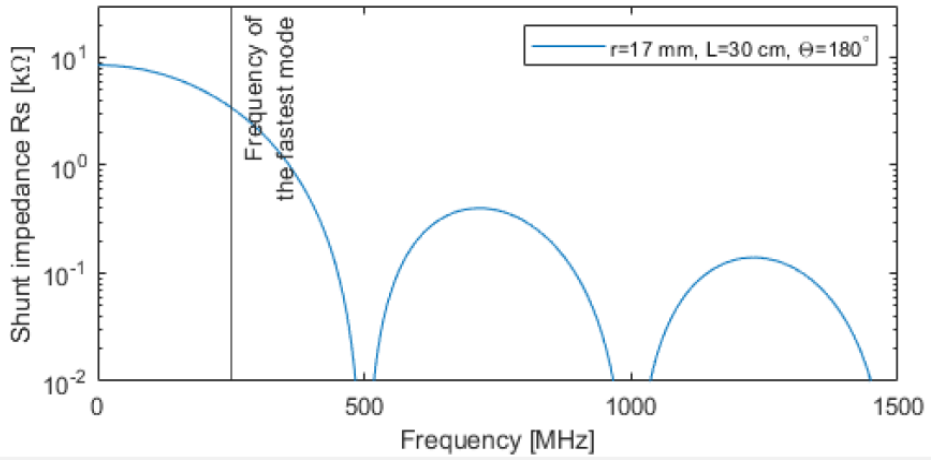
MBFB design status

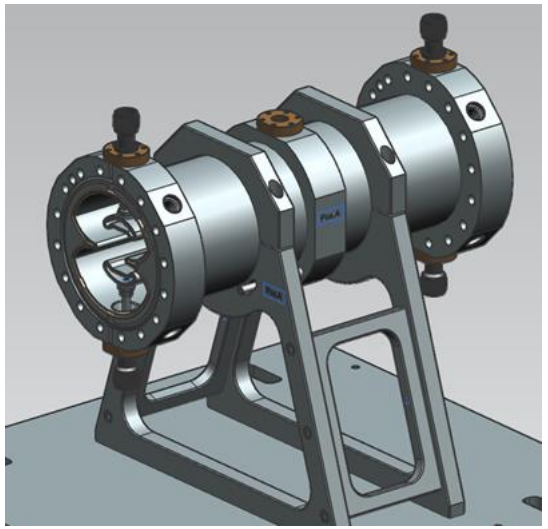
Layout of the T-MBFB system

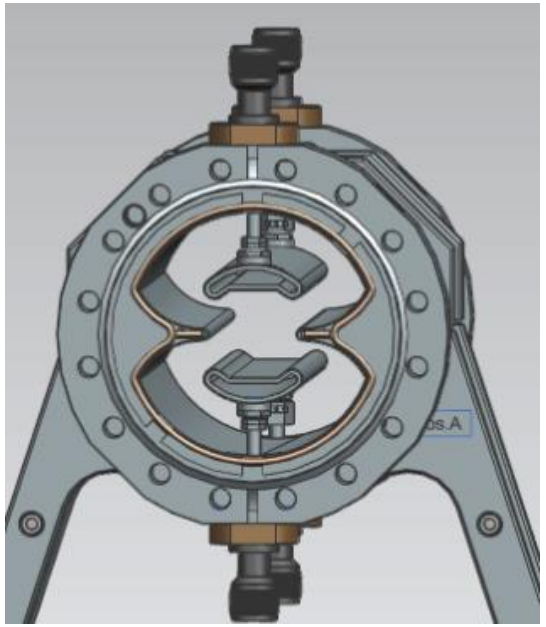
- Stripline BPM
- Front end electronics
- Signal processing
  - ADCs
  - Digital processing
  - DACs
- **HPAs and stripline kickers**

Requirements

- 8 HPAs per plane (2 per stripline kicker)
  - At least 250 MHz bandwidth
- 4 stripline kicker per plane
  - Designed by WP2.14
  - Reliably on every single bunch
  - Decay time of the EM field < 2ns



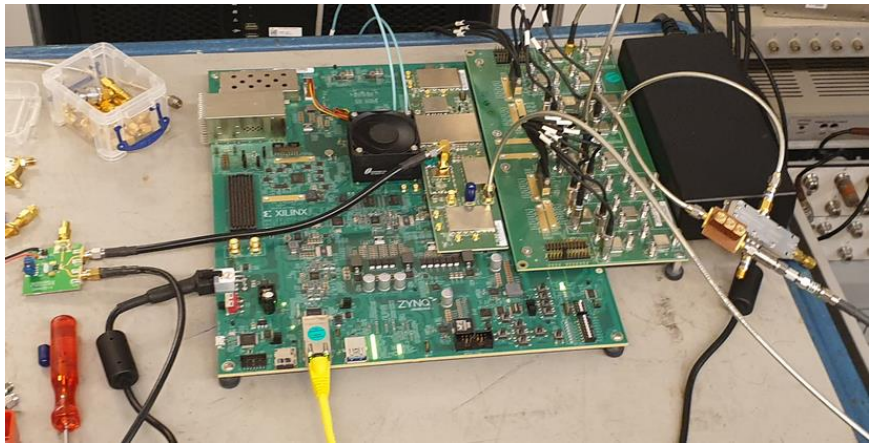




First measurements at PETRA III

Using Zynq UltraScale+ RFSoC ZCU208 Evaluation Kit

- Analog electronics analytically modelled to have SNR 70 dB
- Digitizer on evaluation board experimentally tested both in the laboratory setup and at PETRA III
- Dominant noise source is the digitizer front-end noise limiting the resolution
- **Project requirements (SNR > 60dB) are fulfilled**
  - SNR can be improved by ADC parallelization and pulse multiplication to more than 70 dB



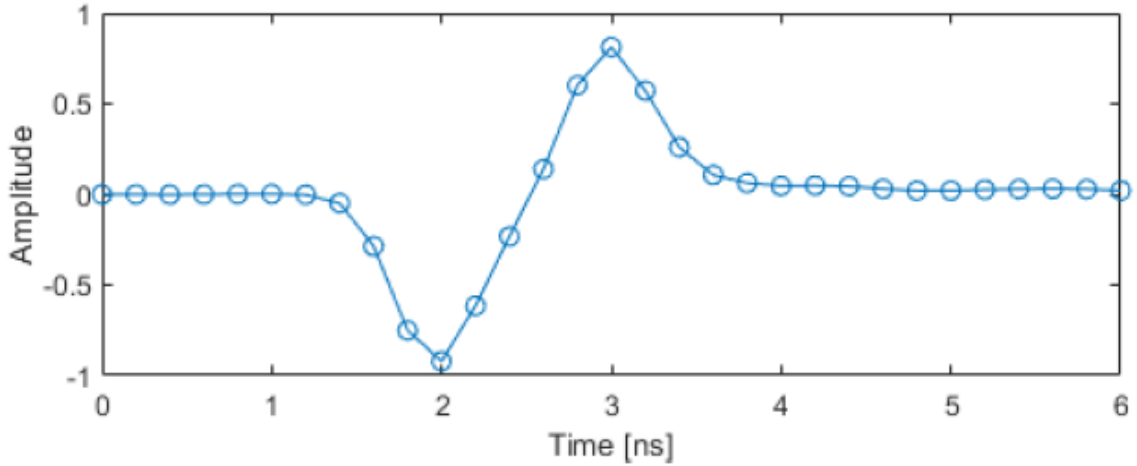


Figure 3: Digitized bunch pulse at PETRA III with the sampling rate of 5 GSPS.

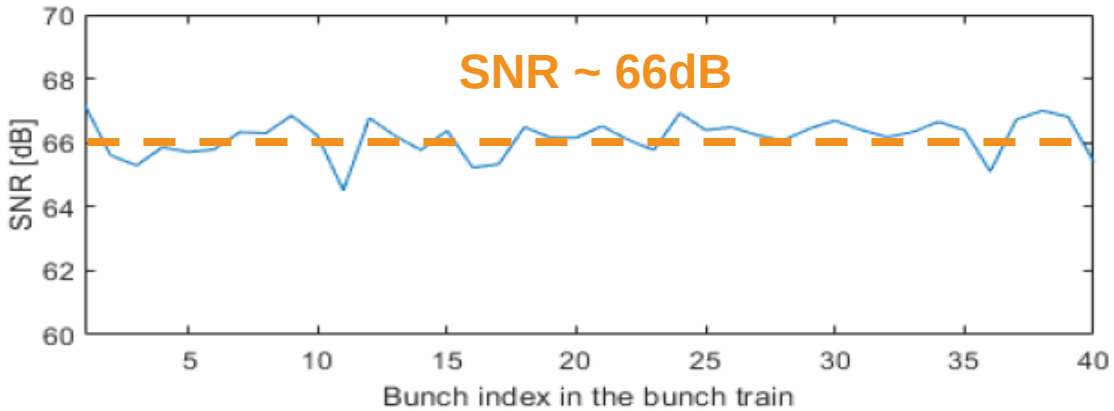


Figure 4: SNR of the RFSoC based T-MBFB detector evaluated at PETRA III in the timing mode with 40 bunches.

→ Expected SNR PIV ~63dB

PETRA IV MBFB diagnostics / active control

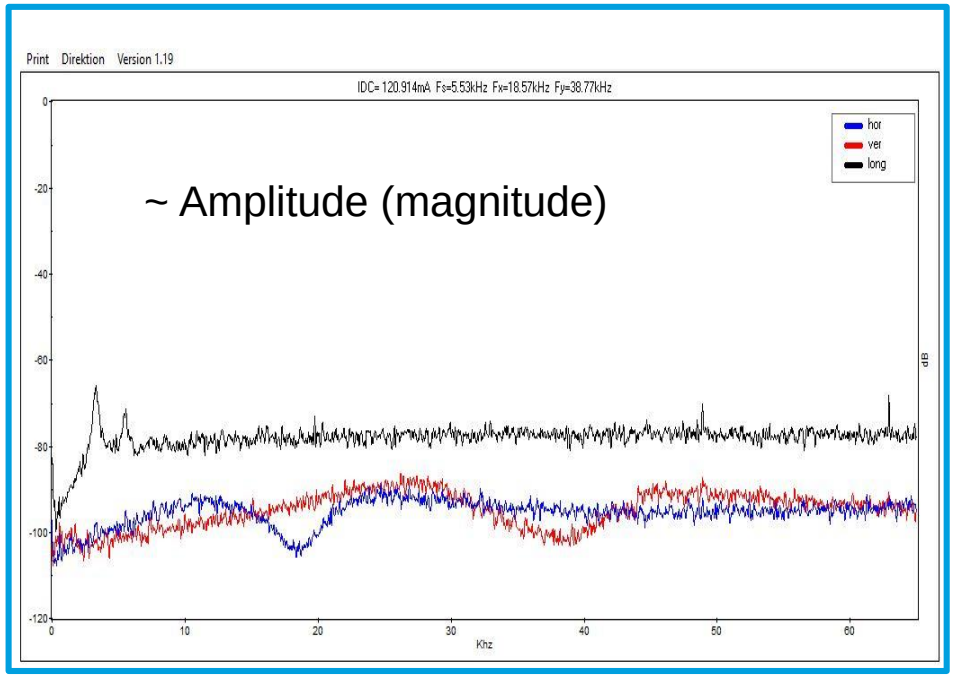
Bunch by bunch diagnostics

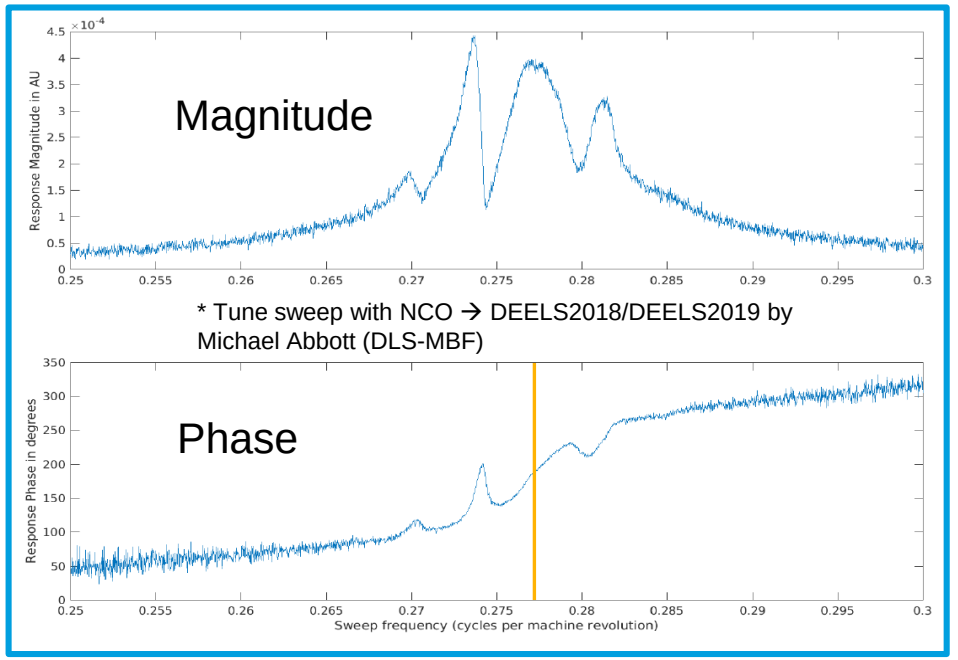
Measurement of beam transfer function

- Transverse (betatron) oscillations
  - Noise holes / dip with medium resolution close to noise floor under feedback control with relatively large feedback gain
    - $\sigma(\beta)/\beta \approx 1\%$ (typical PIII deviation)
  - Tune sweep with NCO* of 1 bunch → high resolution
    - Open loop → Beam transfer function
    - Closed loop → Combination of feedback damping and NCO excitation
- Longitudinal (synchrotron) oscillations
  - Bunch by bunch phase variations → should not occur at PIV
  - If so, send this information to BLs or LLRF

Additional diagnostics

- Relative charge and absolute bunch position
- …





* Tune sweep with NCO → DEELS2018/DEELS2019 by Michael Abbott (DLS-MBF)

PETRA IV MBFB diagnostics / active control

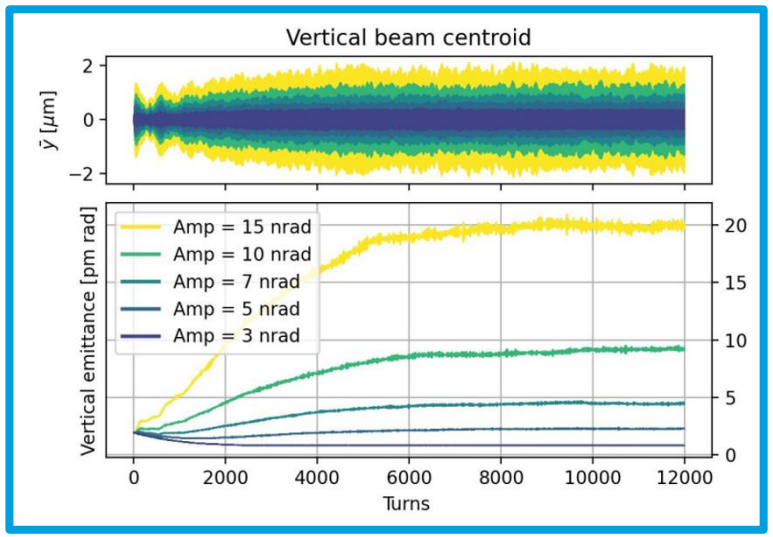
Bunch by bunch feedback

How to preserve low emittance under FB control?

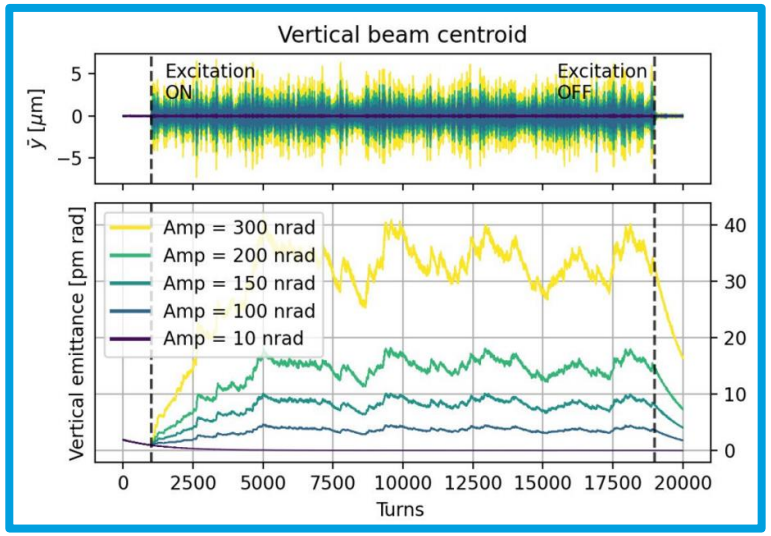
eurizon
Deliverable no. 4.17

- Active transverse feedback for multi-bunch instabilities with only slight inflation of the emittance
  - Simulation required → beam physics and feedback group
- Simulation of active emittance control for EURIZON
  - Blow up to 20pm.rad doable, BUT larger (10%) mean orbit variations depending on excitation signal for nominal beam size of 11.8µm
  - For vertical emittance target of 10pm.rad, it drops to 4% of the beam size → barely acceptable value for orbital distortion
- Cleaning of parasitic bunches
- Growth-/damp rate measurements
- …
- Event/user based data recording for post mortem analysis
- …

Colored noise excitation



Betatron as excitation frequency



Simulations by C.Cortes

Summary

- PETRA III hardware status and upgrade planning for MBFB system
- MicroTCA.4 based system under design with RFSoC as main processing unit
- Collection of specifications of new board (DAMC-DS5014DR) for various applications
  - Chip proposed: XCZU47DR-1FFVG1517E with 8 ADCs (14-bit 5GSPS) and 8 DACs (14-bit 10GSPS)
  - Project owner at DESY → Behzad Boghrati (behzad.boghrati@desy.de)
  - Recommended 2 step (foreground/background) ADC calibration mechanism

    → Need to be clarified if needed, and know how to implement the short-circuit for the inputs

    → Recommendations / suggestions welcome
- MBFB diagnostics and communication to other subsystems
- MBFB with active feedback control while preserving the low emittance
  - Simulations required at DESY
  - Suggestions from community welcome

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Thank you

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