



IPE DAQ for TRISTAN



Max-Planck-Institut für Physik
(Werner-Heisenberg-Institut)

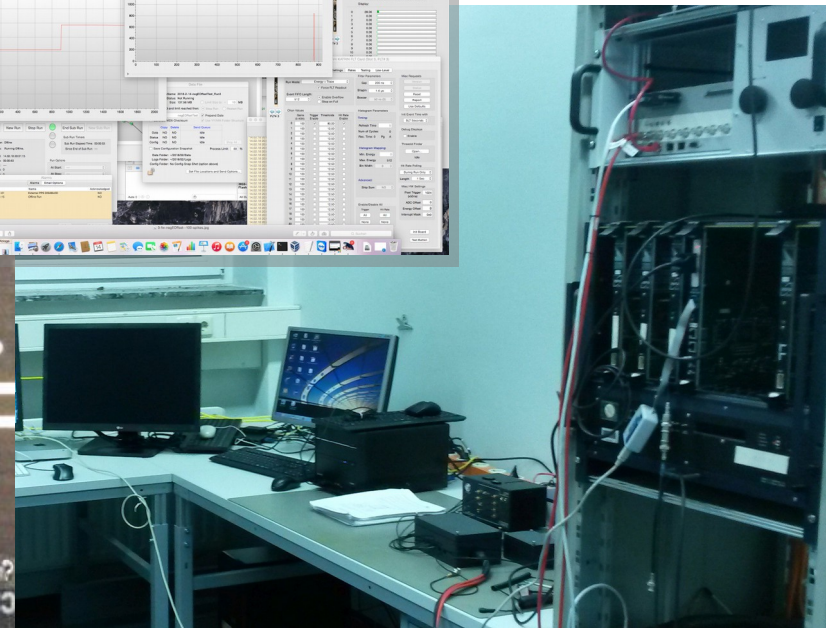
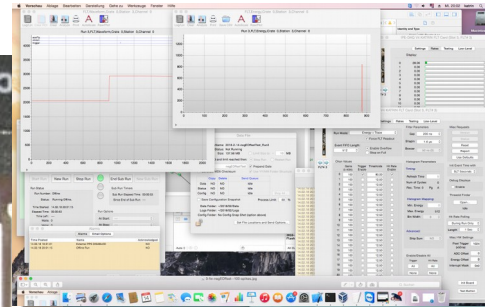
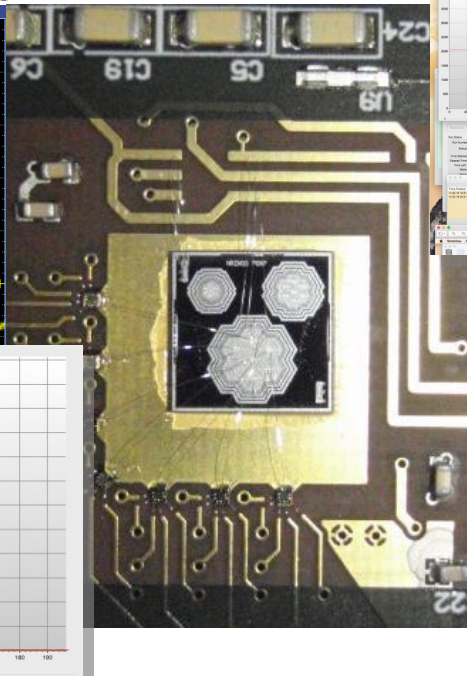
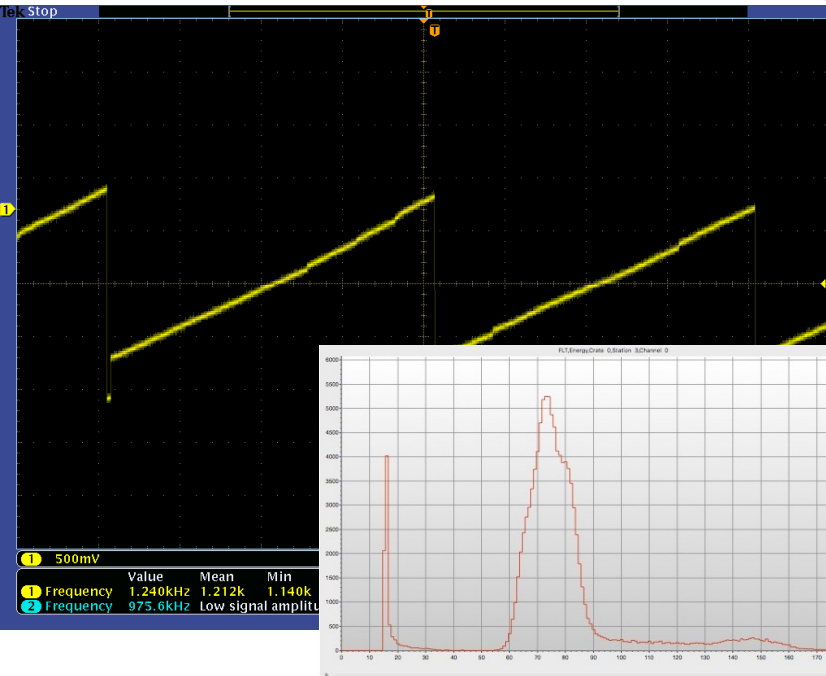
KIT TRISTAN lab: characterising the IPE4 DAQ system

Till Bergmann

34th KATRIN Collaboration Meeting
February 2018



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Tasks

- IPE4 crate + ORCA upgrade + recommissioning
- Data taking with IPE4+ORCA
- Investigate KATRIN trigger for TRISTAN signals
- Support TRISTAN MTCA crate development

TRISTAN Test Stand at KIT

Marc Korzeczek,
KIT, IKP

Crate PC
Linux

Building 601
Room 106A

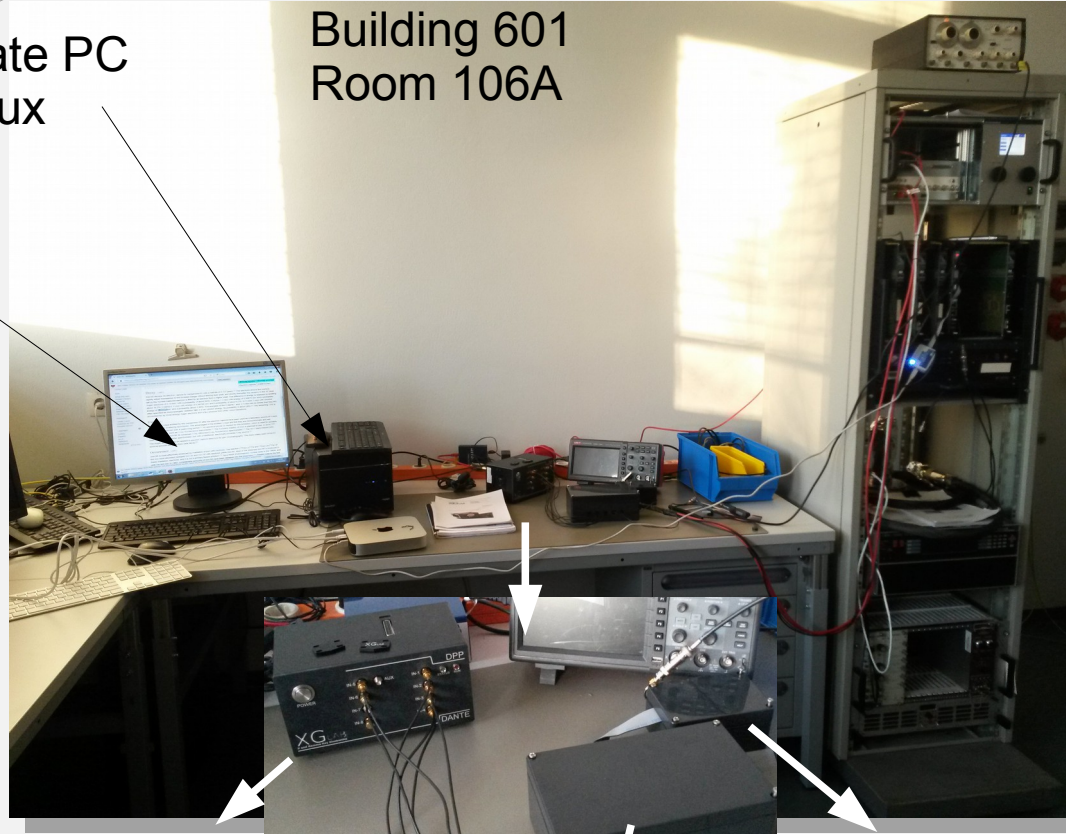
Testpulser

PC + XGlab
software

Power Supply



MacMini
ORCA

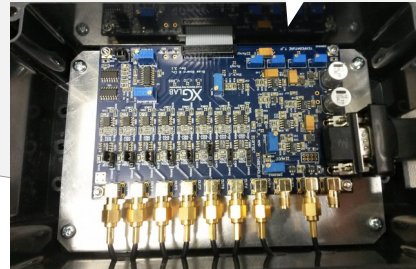


IPE4 Crate

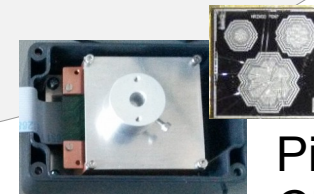
E-Gun



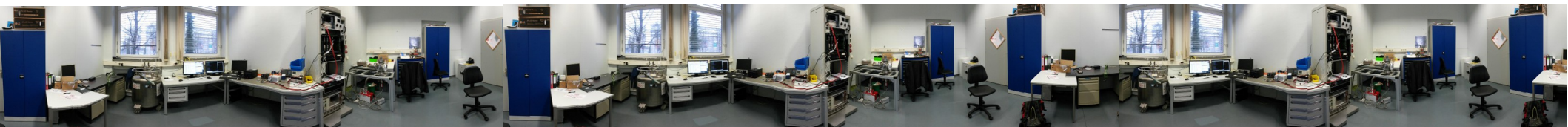
XGlab DANTE DAQ



XGlab Bias Board



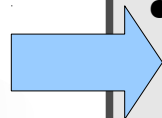
Pixel detector +
CUBE ASIC +
Fe55 source



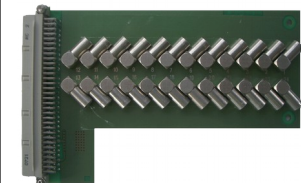
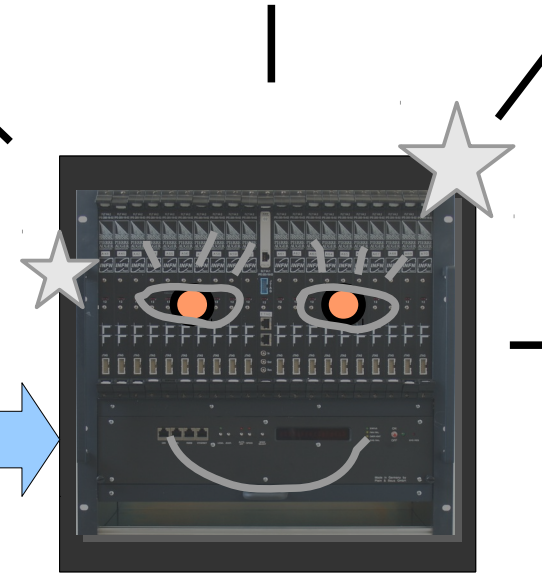
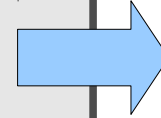
IPE4 Crate Upgrade



Former Myon Panel DAQ,
unused for ~ 2 years

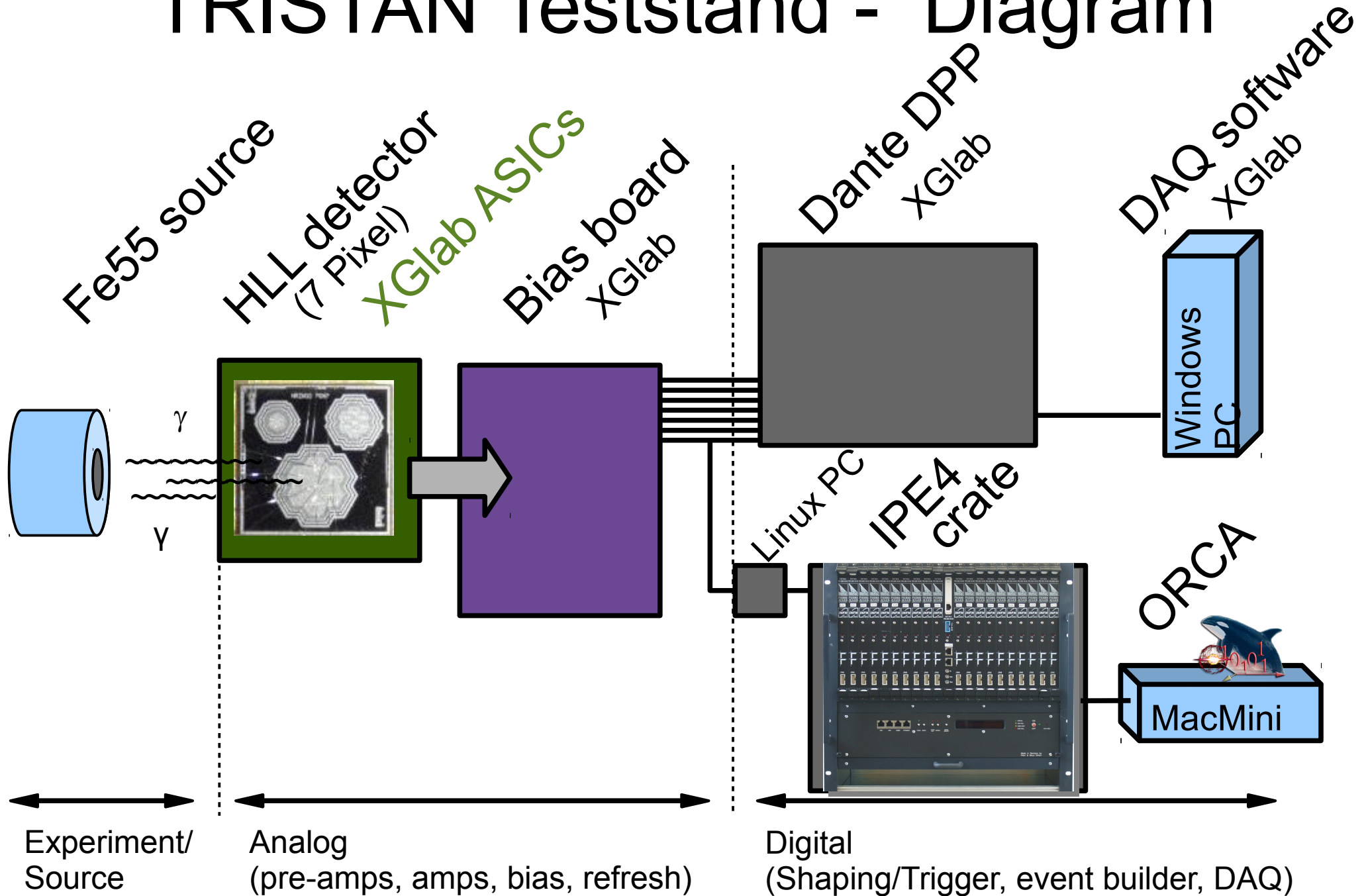


- PrPMC Replacement
→ PCIeexpress Link +
Crate PC
- Firmware (FPGA)
- SLT driver
- Crate PC: Linux +
hardware library
- MacMini setup
- Orca
- OrcaRoot
- Router (local LAN)
- modified Lemo Adapter
(Sascha Wüstling)



ch 1-8:
polarity
reversed

TRISTAN Teststand - Diagram

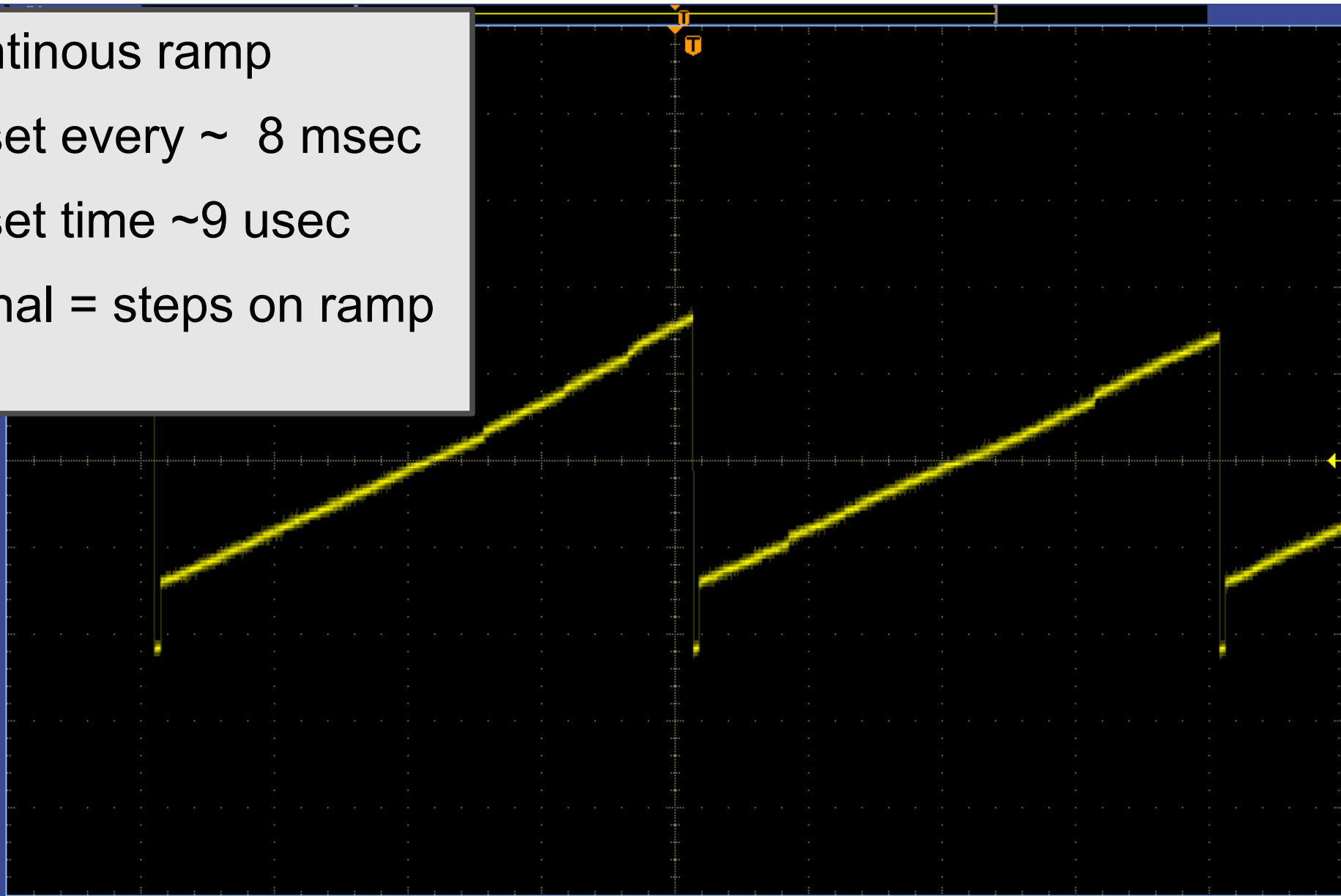


Data taking with IPE4+ORCA

- Details of the detector signal using a Fe55 source
- Compare DANTE and IPE4 data
- Issues

Signal from Fe55 source

- Continuous ramp
- Reset every ~ 8 msec
- Reset time ~ 9 usec
- Signal = steps on ramp



1 500mV

200 μ s

50.0MS/s
100k points

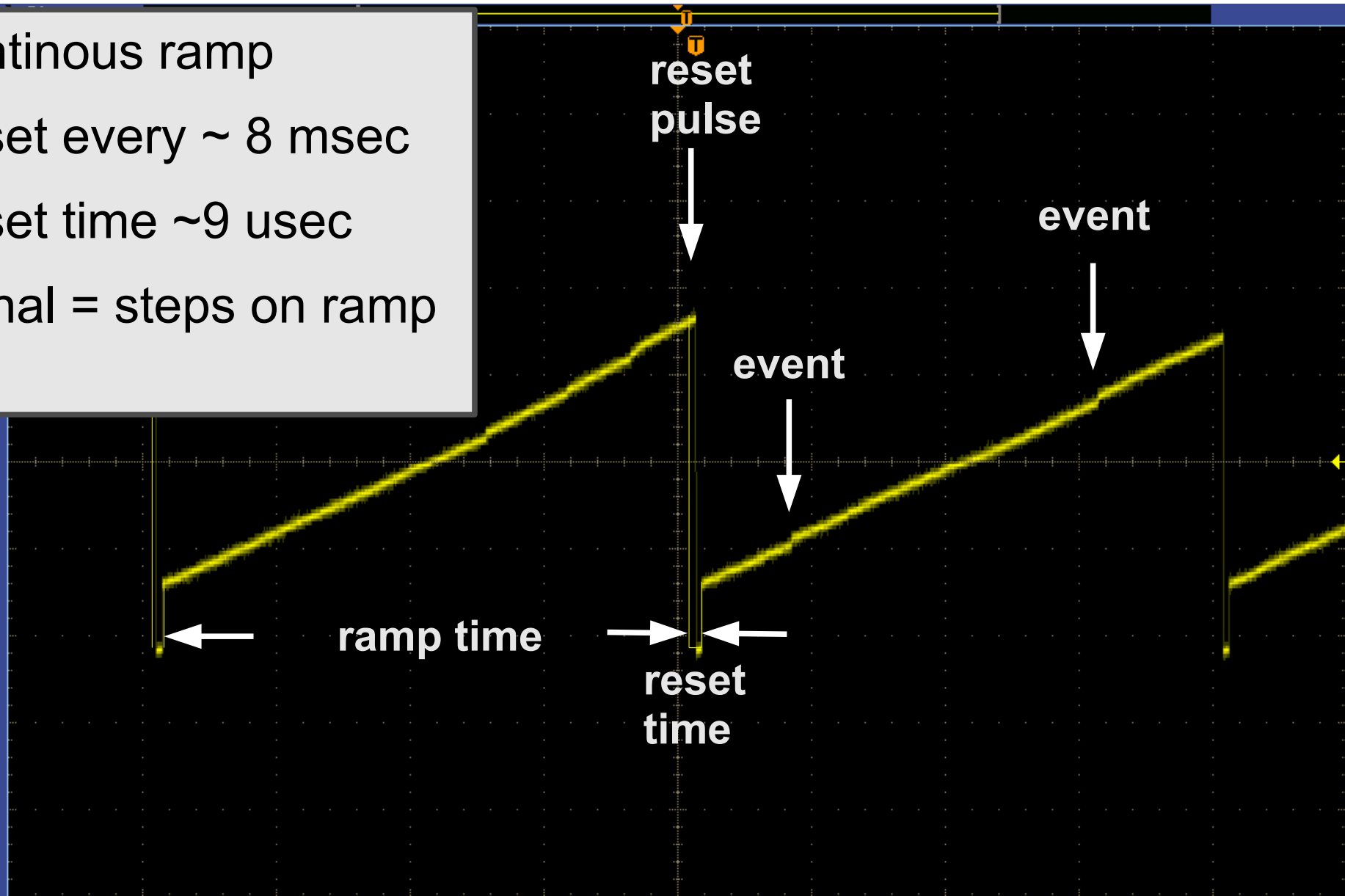
1 \sim -700mV

	Value	Mean	Min	Max	Std Dev
1 Frequency	1.240kHz	1.212k	1.140k	1.252k	40.99
2 Frequency	975.6kHz	Low signal amplitude			

\rightarrow -28.00000 μ s

Signal from Fe55 source

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200µs

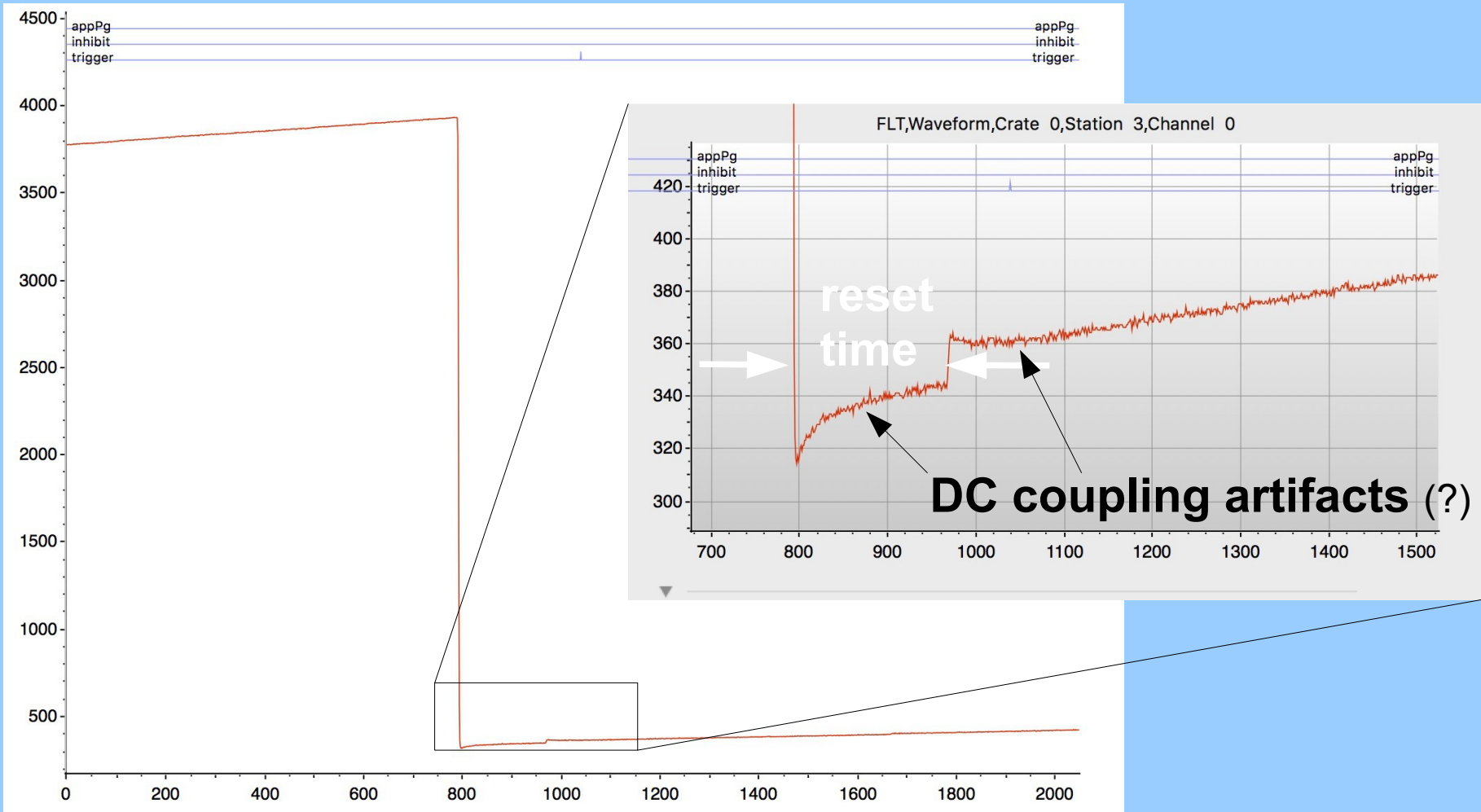
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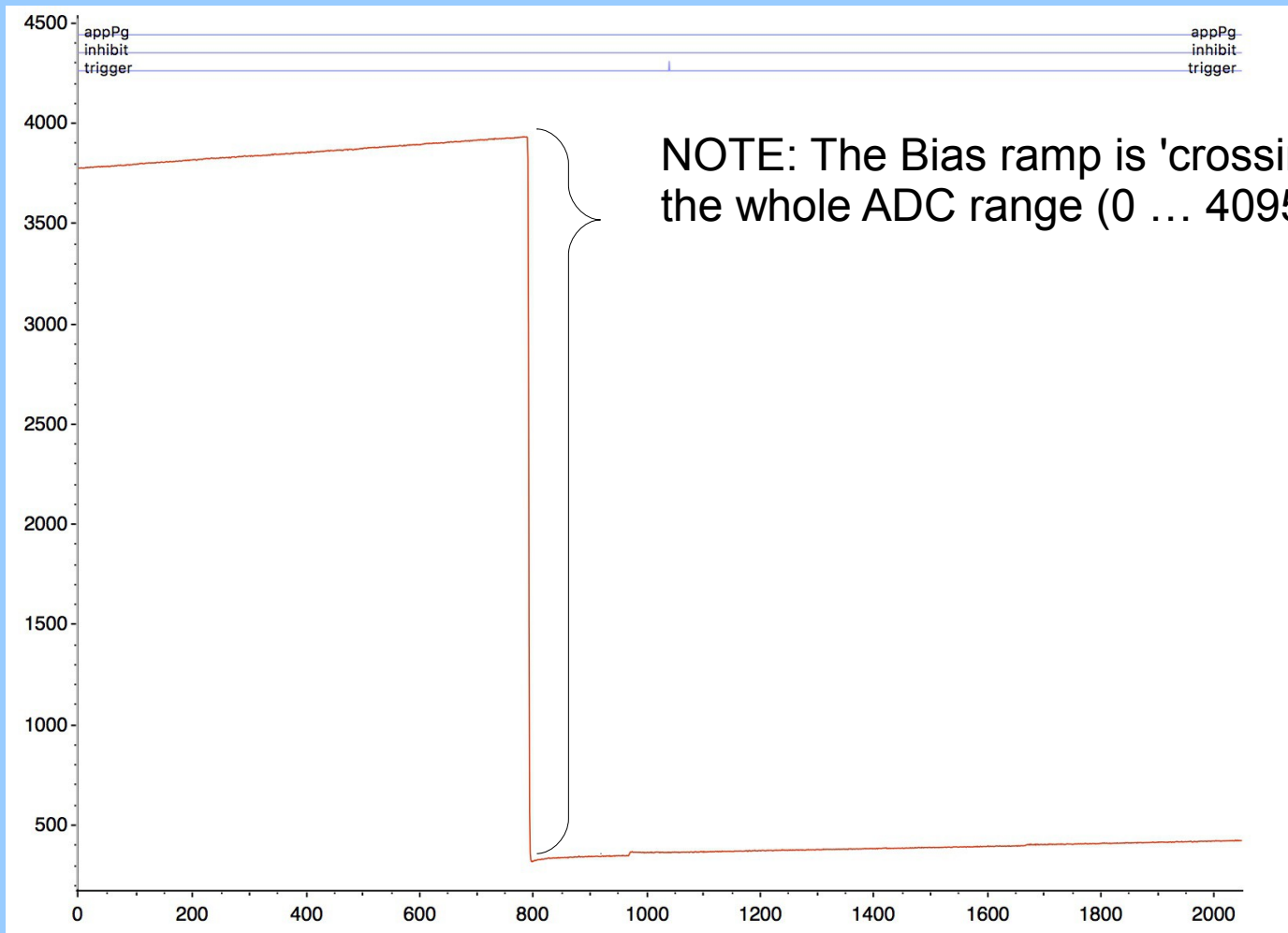
Waveforms/signals



ADC units
t/50 nsec

Reset Pulse

Waveforms/signals

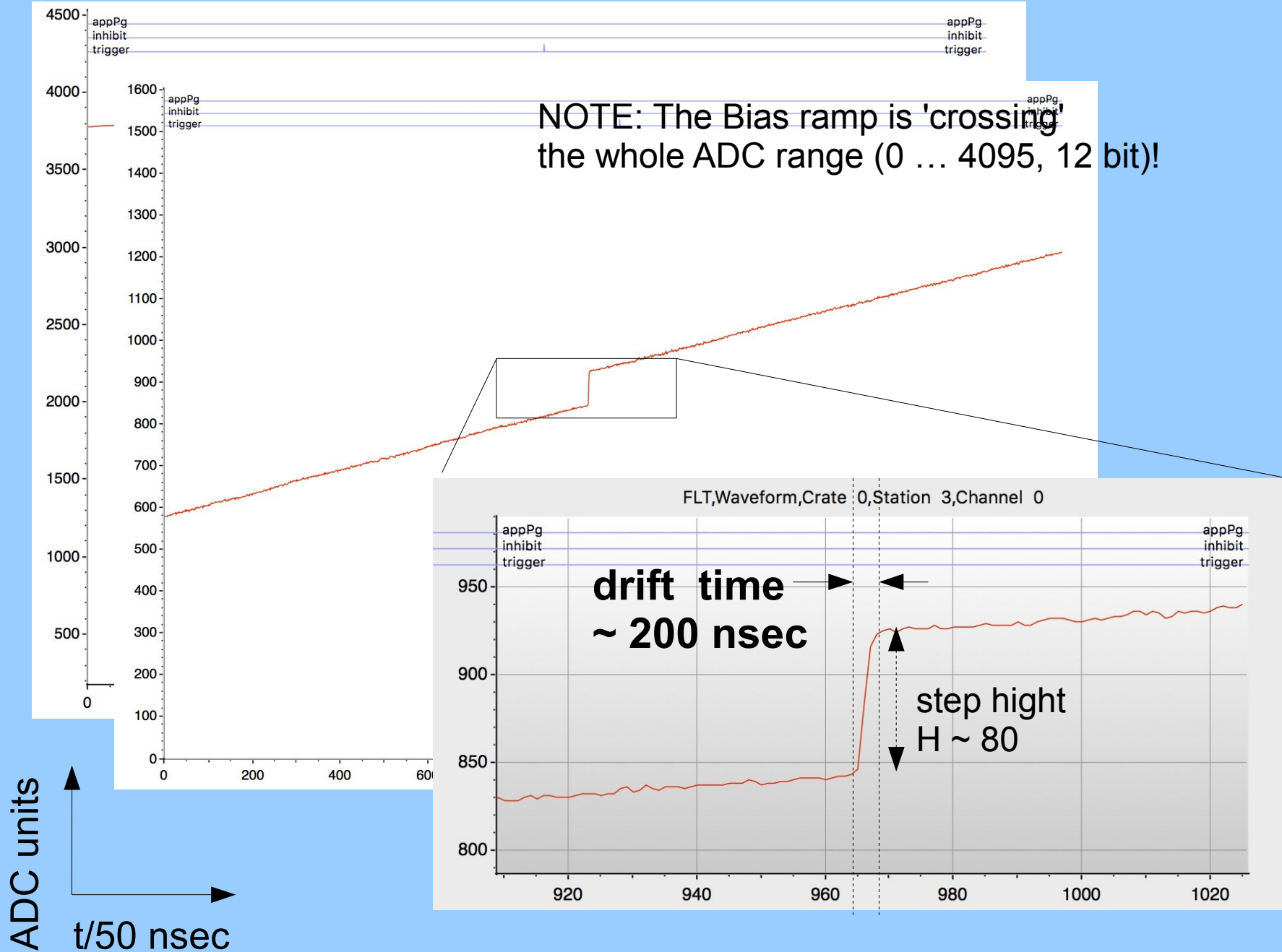


ADC units
↑
t/50 nsec
→

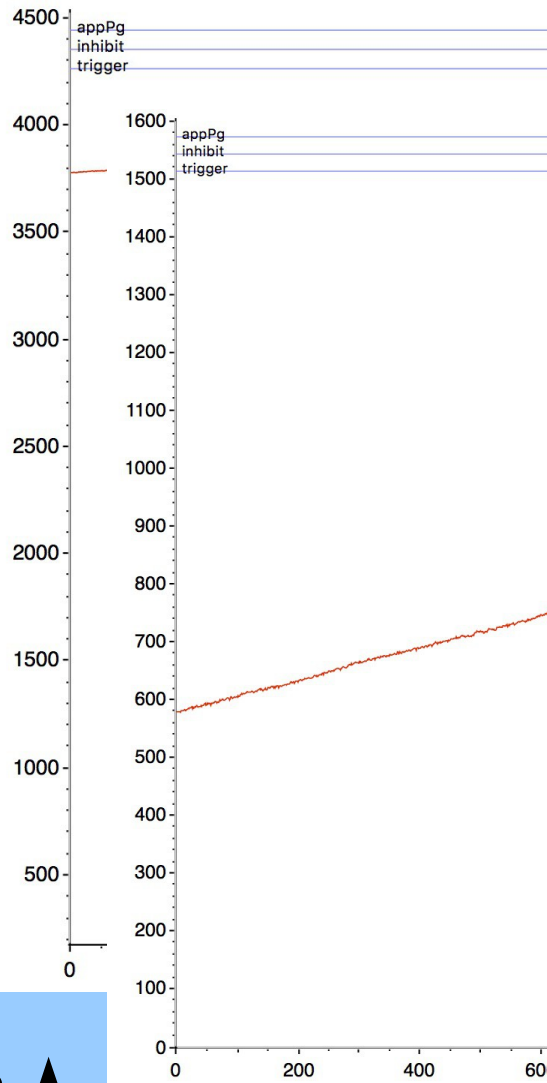
Reset Pulse

Waveforms/signals

NOTE: The Bias ramp is 'crossing' the whole ADC range (0 ... 4095, 12 bit)!

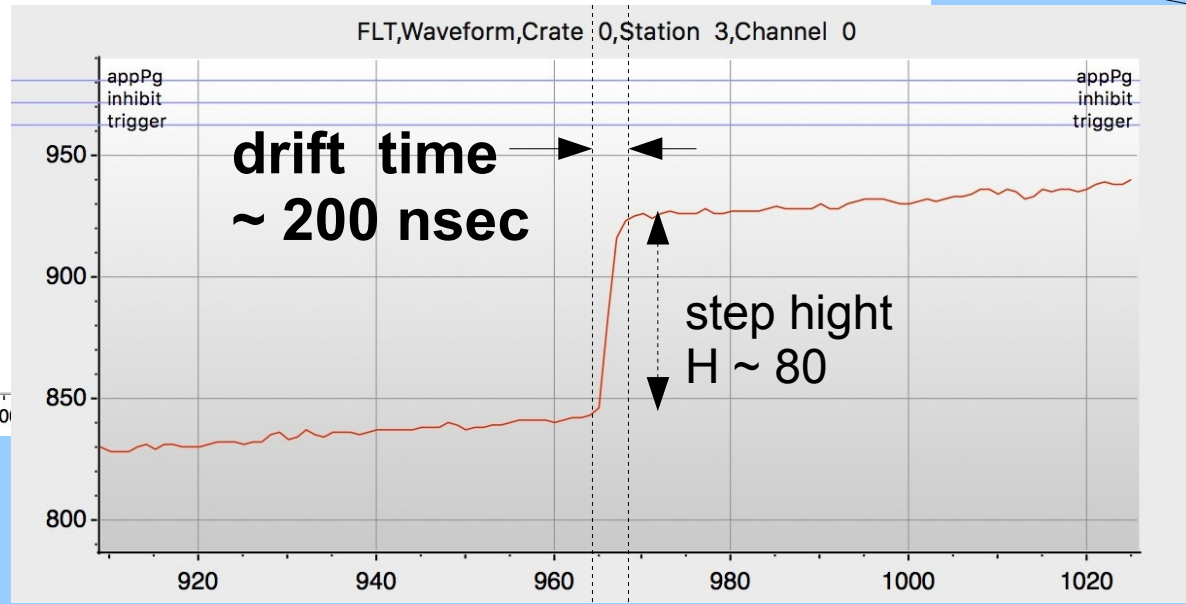


Waveforms/signals



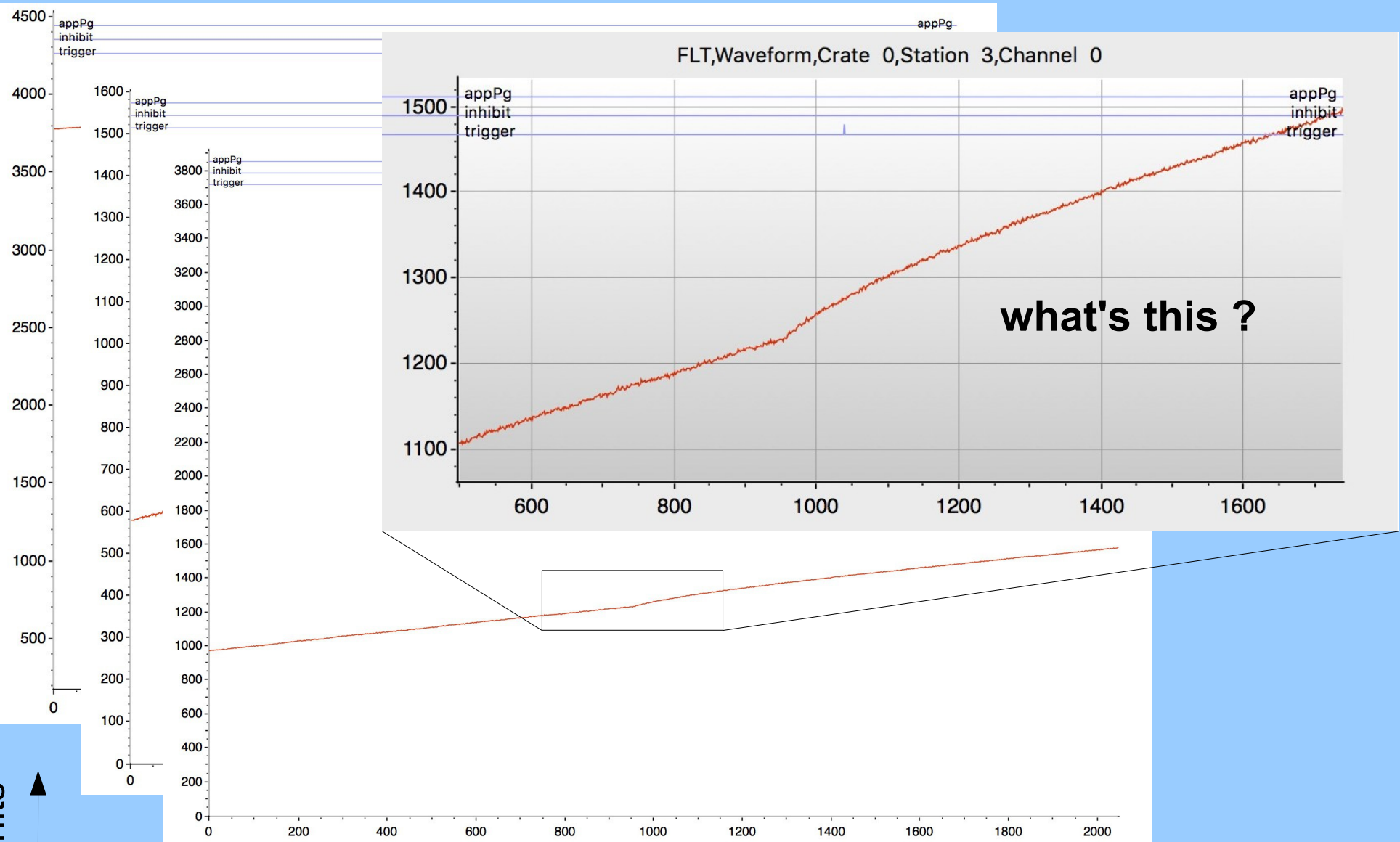
NOTE: The Bias ramp is 'crossing' the whole ADC range (0 ... 4095, 12 bit)!

- cannot amplify the signal
- reduced ADC resolution (~ 80 ADC units or ~ 2 % of the full ADC range or ~ 7 bit)



ADC units
t/50 nsec

Waveforms/signals

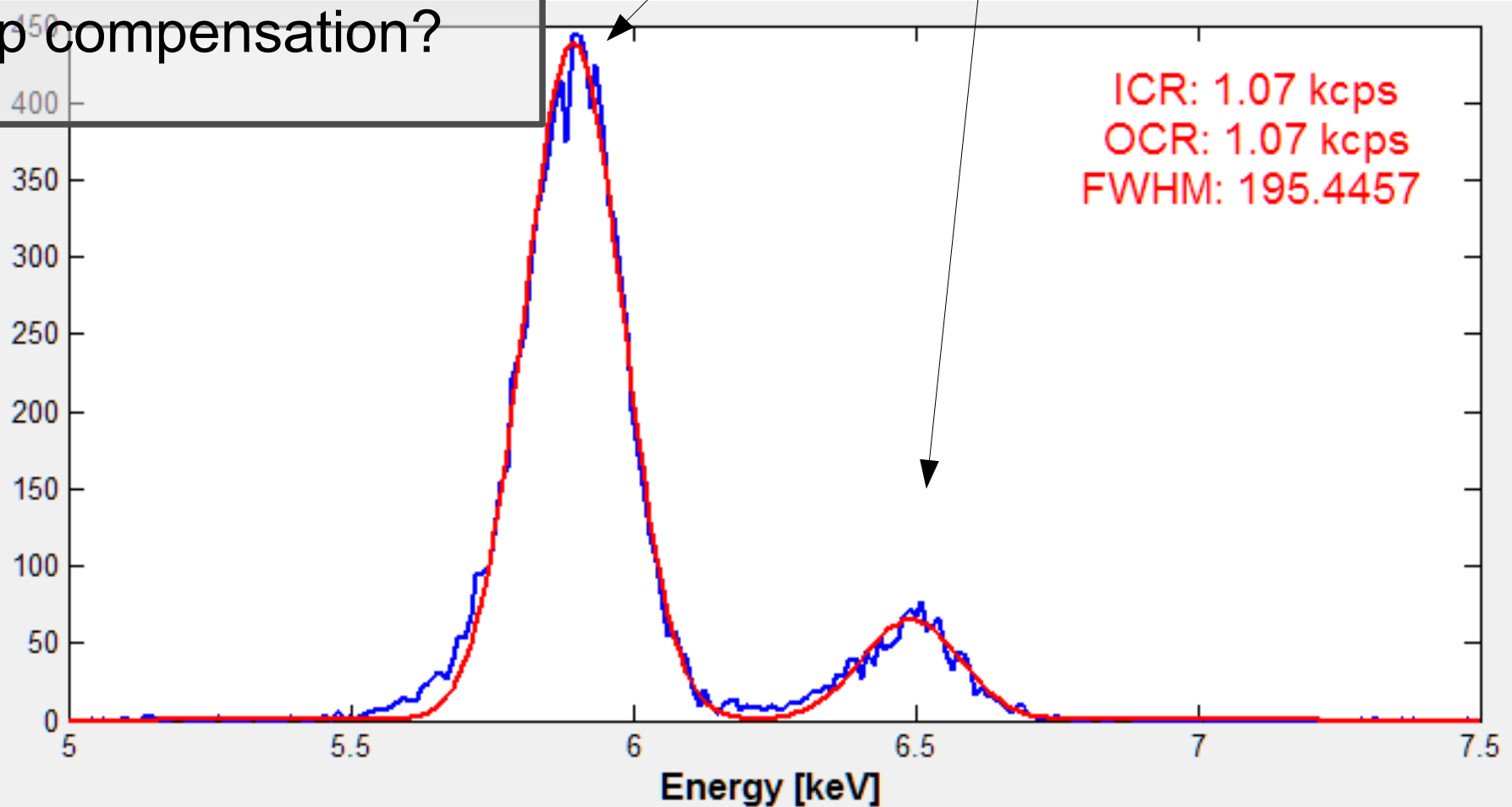


ADC units
t/50 nsec

Energy spectrum Dante

- ADC: 16 bit, 62.5 MHz (?)
- Complex trigger (shaper, pileup detection, edge detection)
- Ramp compensation?

Zoom to the energy peaks at 5.9 and 6.5 keV of Fe55



Energy spectrum IPE4

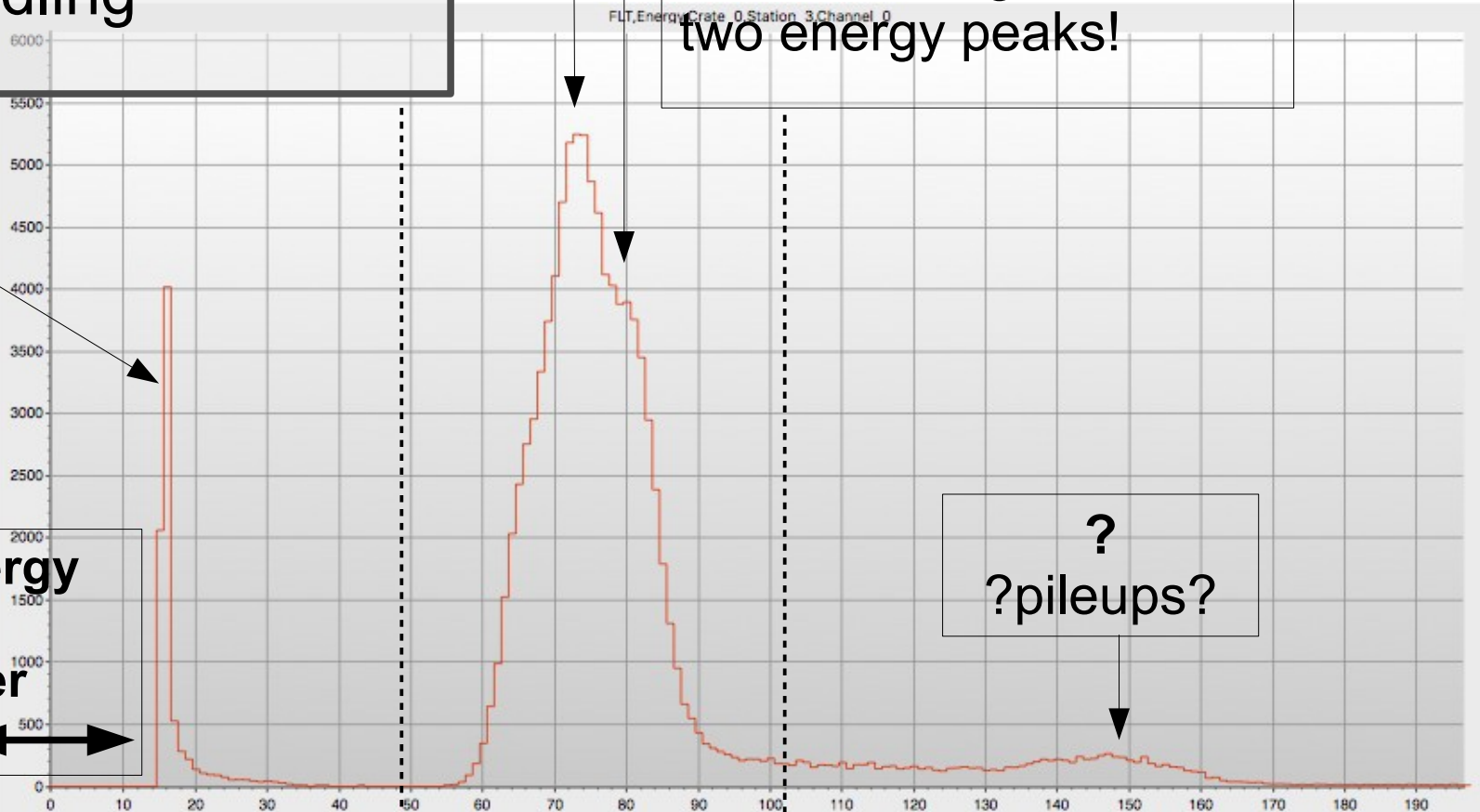
- ADC: 12 bit, 20 MHz
- KATRIN trigger (trapezoidal filter)
- No Ramp and Refresh Pulse handling

Two energy peaks?

cannot distinguish the two energy peaks!

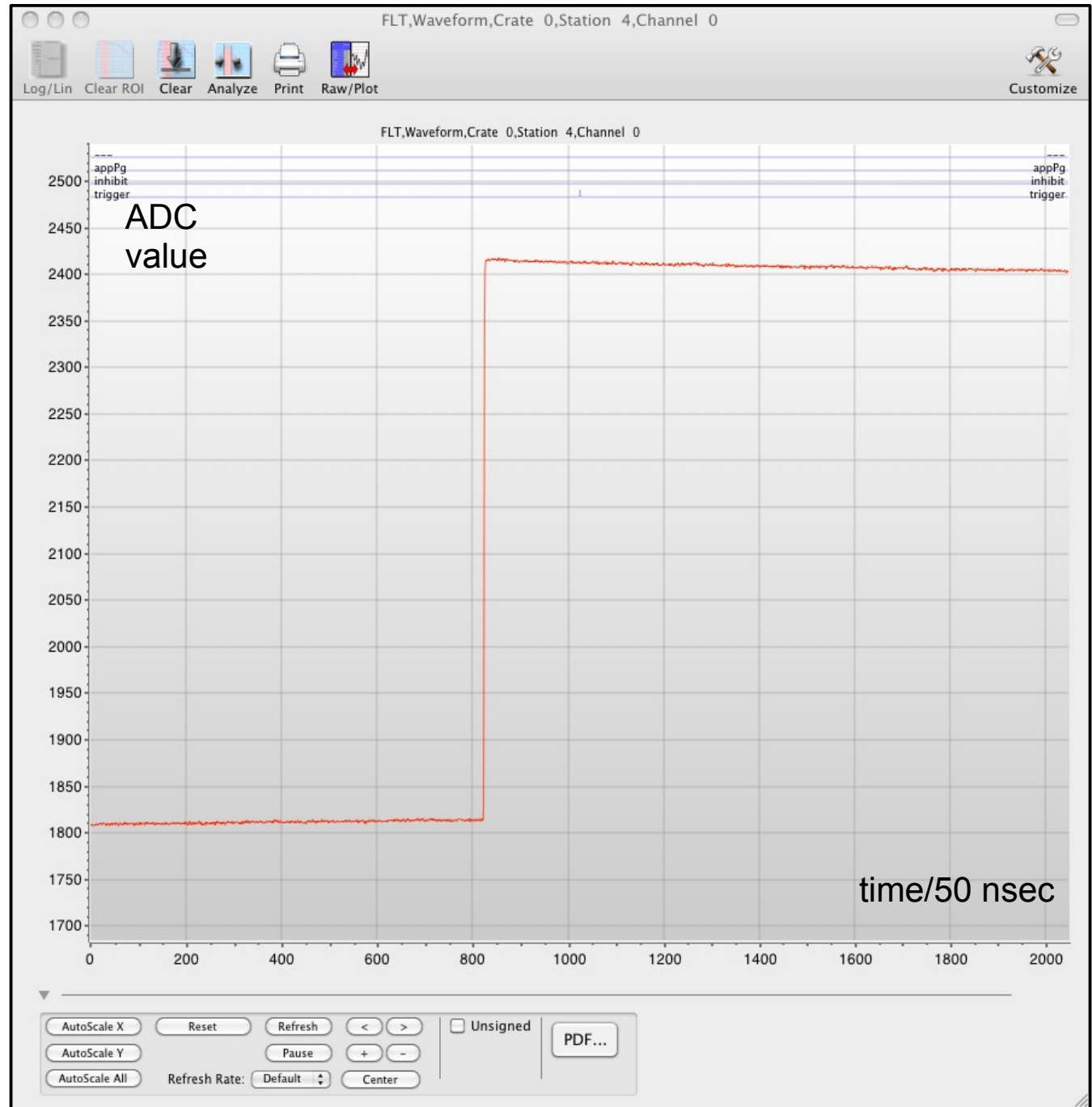
Reset pulse

Observation: energy shifts depending on KATRIN trigger settings

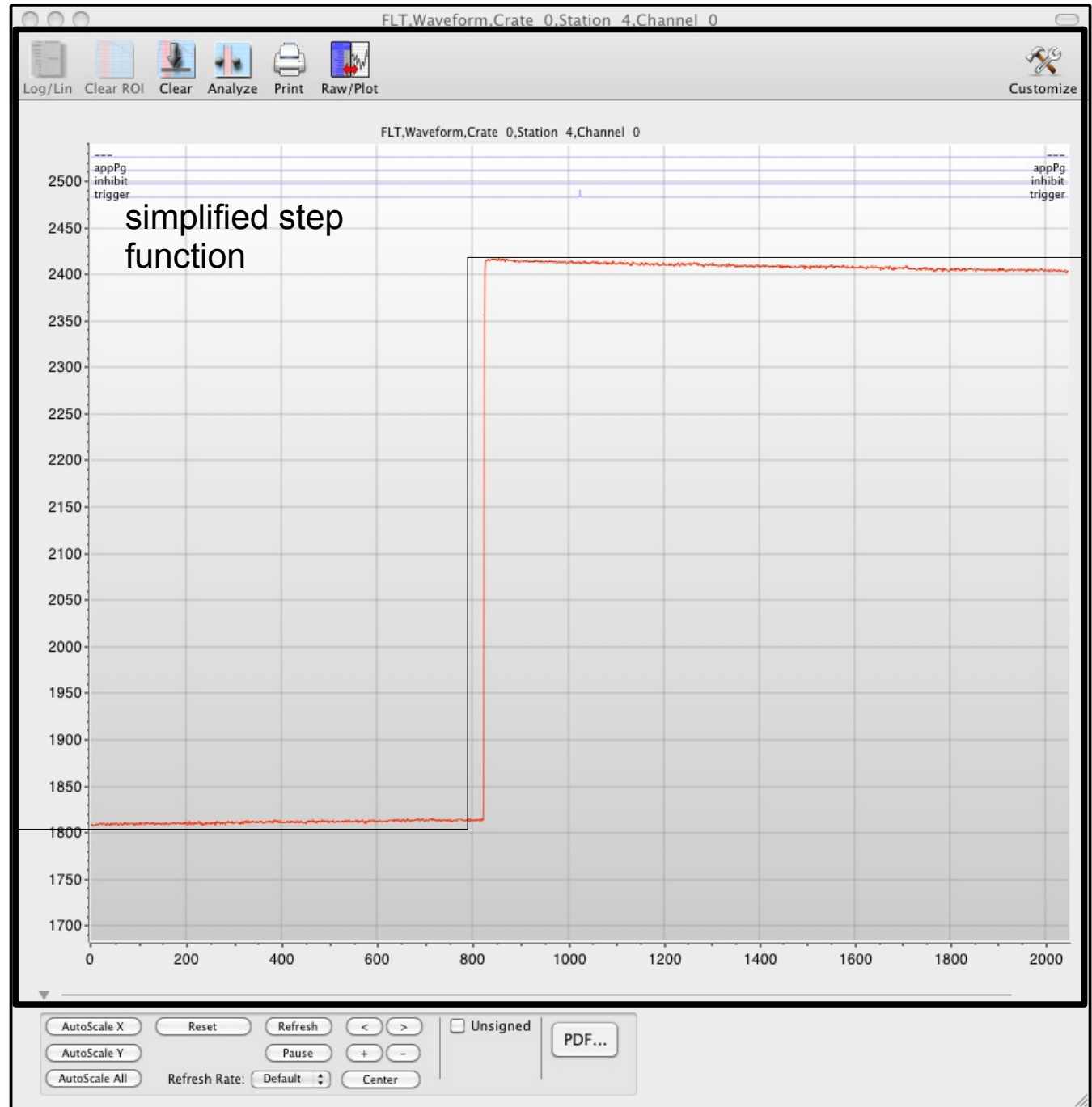


The KATRIN trigger in a nutshell

- observed energy shifts depending on KATRIN trigger settings
- → short excursion to KATRIN trigger



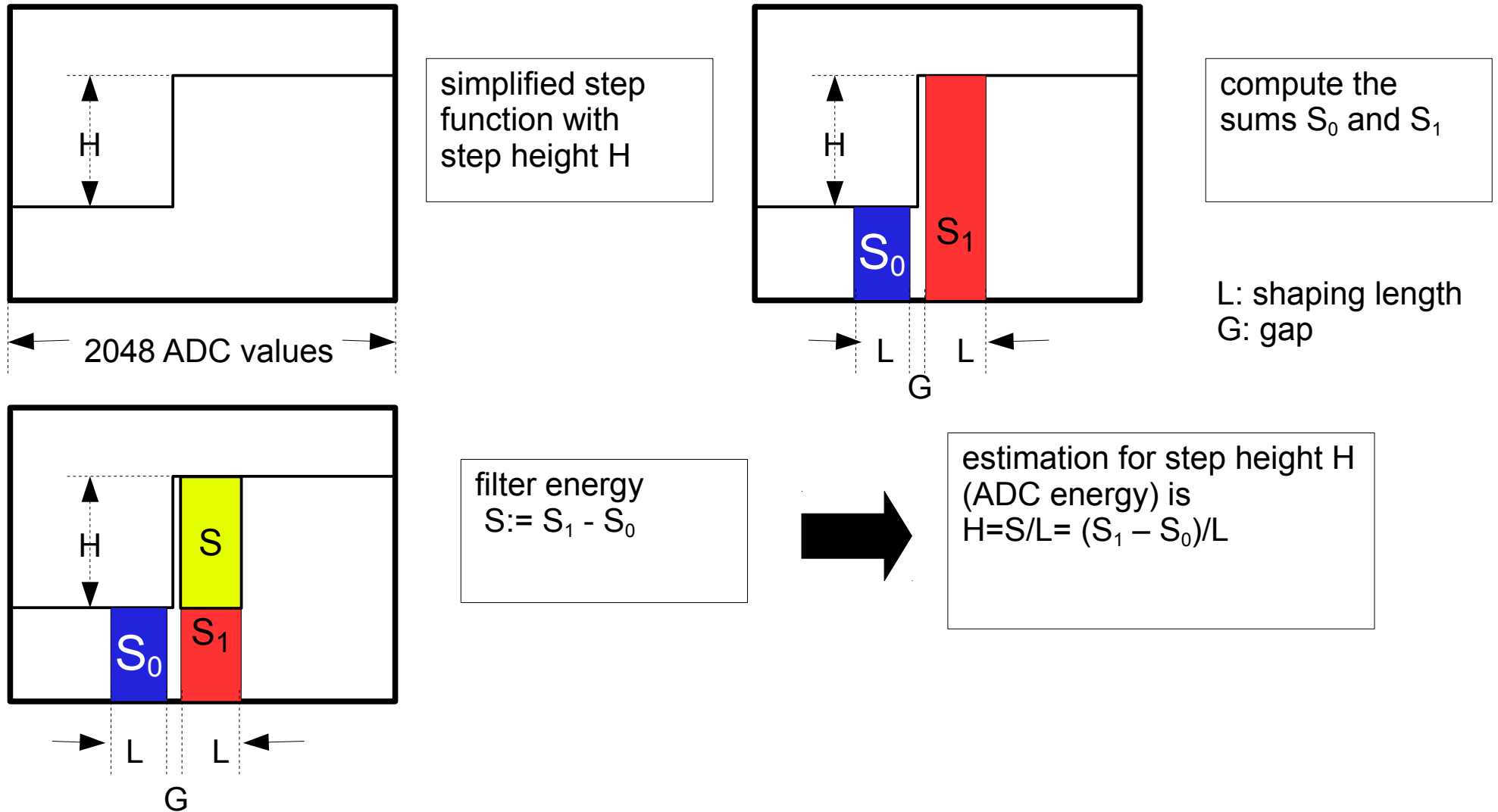
The KATRIN trigger in a nutshell



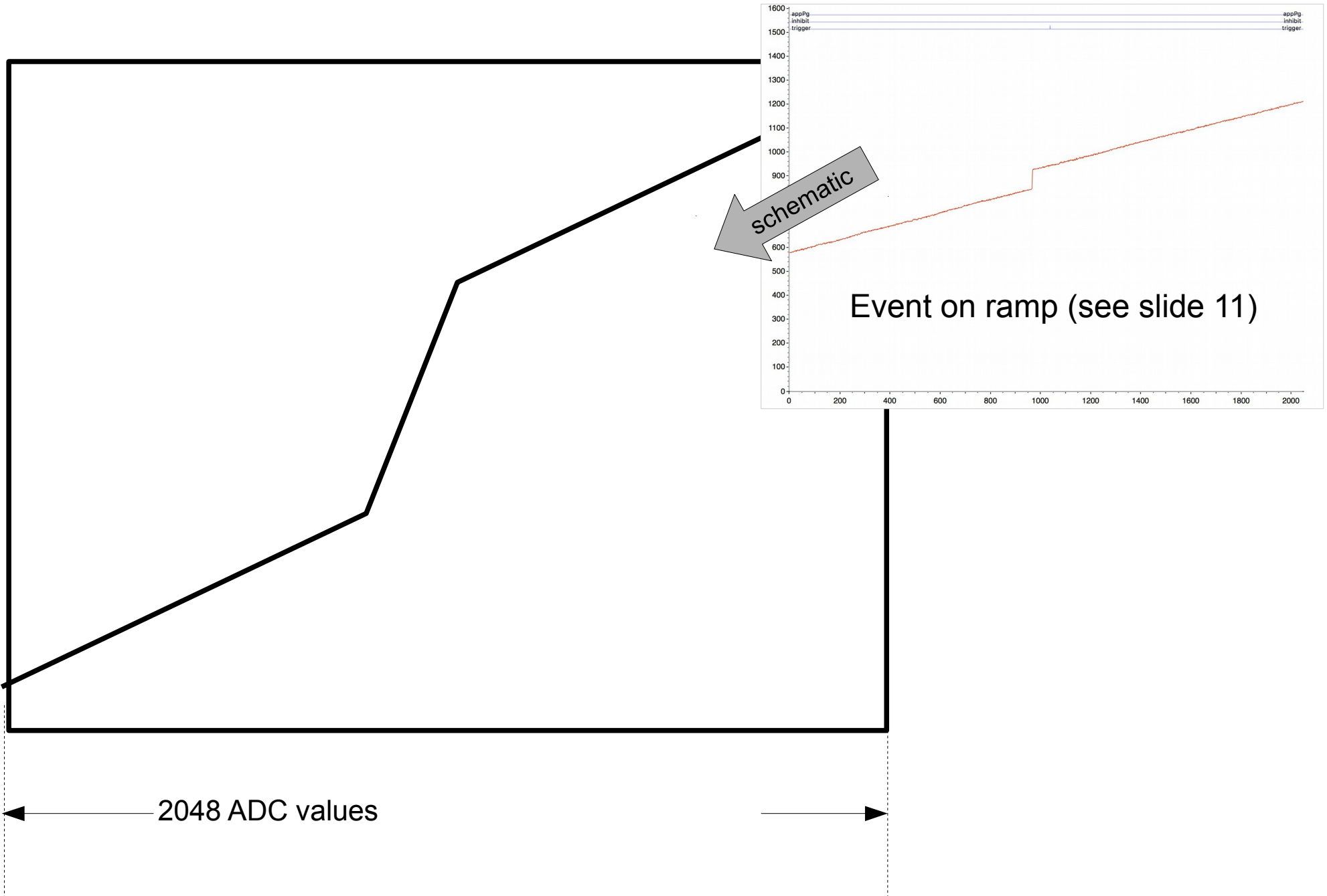
The KATRIN trigger in a nutshell



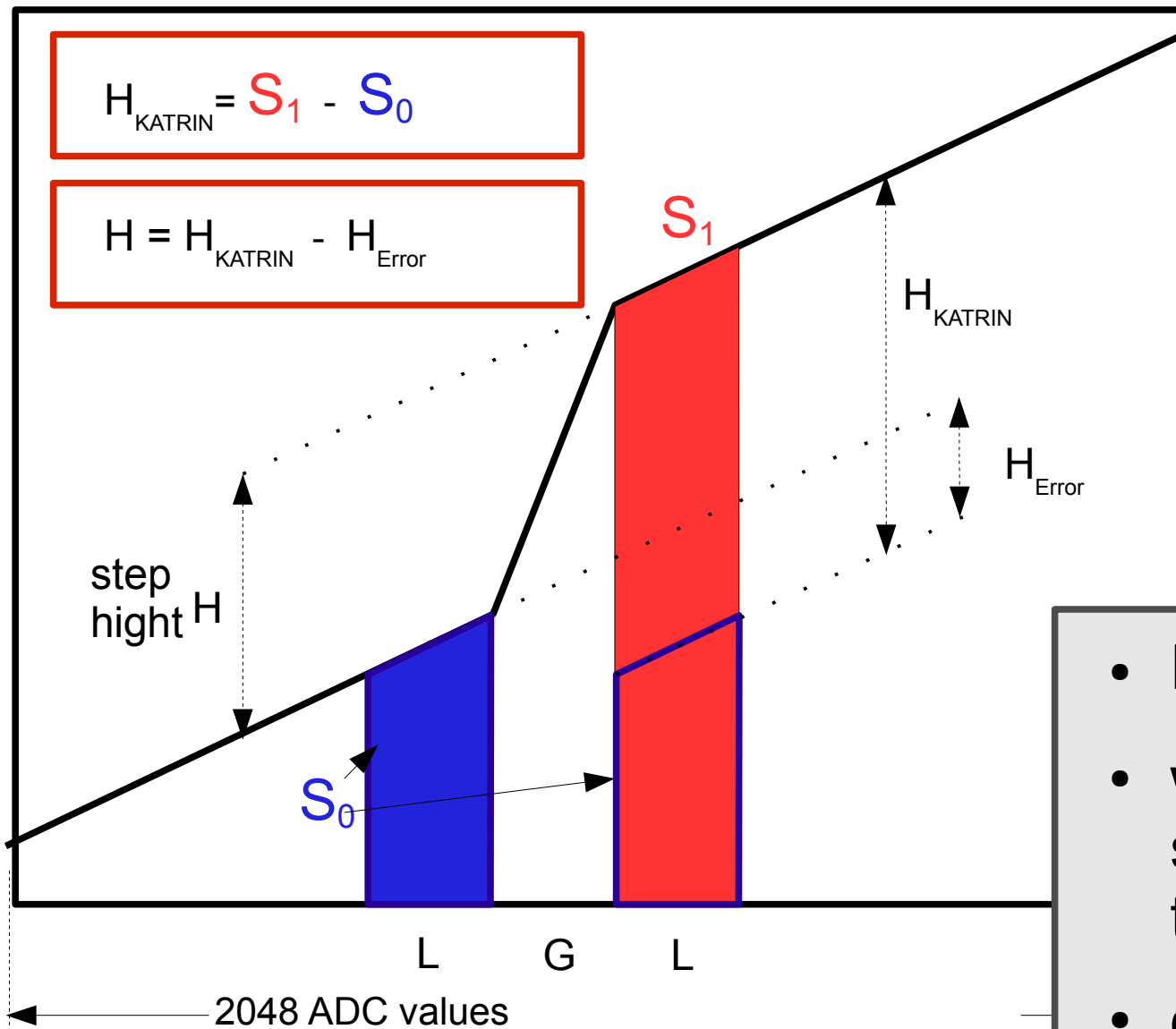
The KATRIN trigger in a nutshell



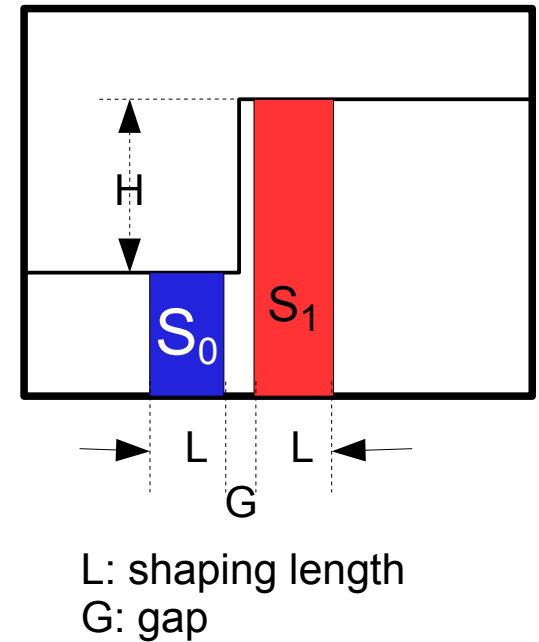
The KATRIN trigger with Bias ramp



The KATRIN trigger with Bias ramp

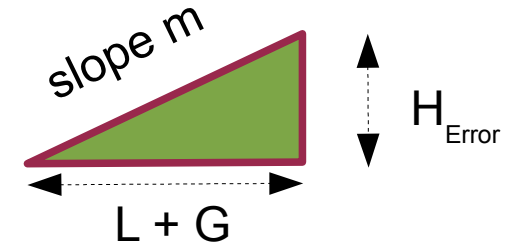
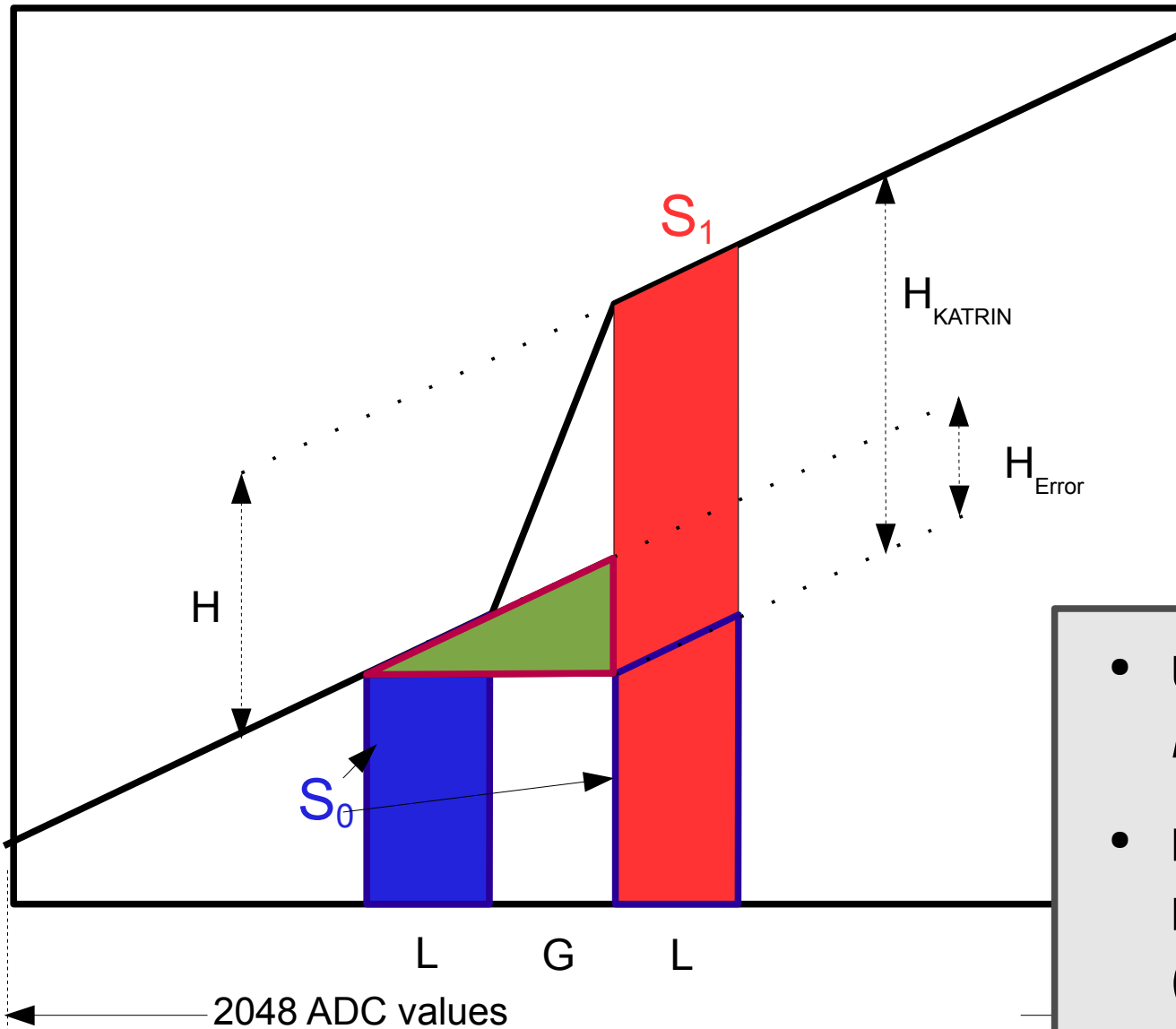


Reminder: without ramp



- H_{KATRIN} is larger than H
- will trigger on smaller thresholds than specified!
- depends on L and G !
(see next slide)

The KATRIN trigger with Bias ramp



$$H_{\text{Error}} = m * (L + G)$$

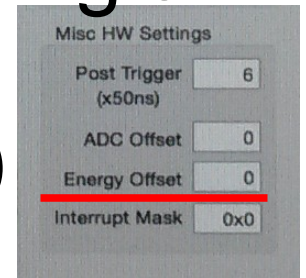
$$H = H_{\text{KATRIN}} - H_{\text{Error}}$$

$$= H_{\text{KATRIN}} - m * (L + G)$$

- use FLT parameter *EnergyOffset*
- new firmware with negative values (currently testing)

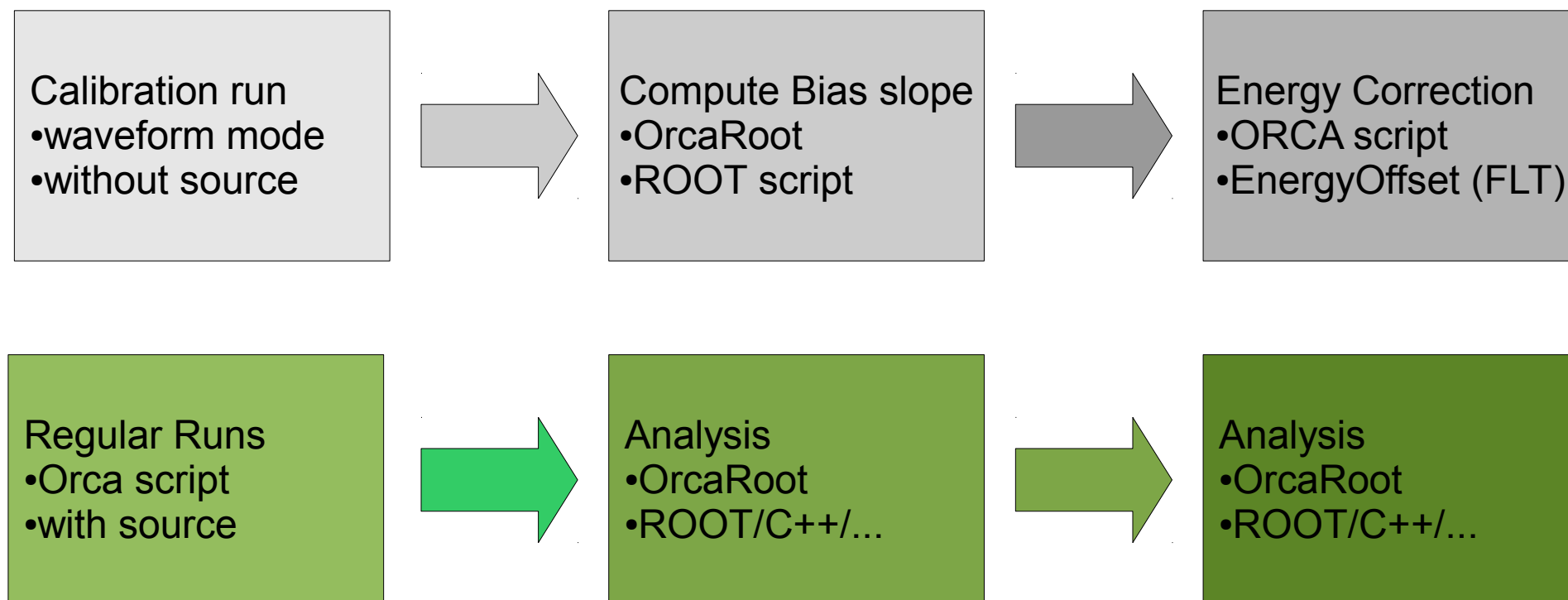
Issues with IPE4 recording and solution

- Bias ramp exhausting the ADC range
→ effectively using only 7-8 bits of the 12 bit ADC
- KATRIN energy trigger: Bias ramp producing a constant energy offset
→ calibration and correction (FPGA level)
- Reset pulse (not critical, recorded as event with sharp energy distribution)
→ use analog inhibit signal (SLT lemo input)



FLT dialog

Suggested DAQ Workflow



MTCA based TRISTAN DAQ ("IPE5 DAQ")

- MTCA = new DAQ standard (successor of VME etc.)
- Kickoff meeting 2018-02-02 in TRISTAN lab: Matthias Balzer, Denis Tcherniakhovski, Oliver Sanders (all KIT/IPE); Marc Korzeczek (KIT/IKP); Till Bergmann (MPP)
- Discussion of tech. specifications (11 pages, Susanne Mertens) and experience from test stand
- Plan: first prototype (7/32 chan?) April 2018, 168 channel prototype end of 2018

TRISTAN DAQ Overview Susanne Mertens, Jan. 2018
11 pages specifications
Specifications for ADC and FPGA
<ul style="list-style-type: none">• 100 MHz sampling rate• ≥ 14 bit• < 0.1 ps clock jitter• < 5 ns time synchronization between channels within one module• As low as possible ADC non-linearity• User-defined time resolution for a multiplicity calculation [over pixel neighbors] [per module]• Waveform mode [write out full waveforms for selected channels, length user-specified up to 40 μs]• Energy mode [write out energy, time, channel, pile-up flag, [multiplicity]]• Histogramming mode [different histograms for: multiplicity 1 - x, pile-up flag]
Three trigger modes



Conclusion

- IPE4 DAQ system upgrade
- Bias ramp: calibration, energy correction (new firmware). Inhibit during reset.
- Suggestions for MTCA development (Bias ramp: cancel out, 16 bit ADC or modified AC coupling?)
- Outlook: IPE4 calibration with Egun

Thank you for your attention!



Thank you for your attention



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The END



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ENDE

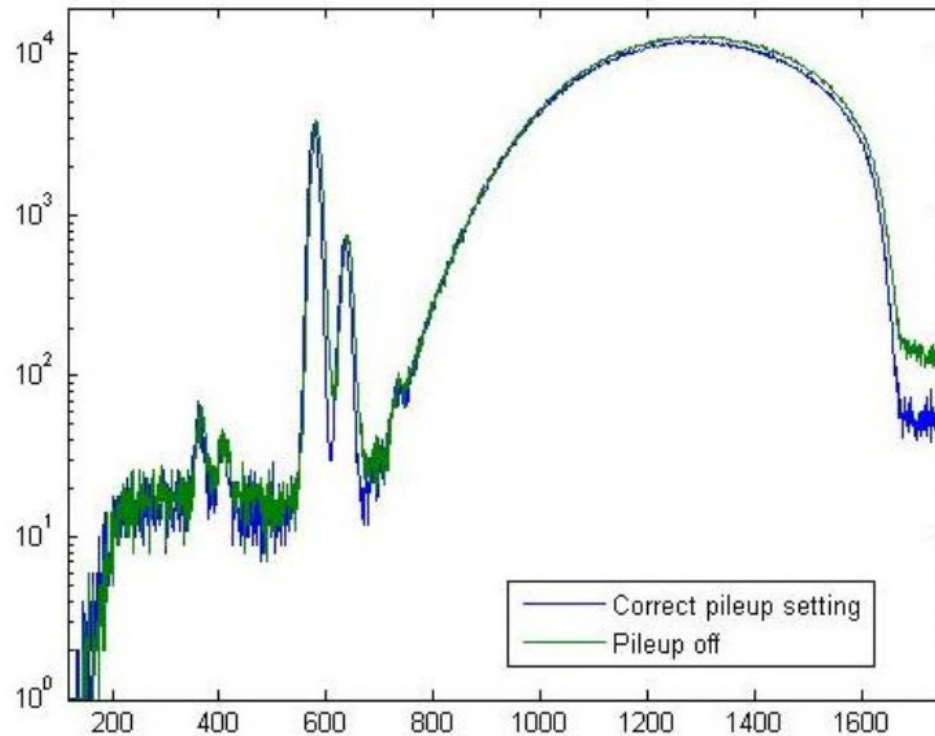


BACKUP SLIDES



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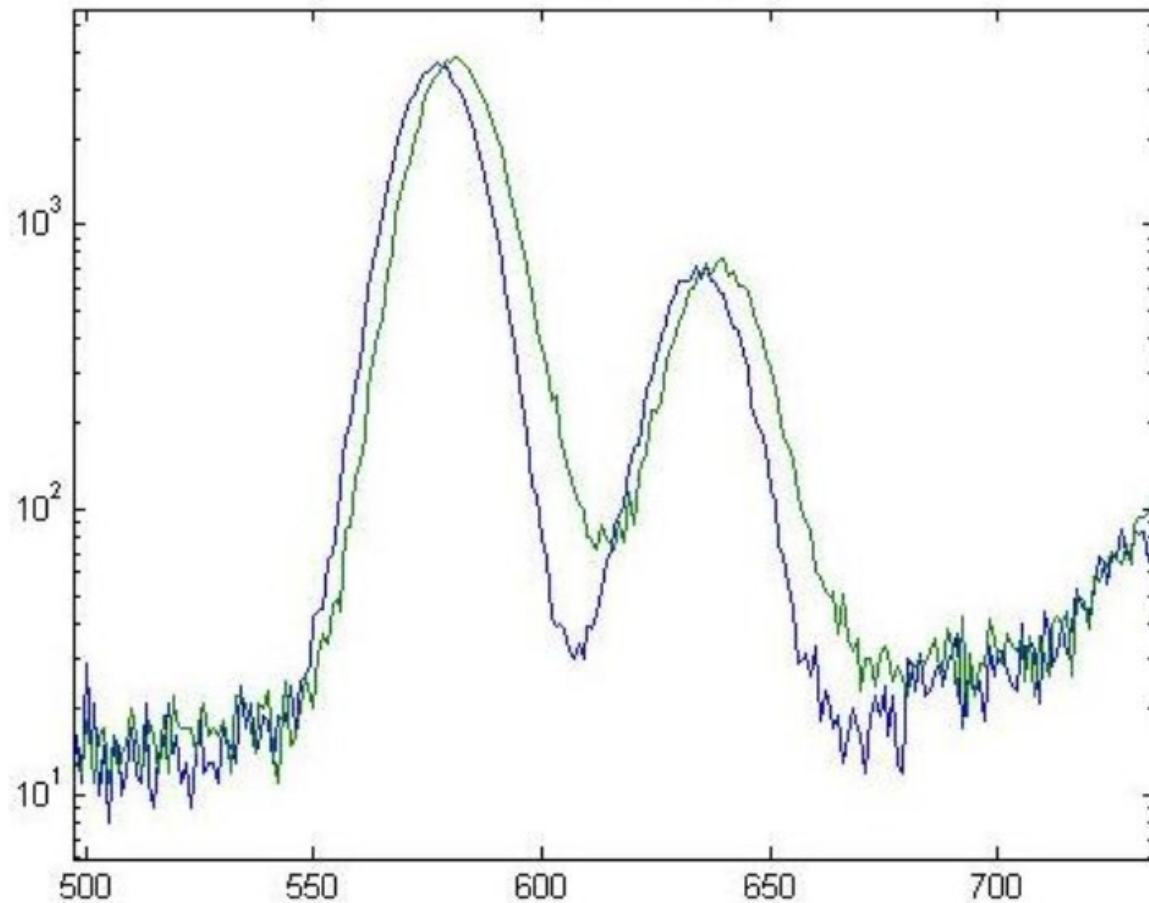
XGlab DANTE DAQ example



This measure has been taken with a Ketek 20mm² detector, a Fe55 source and an X-Ray Tube producing about 2.2 Mcps of ICR. The flattop was 224 ns and the peaking time 32 ns.

from the DANTE manual ...

XGlab DANTE DAQ example



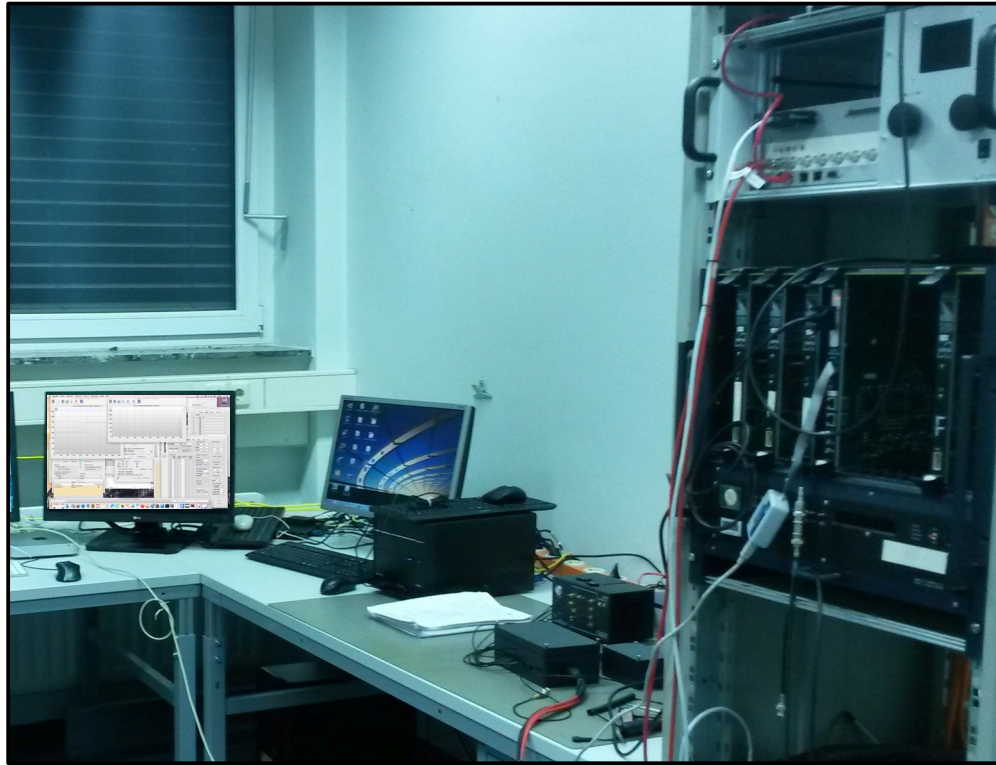
As you can see better from this figure there is an energy shift between the two and it is about 40 eV and also the resolution worsen of about 10 eV.

**from the DANTE manual ...
pileup detection ...**

TRISTAN Test Stand at KIT



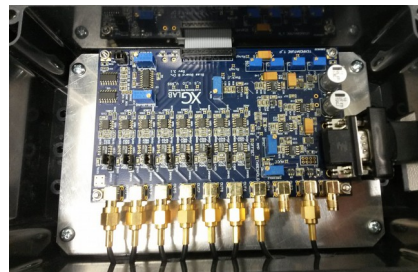
MacMini
ORCA



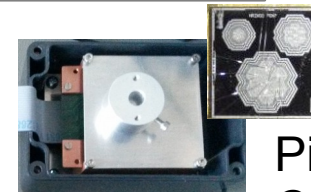
IPE4 Crate



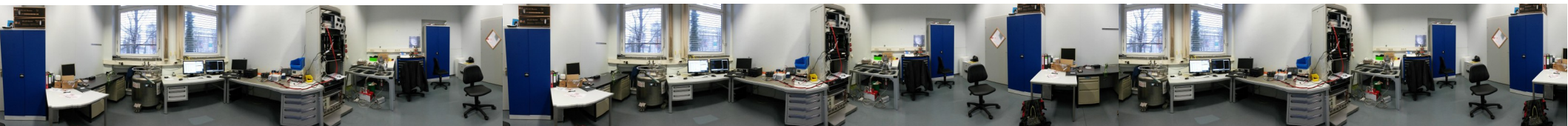
DANTE DAQ



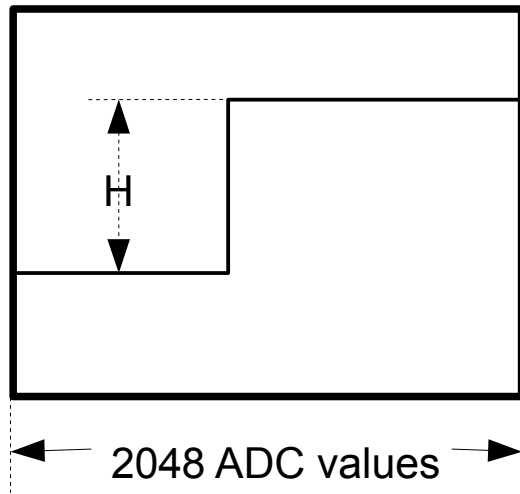
Bias Board



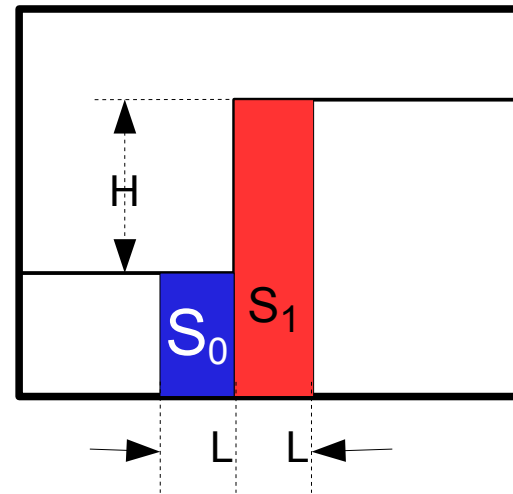
Pixel detector +
CUBE ASIC +
Fe55 source



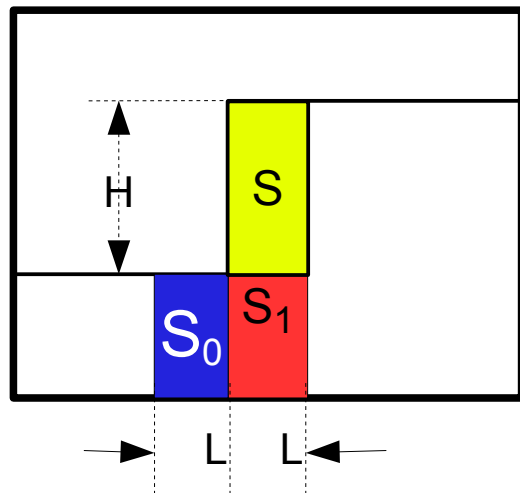
The KATRIN trigger in a nutshell



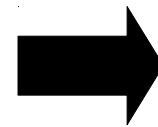
simplified step function with step height H



compute the sums S_0 and S_1



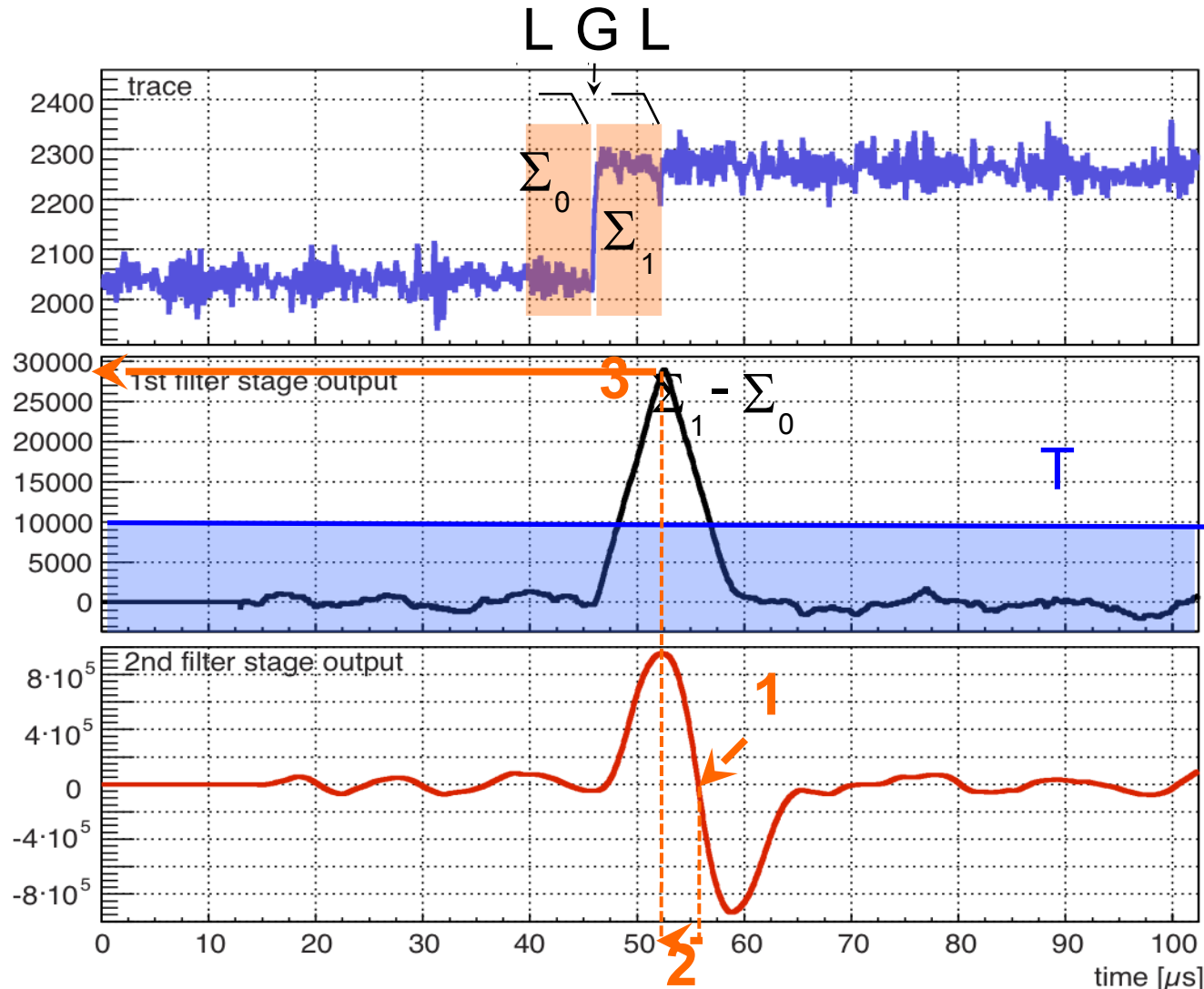
filter energy
 $S := S_1 - S_0$



estimation for step height H
(ADC energy) is
 $H = S/L = (S_1 - S_0)/L$

KATRIN trigger example

(without bipolar extension)



L: shaping length

G: gap length

T: threshold

1 determine zero-crossing

2 go back L/2

3 determine energy