高能同步辐射光源
High Energy Photon Source

HEPS Fast Orbit Feedback system

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CONTENT

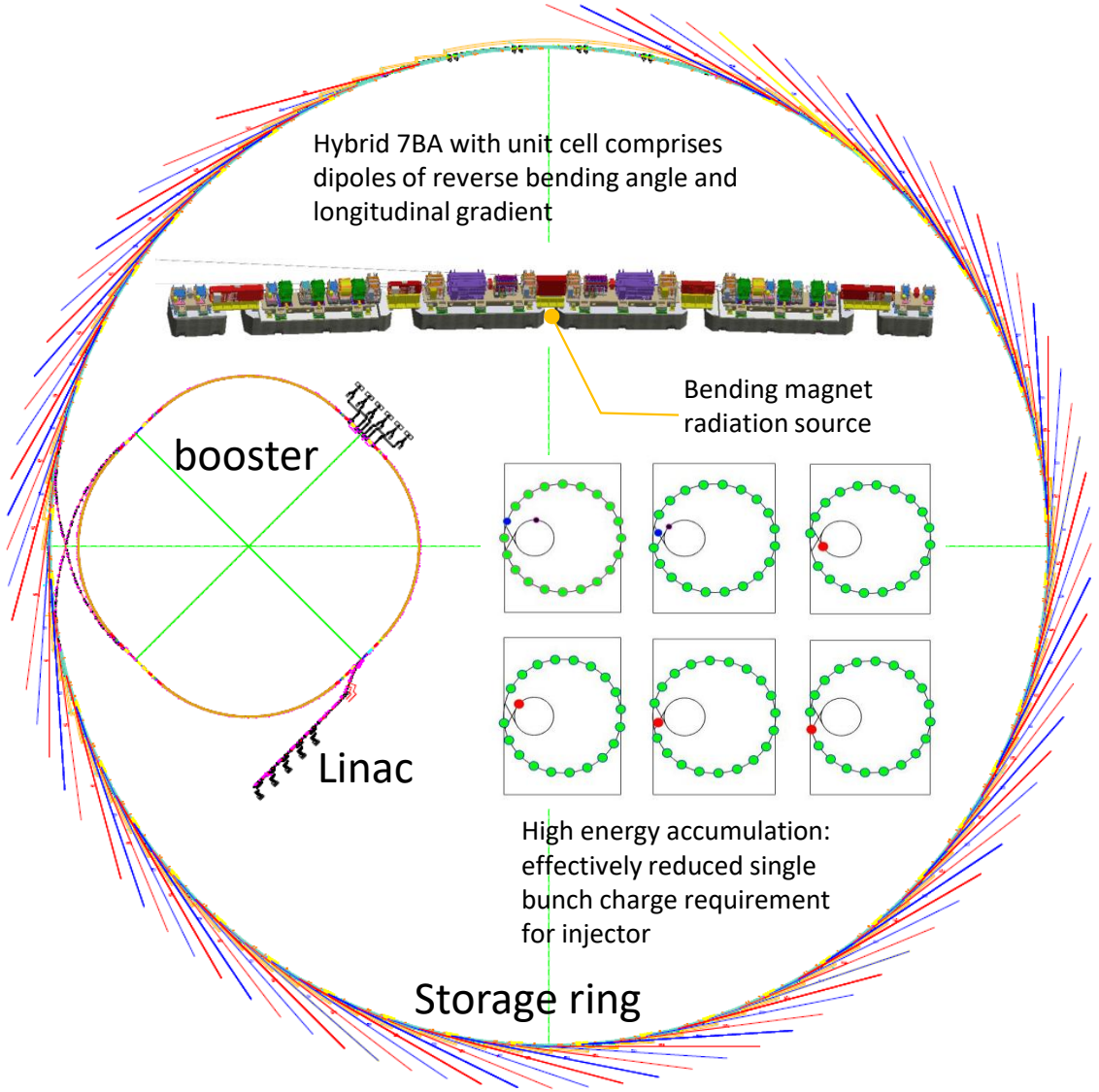
1, Introduction to HEPS

High Energy Photon Source

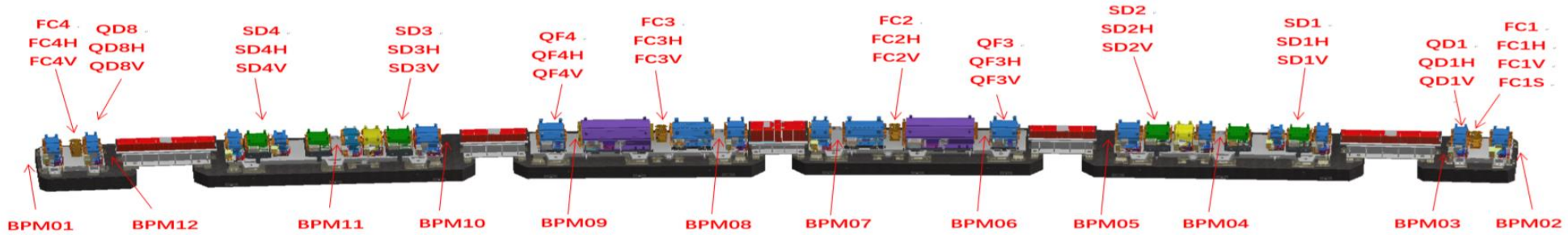
高能同步辐射光源

(HEPS | High Energy Photon Source)

Parameter	Value
Energy	6 GeV
Circumstance	1360.4 m
Emittance	34 pm·rad
Brightness	>1x1022 phs/s/mm^2/mrad^2/0.1%BW
Betatron tune	115.15/104.29
Radiation loss	2.64 MeV
Momentum compaction factor	1.83e-5
Harmonic ratio	3



Orbit stability criteria

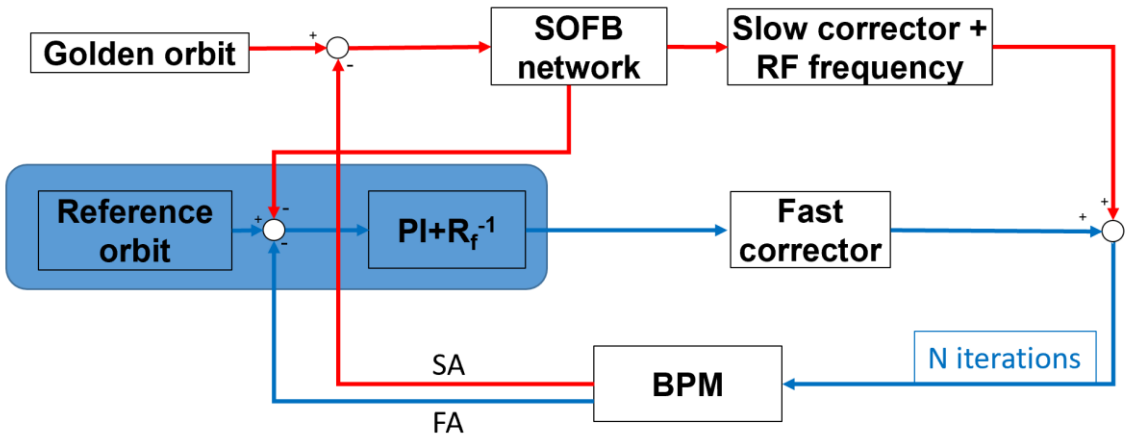


48 7BA cells, 576 BPMs, 192 fast correctors (FC), 288 slow correctors (SC)

HEPS stability requirement	Short time (0.01-1000 Hz)	
	orbit	angular
Horizontal	1.0 μm	0.2 μrad
Vertical	0.3 μm	0.06 μrad

Global orbit feedback scheme

- Strategy: SOFB+FOFB+RFFB
- Commissioning: SOFB+RFFB



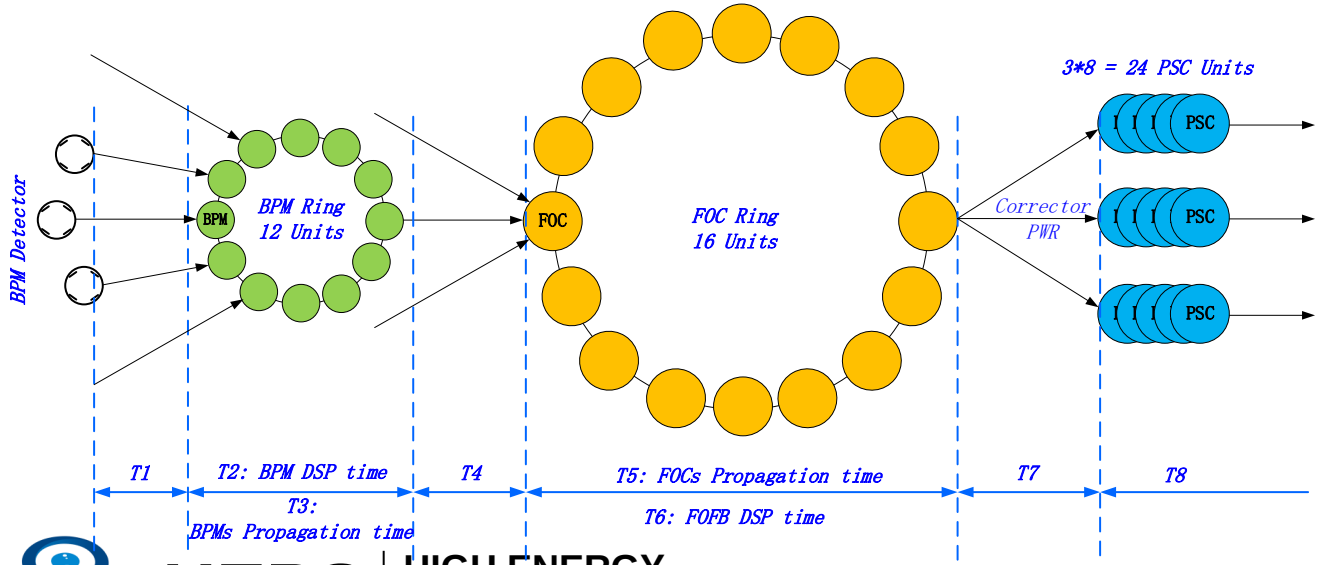
Global orbit feedback

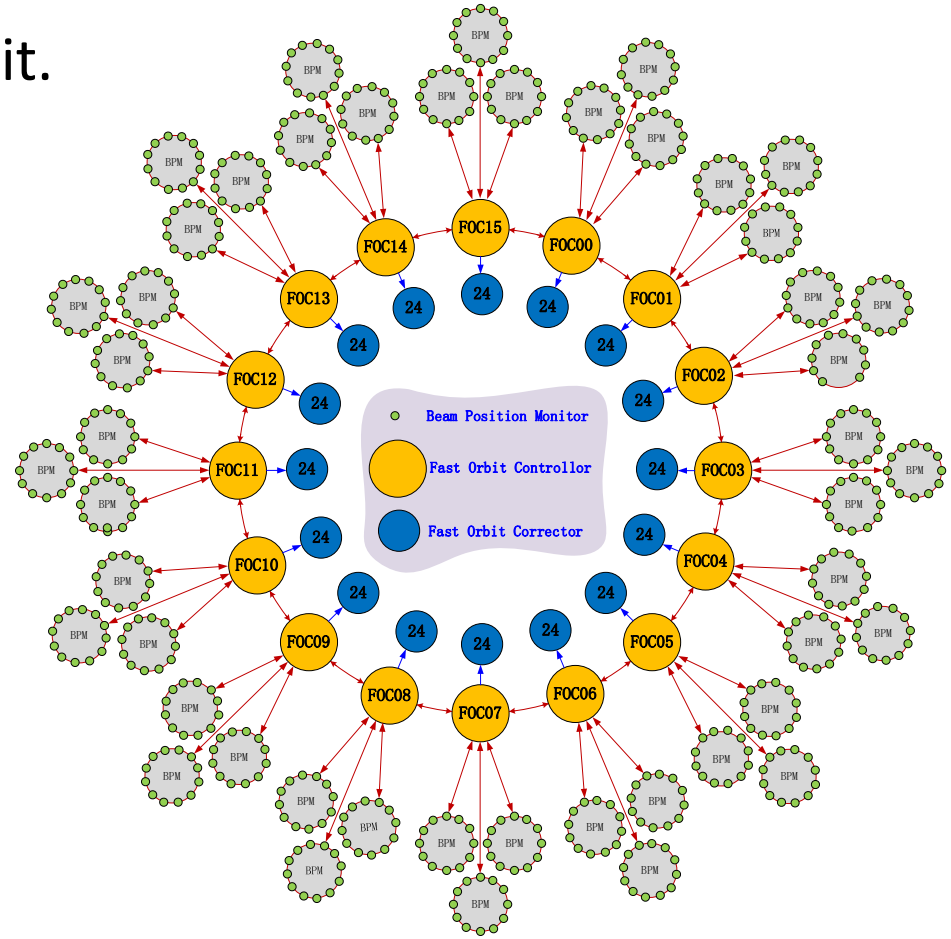
Parameter	Feedback design
Algorithm implementation	Fast + SOFB
BPM sampling rate	22 kHz (FA)
FC sampling rate	22 kHz
Signal processors (16 stations)	FPGA (Virtex-7)
Num. BPMs /plane	576 (12 per cell)
FC /plane	192 (4 per cell)
SC /plane	288 (6 per cell)
FC PS bandwidth	10 kHz
FC latency	< 25 μs
FOFB closed-loop bandwidth	>500 Hz

2, FOFB Architecture of HEPS

FOFB system framework

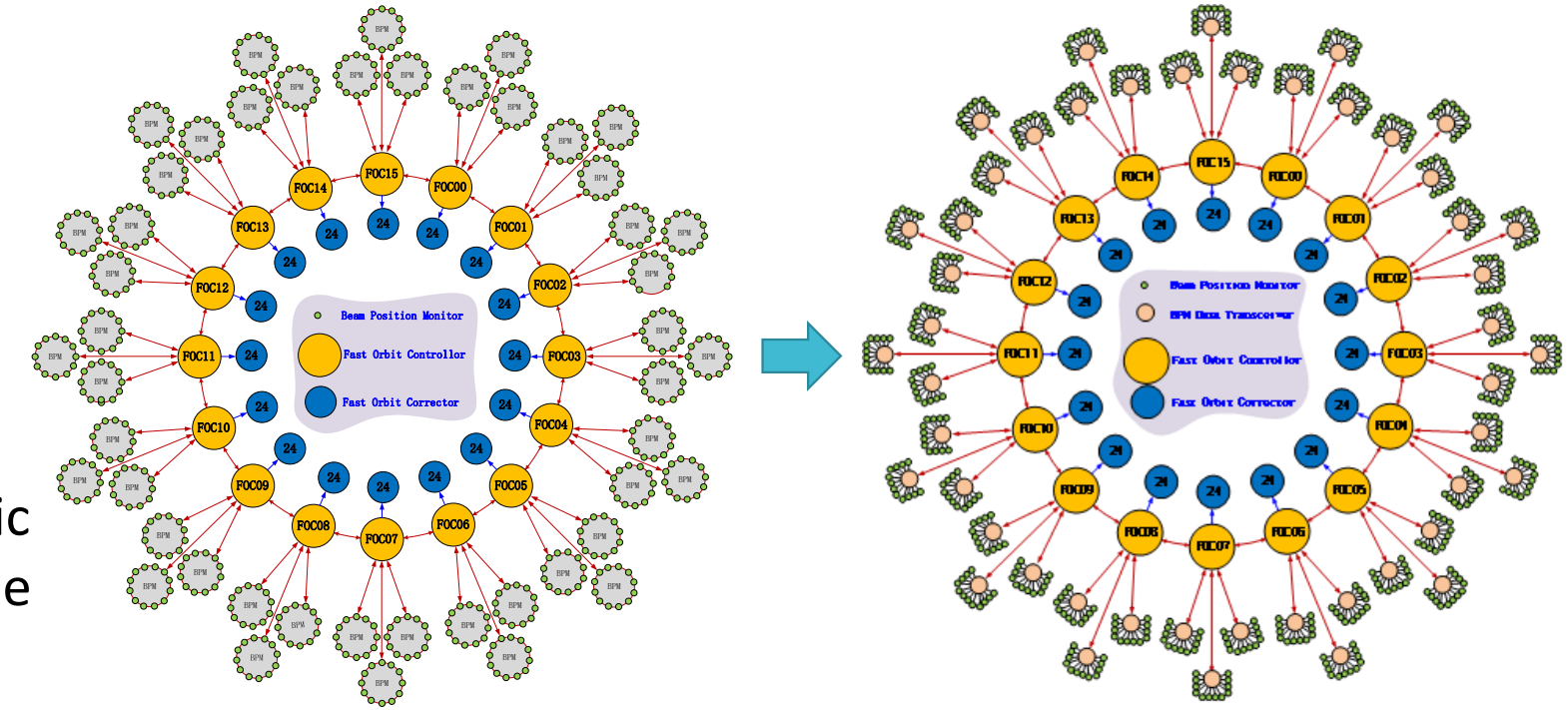
- "Ring-Star-Ring" structure
  - For each BPM station, construct all 12 BPMs to a BPM ring;
  - Connecting adjacent 3 BPM rings to 1 FOFB unit.
  - Link all 16 FOFB units to 1 large FOFB ring.
  - Connecting 1 FOFB unit to 3 FC PSC units.





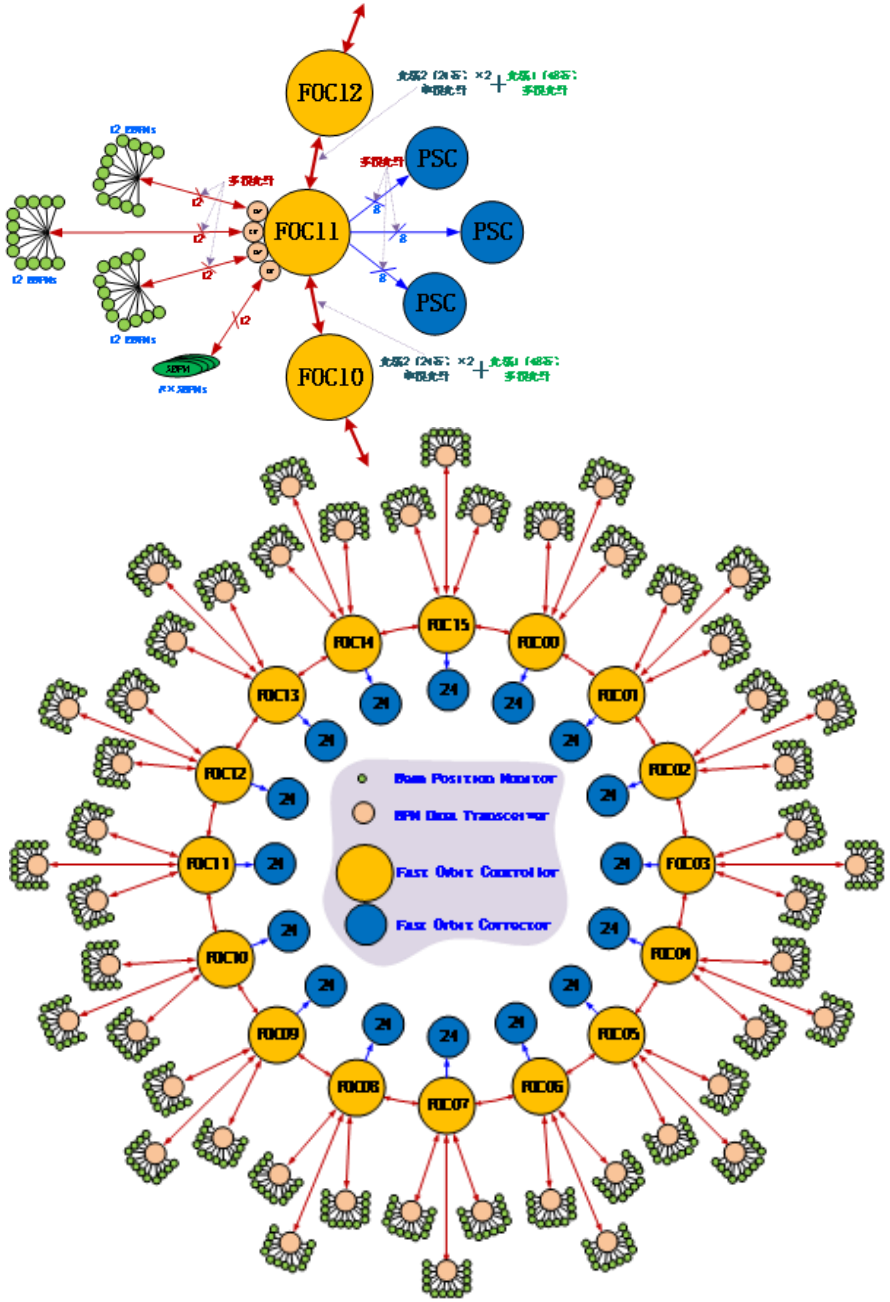
Data Transmission Network

- Our entire system has undergone two iterations of version development.
- In the previous version, the FOFB framework featured a “ring-star-ring” two-layer design. With the latest design, we have incorporated a BDT module and developed a “star-ring” framework.
  - Reduce the latency;
  - Expand the inputs for XBPM;
  - Promote the system stability.
- Note: Changing the data transmission framework only requires changing the fiber optic connection method, without the need to modify the hardware and software of each system.



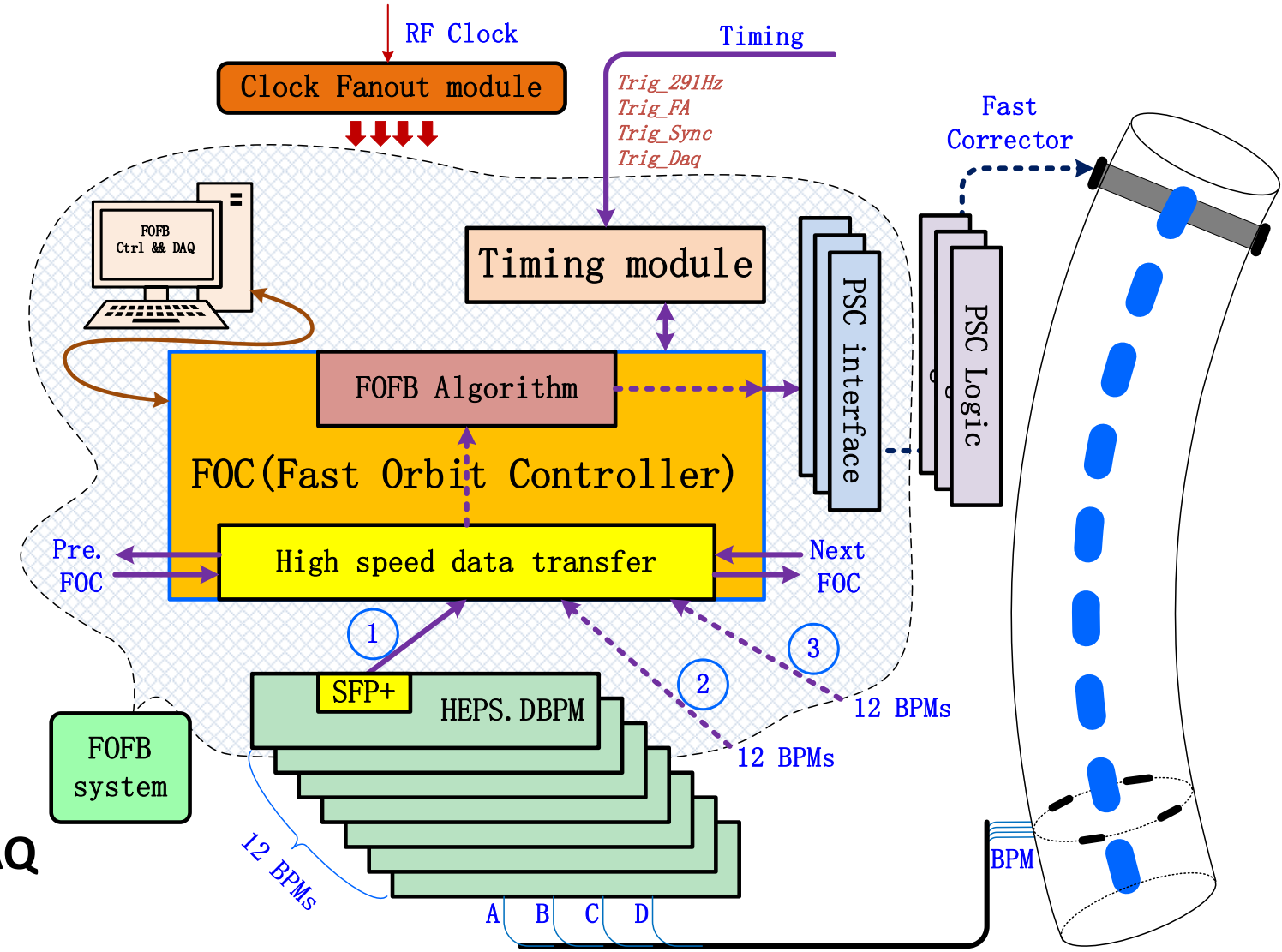
Data Transmission Network

- A “star-ring” data transmission network structure.
  - Added BPM data transceiver (BDT) module for point-to-point reception of all BPM data corresponding to BPM sub stations, and then sent to FOC.
  - The advantages of “star-ring” framework:
    - Reduce the power consumption of FOC;
    - Decrease data transmission latency;
    - Prevent the failure of one BPM from affecting the transmission of data to other BPMs;
    - It make XBPM input possible.

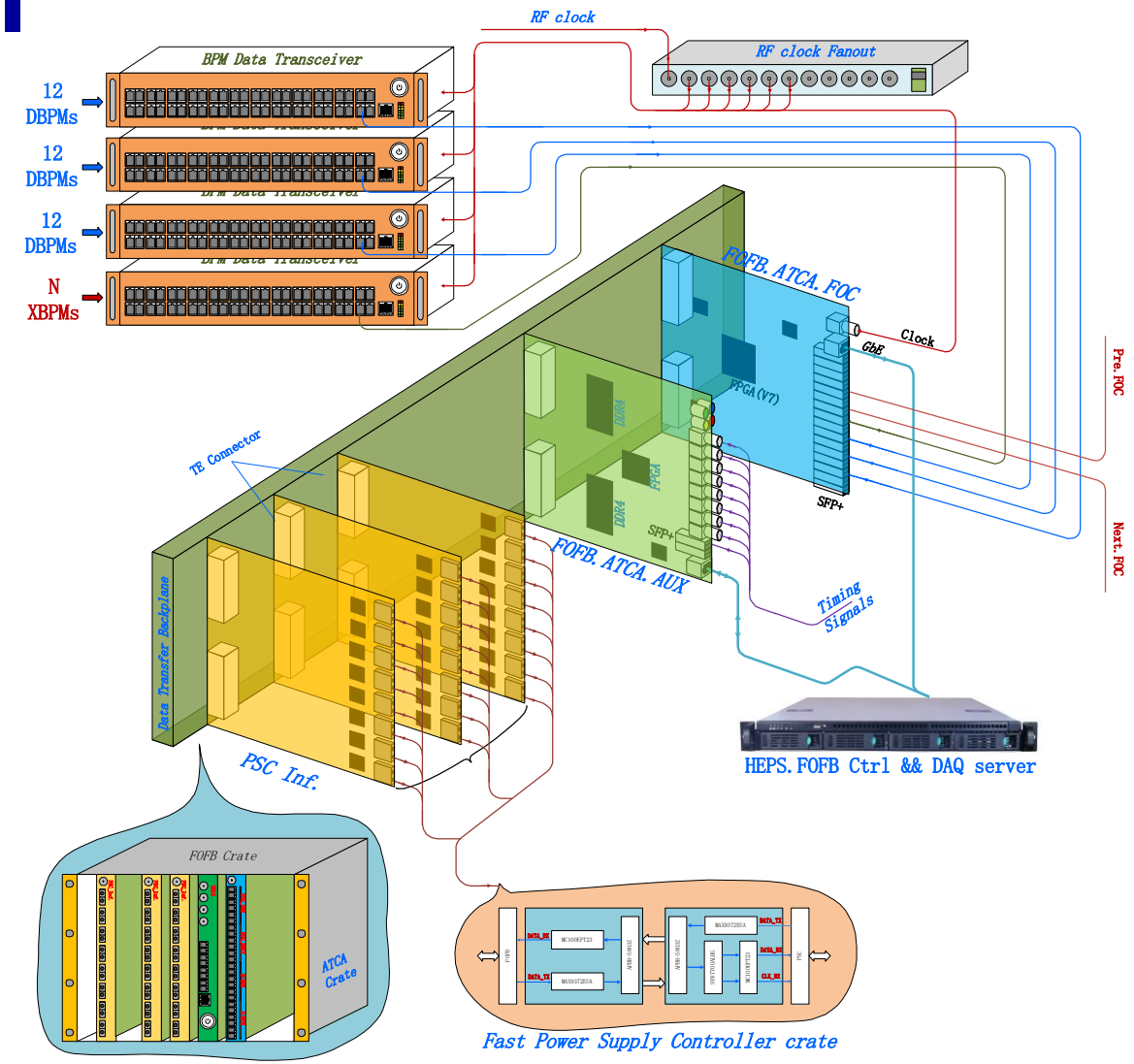


FOFB system Hardware Unit

- **FOFB Unit Function block**
  - 3*12 BPMs
  - 3*8 PSCs
  - 1 FOC
  - 4 Timing signals
    - Trig_291Hz
    - Trig_FA
    - Trig_Sync
    - Trig_DAQ
  - 1 Clock Fanout module
  - FOFB Server for Control and DAQ



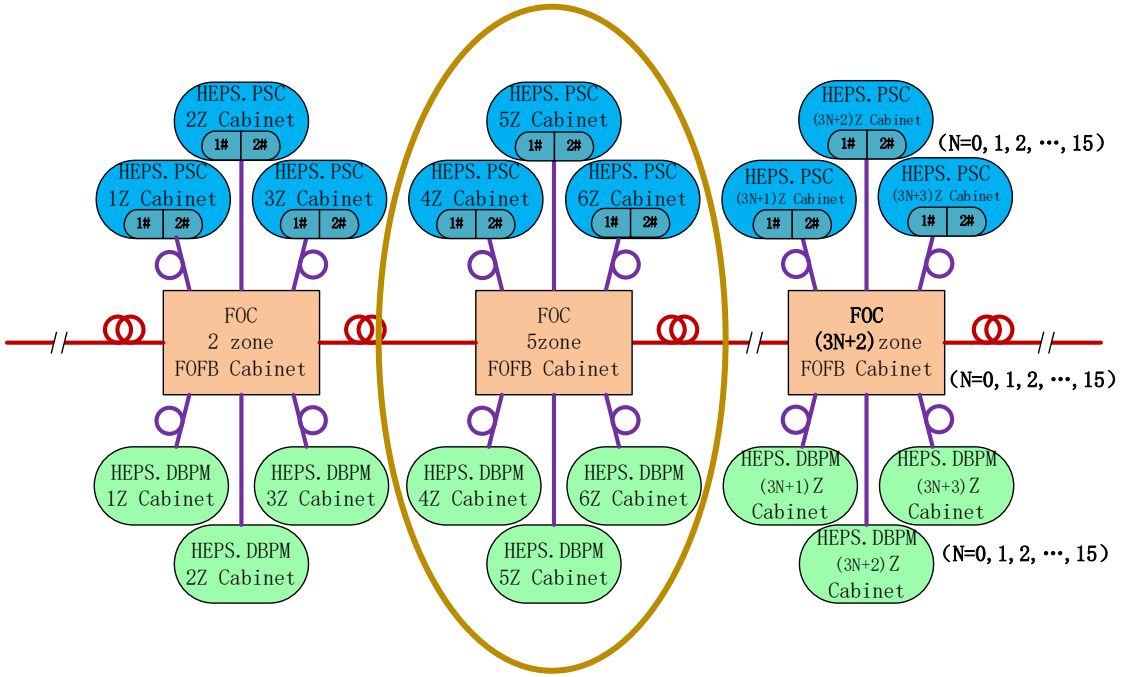
FOFB system Hardware Unit

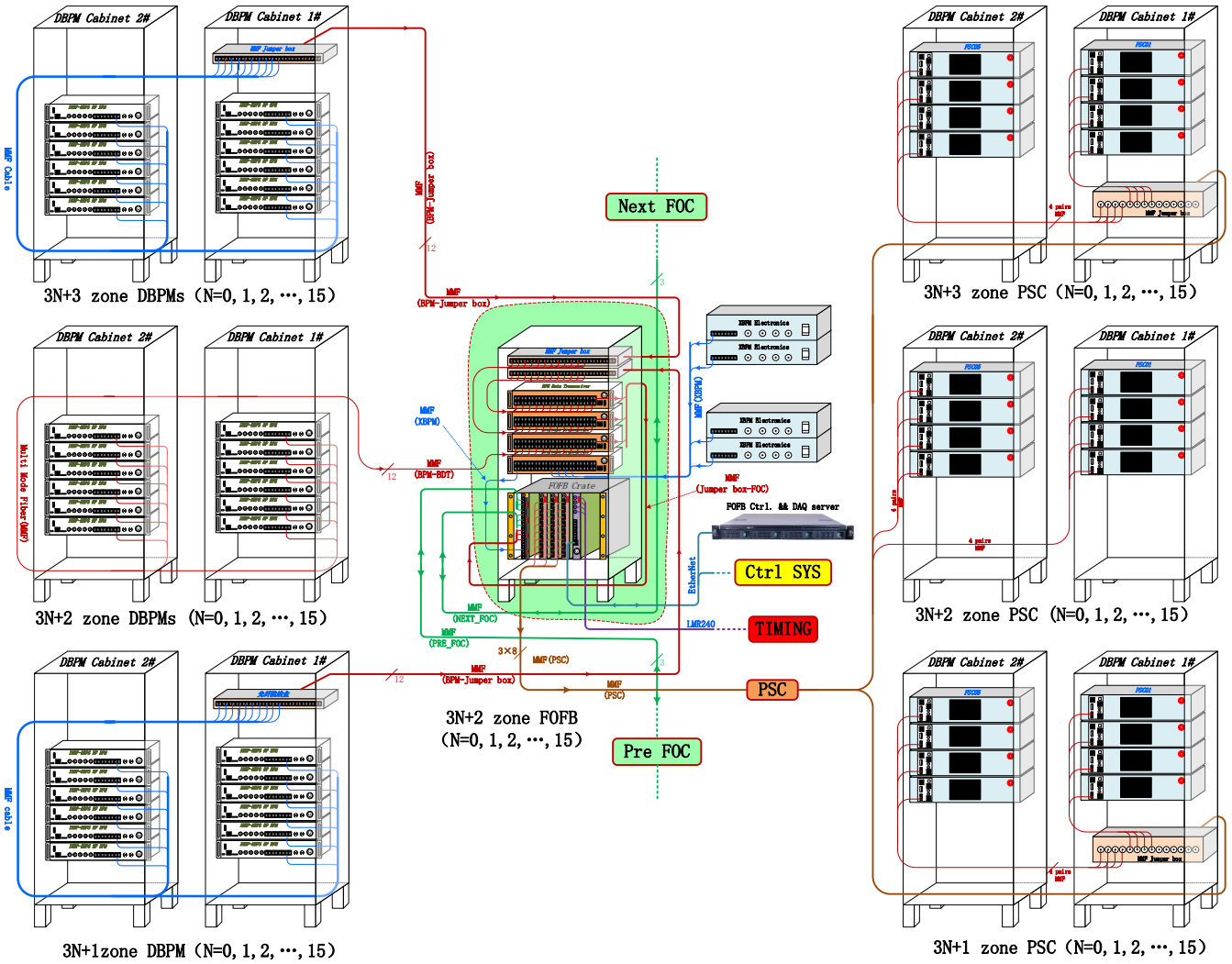


- FOFB Unit Components
  - FOFB.ATCA.BackPlane
  - FOFB.ATCA.FOC
  - FOFB.ATCA.AUX
  - FOFB.ATCA.PSC_Interface
  - FOFB Server for control and DAQ Op.
  - RF clock Fanout module
  - BPM data Transfer module
    - Used for BPMs data reassemble and forward function.

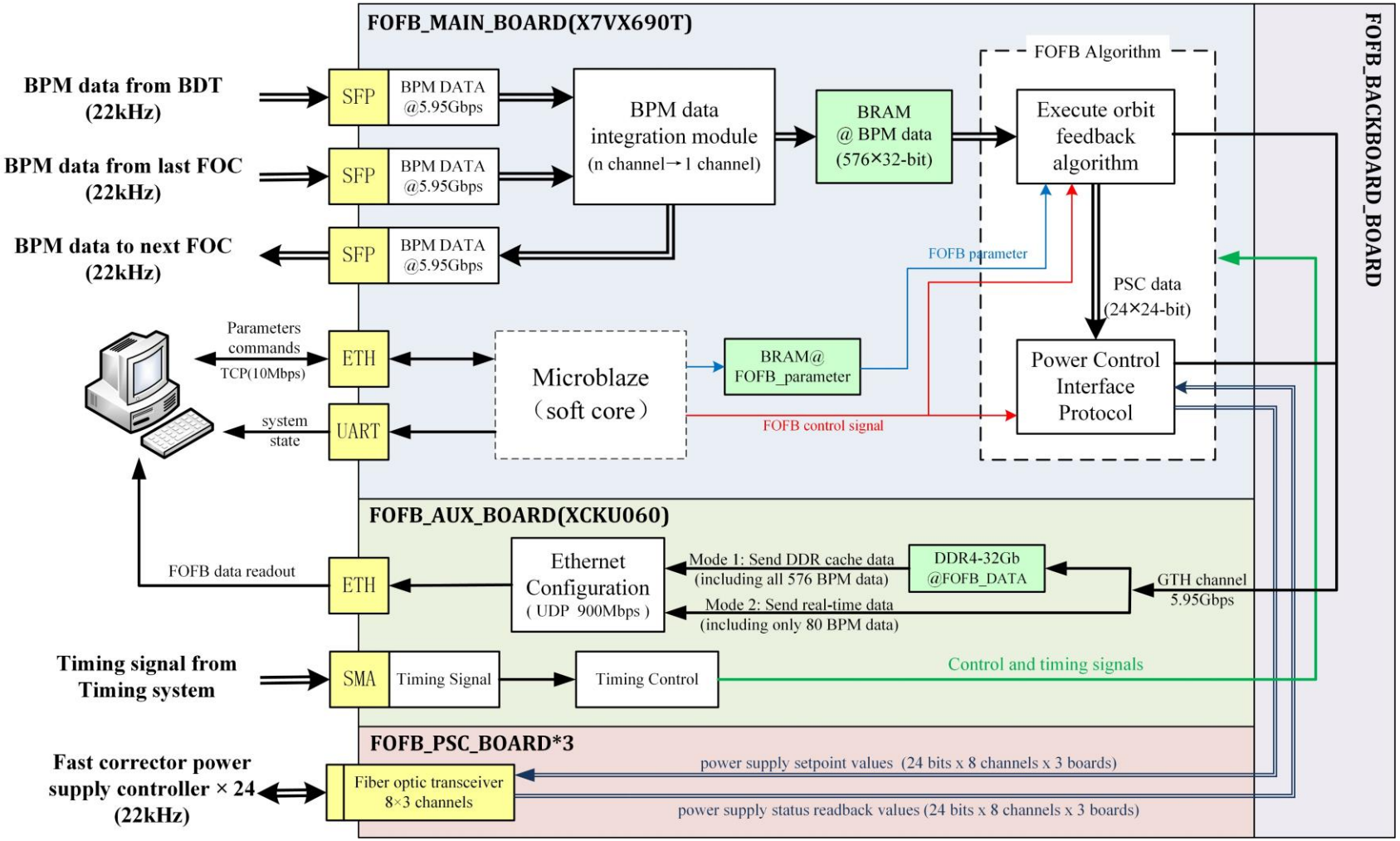
FOFB system Hardware Unit

- All components and Signal connections in 1 FOFB unit





FOFB system data processing flow



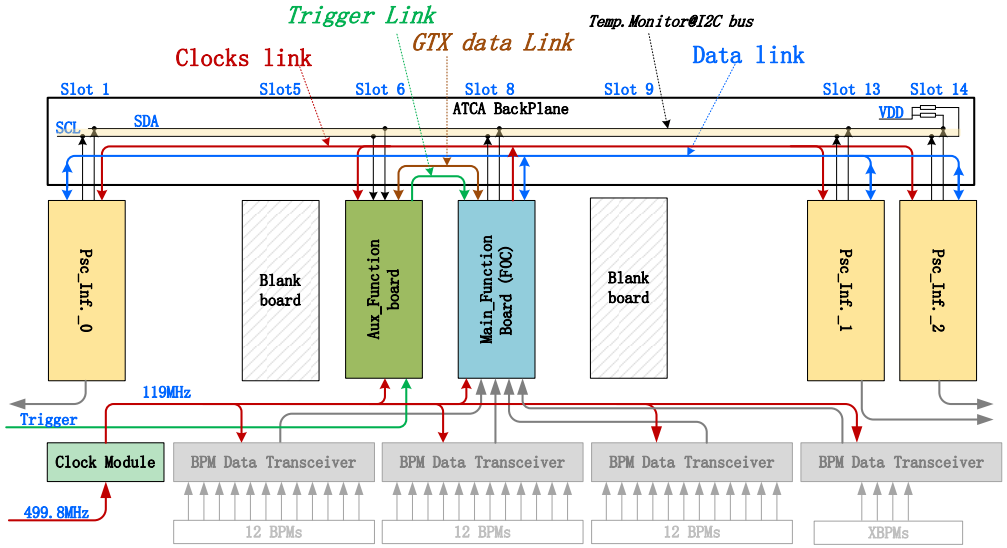
3, FOFB Hardware development

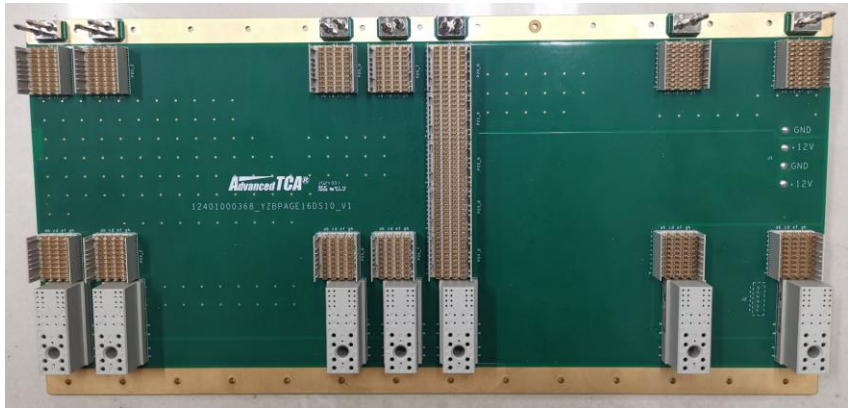
FOFB Hardware development(main parts)

- FOFB.ATCA.Backplane
  - Provide power supply for all FOFB ATCA function modules, and provide the signal interconnection between the ATCA function modules
- FOFB.ATCA.FOC
  - Receiving and Processing the BPMs data, perform the FOFB algorithm and output the PSC correction data
- FOFB.ATCA.AUX
  - Auxiliary function module, processing the Trigger signals, temperature monitor and FOFB system protection, moreover, to perform the data acquisition operation.
- FOFB.ATCA.PSC_Inf.
  - Receive the PSC correction data from FOC module, and forward the information to PSC module, furthermore, read the PSC setting information back to FOFB.

FOFB.ATCA.Backplane design

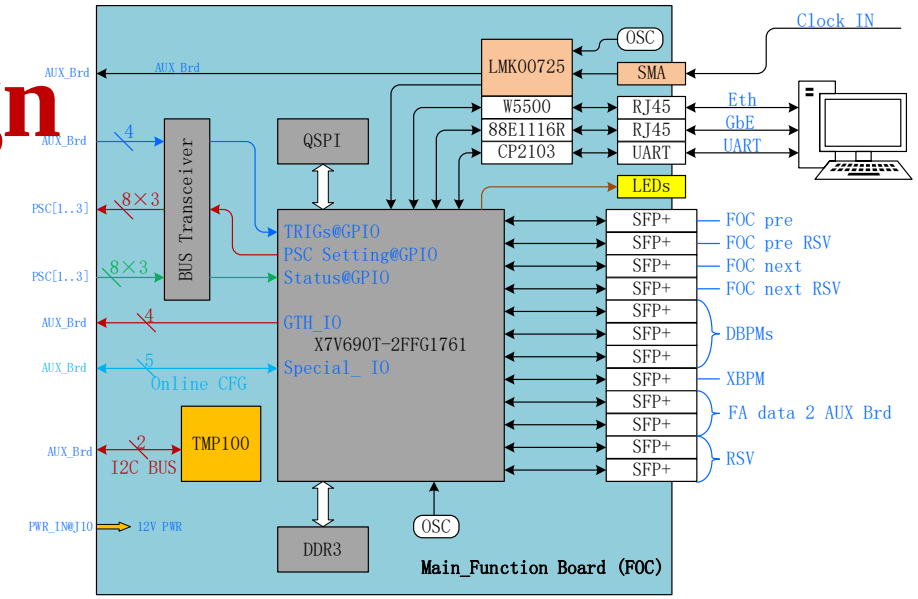
- Signal interconnection scheme
- Key features
  - Power supply for all function module
  - Clock link from FOC to other module
  - Trigger link from AUX to FOC
  - Data link between FOC and PSC
  - I2C bus for Temp. Monitor
  - GTX link between AUX and FOC
- Physical picture of the backplane

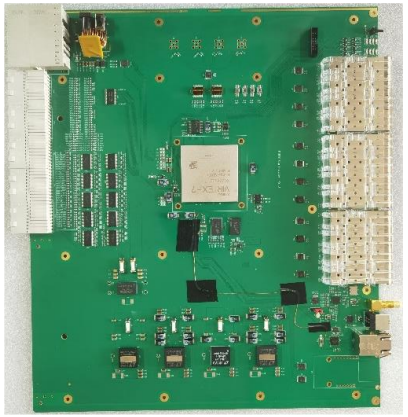




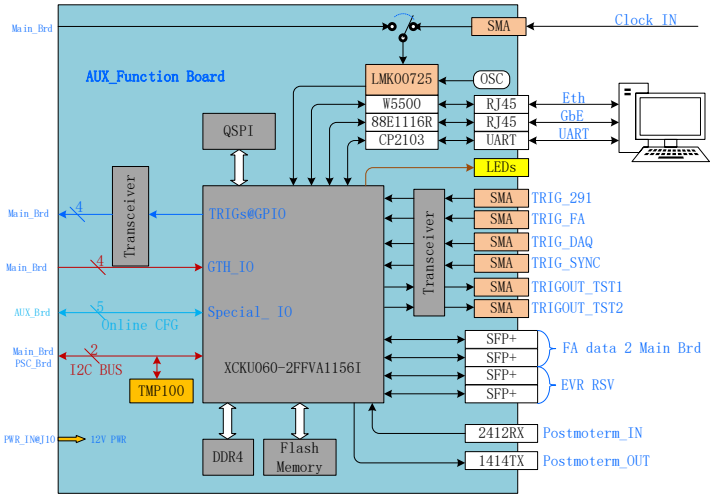
FOFB.ATCA.FOC module design

- FOFB FOC function block
- FOC Key Features
  - Parameters setting by the FOFB Server's program
  - Receive 36 BPM.FA data from adjacent 3 DBPM cabinets
  - Communicate and exchange data with adjacent FOC units
  - Processing the BPMs data and obtaining the fast corrector information through the FOFB algorithm
  - Send fast corrector information to the fast PSC through the PSC interface module.
  - Send BPMs and other data from this station to the AUX board via the GTX high-speed data link.
  - Receive the Trigger information from AUX module, which is used for FOFB data processing.
  - Logic to monitor the FOC's temperature, and send those information to AUX.
- Physical picture of the FOC module

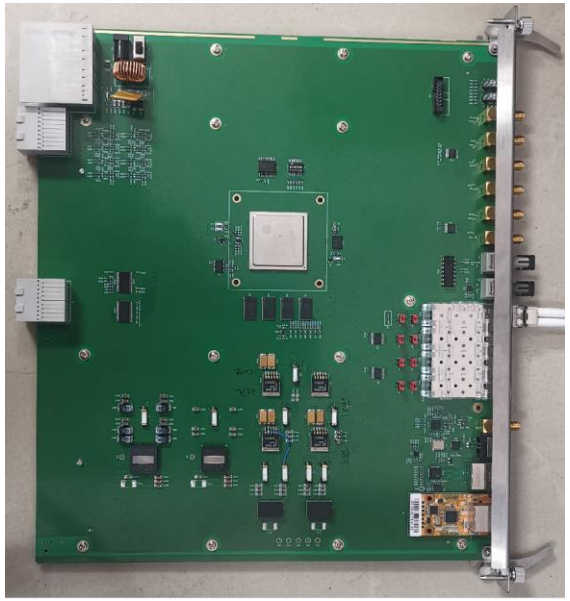




FOFB.ATCA.AUX module design

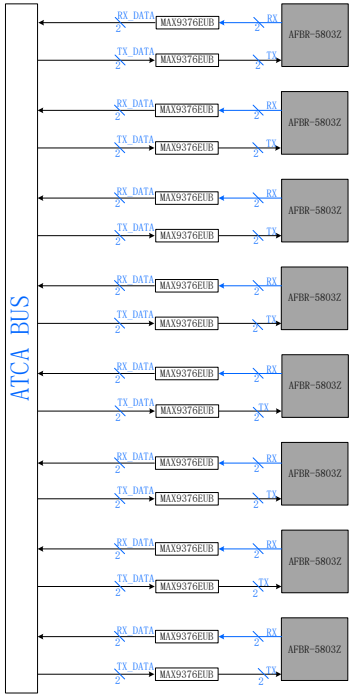


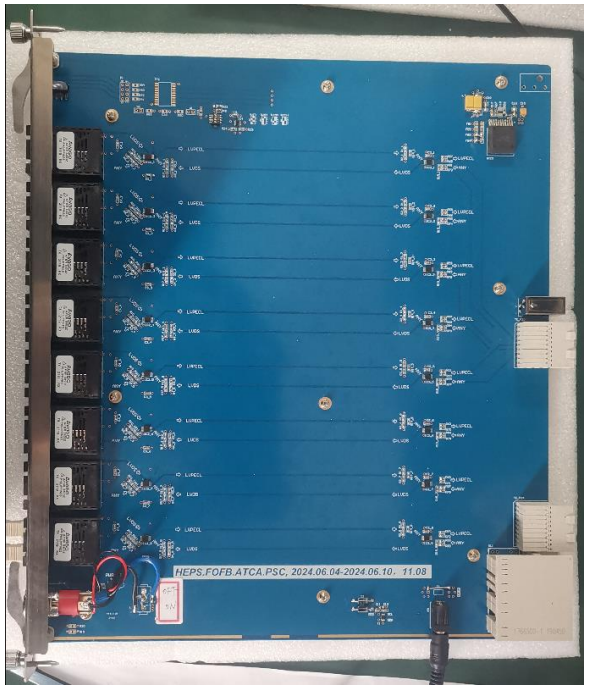
- FOFB AUX function block
- Key features
  - Receiving Trigger signals from Timing system and forwarding those signals to FOC.
  - Receiving local BPM data, PSC data, and other configuration information from the FOC , then storing all those data to the server via GbE.
  - Receiving temperature information from other modules, and sending it to the server program to monitor the FOFB system temperature, to shut off the FOFB system power supply in emergency situations.
- Physical picture of the AUX module



FOFB.ATCA.PSC_Interface module design

- Function block
- Key features
  - Receive the fast corrector information from FOC module, and send it the fast PSC with multimode fiber.
  - Read back the fast corrector information and other configuration information from PSC and send it to FOC
  - Temperature monitor, the temperature information is send to AUX module for the FOFB system protection.
  - Working Status disp.
- Picture of the PSC_inf.

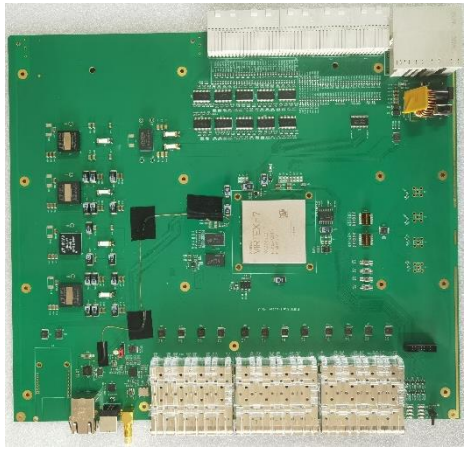




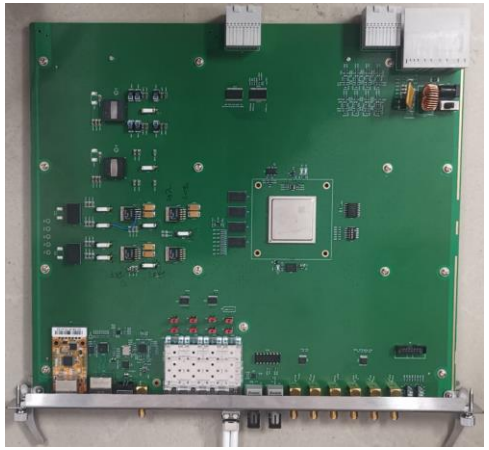
Hardware implementation

- At present, all FOFB system modules have been produced and tested.
- Based on the existing hardware, the FOFB system can be deployed on HEPS to conduct the basic functional testing.

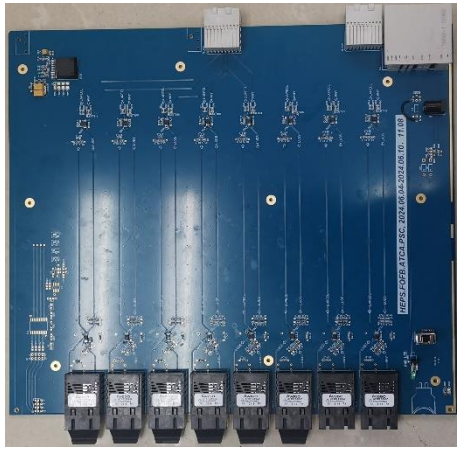
ATCA crate



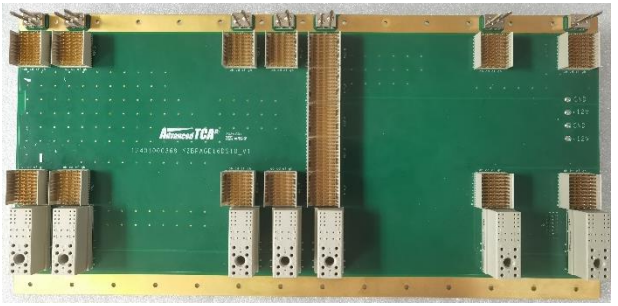
MAIN board



AUX board



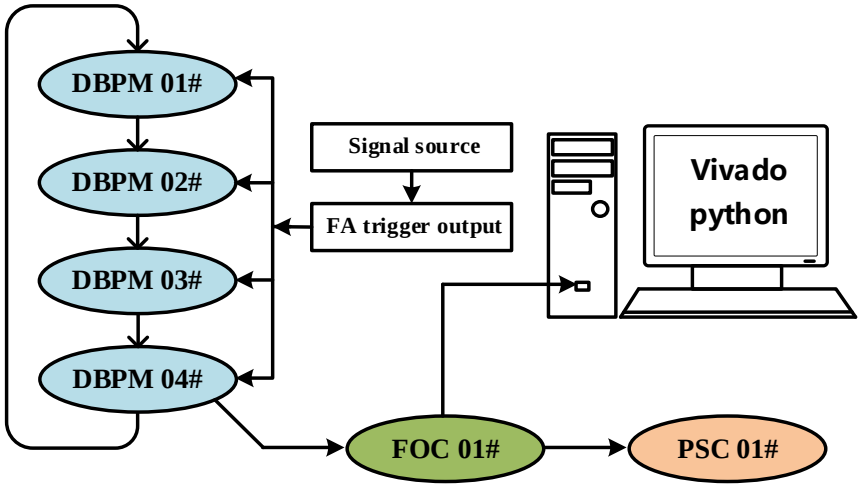
PSC board



Backboard

4, FOFB system laboratory testing

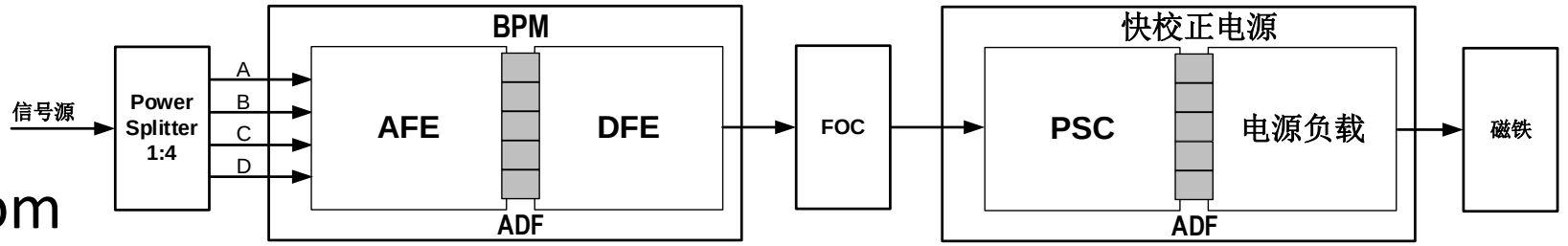
Laboratory testing platform

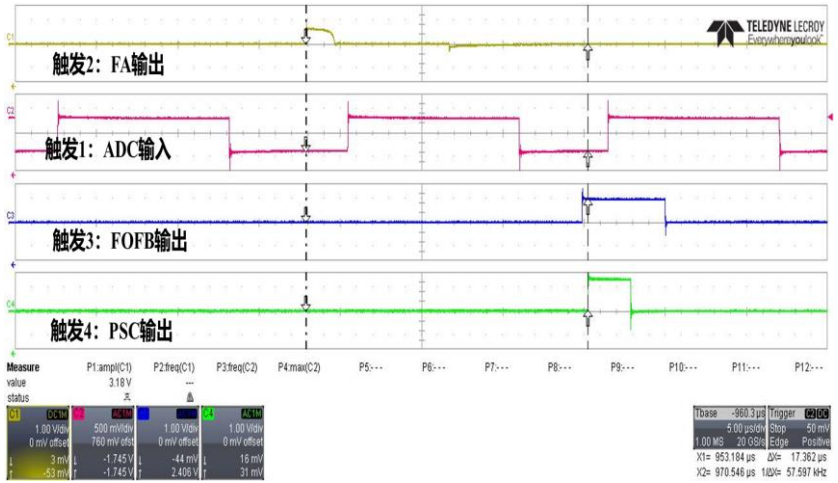


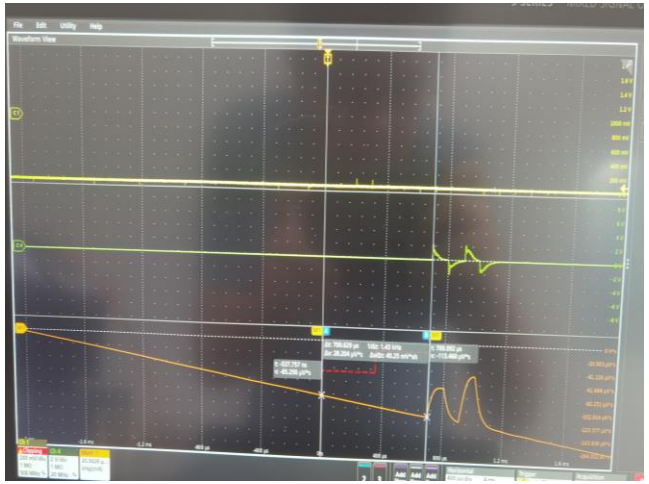
- Four BPM, one FOC and one PSC were used to build a test platform in the laboratory to test the basic functions and evaluate the performance of the system.
- BPM data communication test: The delay of 50 meter fiber optic transmission is about 0.65μs, and the total delay of data transmission is estimated to be about 0.5μs.
- Power controller interface testing: calibration value sending test, read back data receiving, power on/off control, etc.
- FOFB Algorithm Simulation: Calculate PS setpoints using test data in both FOC and the upper computer's Matlab, and cross-check for verification.
- Data Readout Function Test: Real-time reading of FOFB system data at 300Mbps rate by receiving UDP data packets through Python on PC.

Multi-system joint test in laboratory

- Test platform include BPM, FOFB, PSC, and Magnets.
- Function test: the signal from BPM to FOFB, and to PSC, at last, to Magnets. The system have a fixed latency .



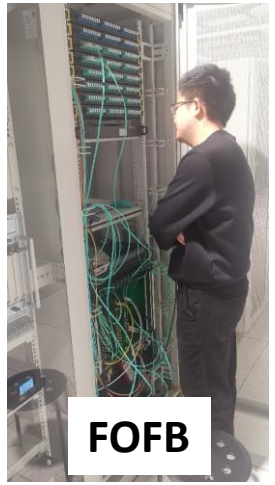


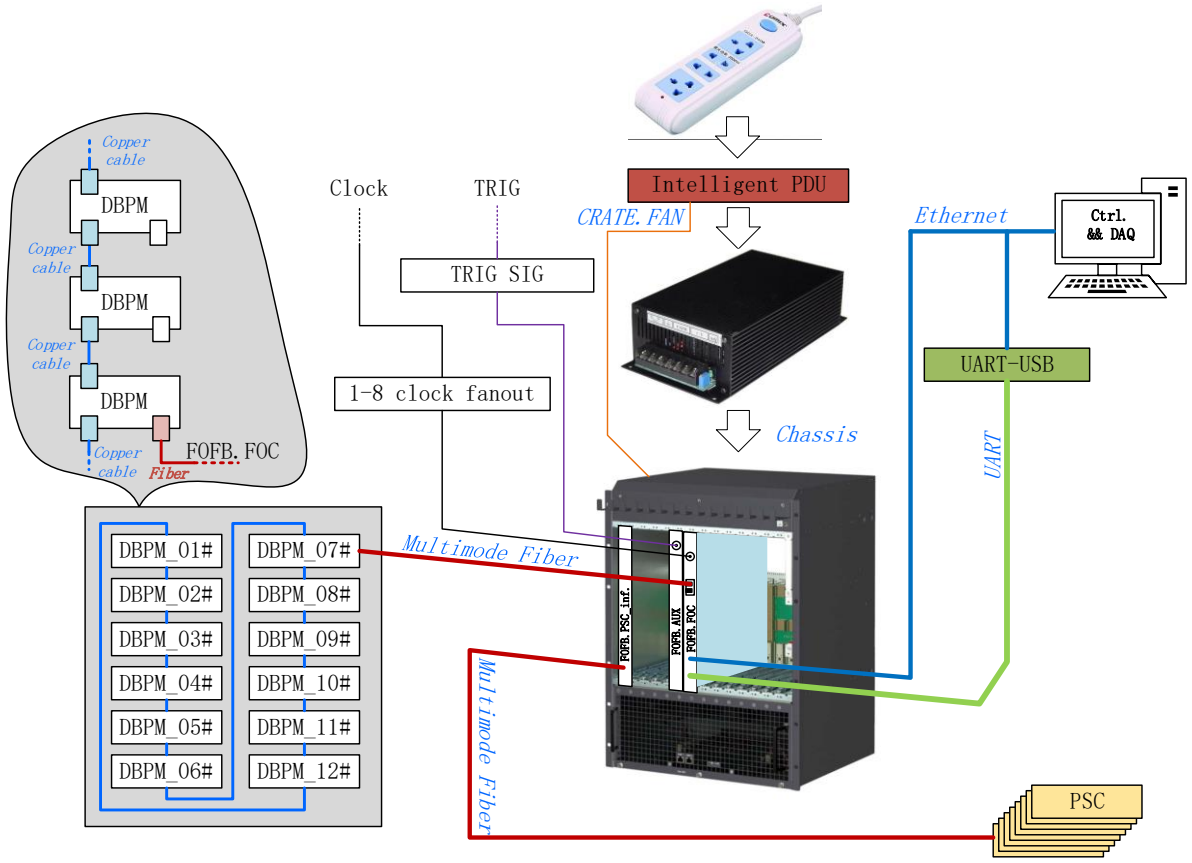


5, FOFB On-site testing without Beam

On site testing platform construction

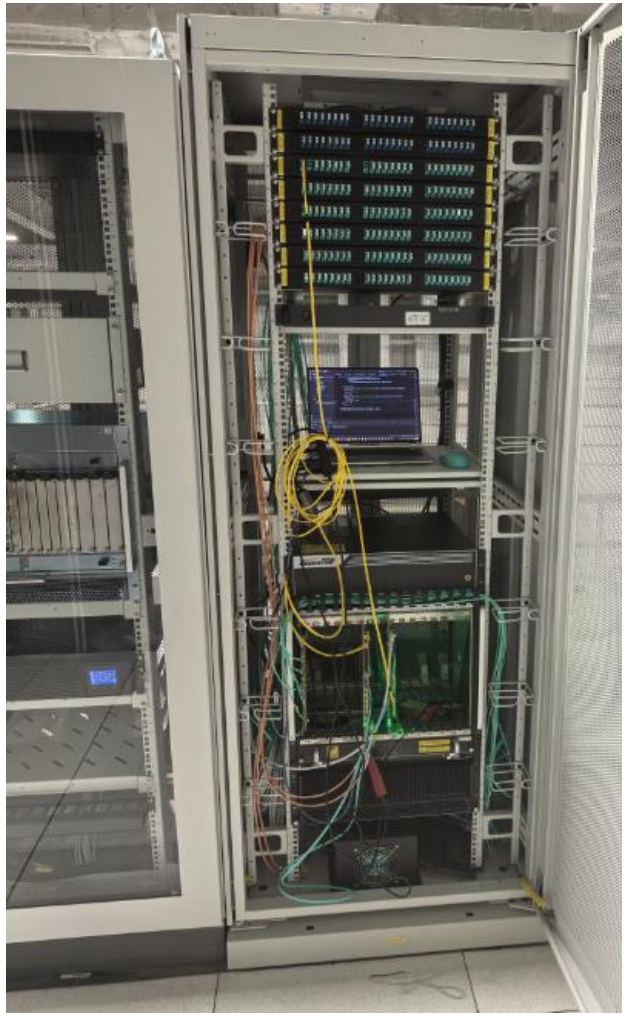
- Testing platform components
  - BPMs: 36BPMs at Zone13, Zone14 and Zone15
  - FOFB Unit: located at Zone 14
  - PSC: 24 PSCs at Zone13, Zone14 and Zone15





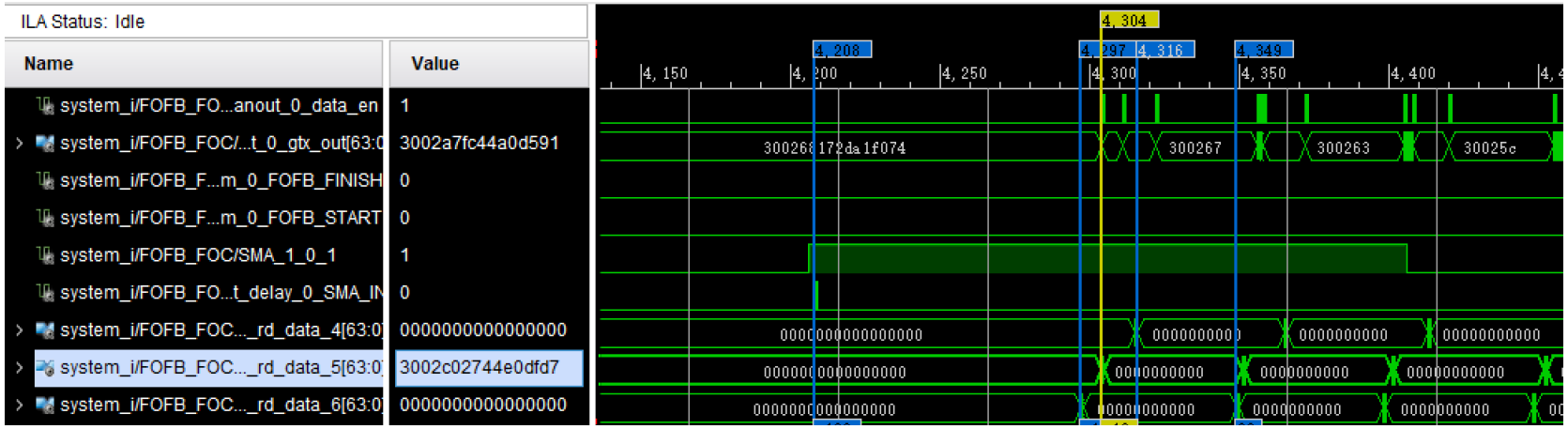
On site testing: FOC self testing

- FOFB components in zone 14
  - FOFB.ATCA.FOC / FOFB.ATCA.AUX / FOFB.ATCA.PSC_Inf.
  - Clock Fanout logic / Trigger Input
  - Intelligent PDU with Remote Control Capabilities
- FOC self testing result:
  - Intelligent PDU Switch ON/OFF with the control program. (OK)
  - FOFB.ATCA.FOC and FOFB.ATCA.AUX program loading. (OK)
  - The server program controls FOFB through the GbE.(OK)
  - Testing program running in FOC is ready



On site testing: DPBMs-FOFB

- Testing the data link from Zone 13 DBPMs to Zone 14 FOC.
  - The following tasks must be ready before the data link testing
    - Related parameter loading is ready, which include: KX,KY / KA,KB,KC,KD/ offset / BPM physical Number / ……
    - DBPM FA data should be synchronized : FA data output from the BPM ring must be synchronized with the FA timing signal(TRIG_FA)



On site testing: FOFB-PSC

- Testing contents include:
  - Corrector value setting and Data frame checking
    - 24-bit data, with 1 bit for the sign, 4 bits for the integer, and 19 bits for the decimal bit, which corresponds to the current setting with a range of ±16A. The current setting resolution is 1.9075 μA.
  - Related parameters readback(all readback data frame is 24bit)

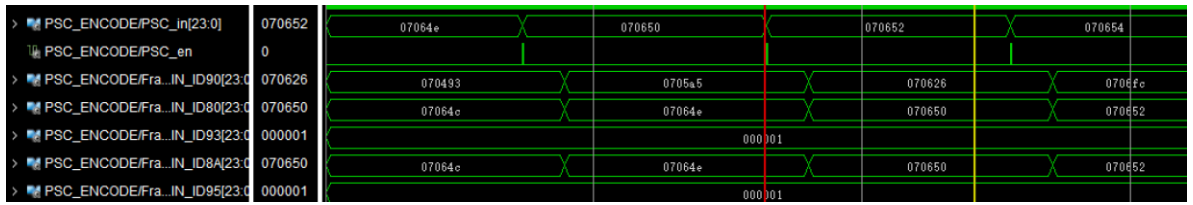
Start(1)	ID(8)	Data(24)	CRC(8)	Stop(2)

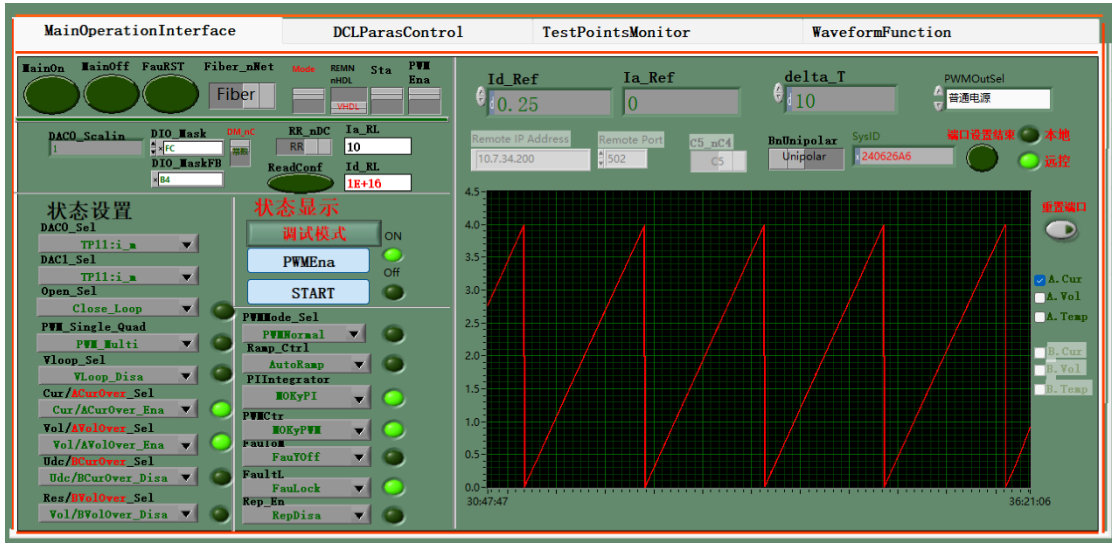
- Start bit: 1 bit, with a constant value: "0";
- ID Number: 8bits, shows the data frame type;
- Setting Value: 24bits, 1-bit sign, 4-bits integers, 19-bits decimals;
- CRC: 8bit，CRC check polynomial: $x^8+x^7+x^5+x^4+x+1$，start and stop bit is not included;
- Stop bit: 2-bits, with a constant value: "11".

			Frame Response from FOFB_PSI				
Protocol	Frame	Delay	Frame1	Frame2	Frame3	Frame4	Frame5
Set setpoint Read status & readbacks& Read setvalue	ID=0x15 Data=Setpoint	4.3us	Same as Received Frame	ID=0x93 Data=Status	ID=0x90 Data= currentback	ID=0x95 Data=Command	ID=0x8a Data= setpointback
Set command Read status & readbacks& Read setvalue	ID=0x0A Data=Command	4.3us	Same as Received Frame	ID=0x93 Data=Status	ID=0x90 Data= currentback	ID=0x95 Data=Command	ID=0x8a Data= setpointback
Read status & readbacks& Read setvalue	ID=0x40 Data=Not used	4.3us	Same as Received Frame	ID=0x93 Data=Status	ID=0x90 Data= currentback	ID=0x95 Data=Command	ID=0x8a Data= setpointback
Set setpoint only	ID=0x55 Data=Setpoint	0us	Same as Received Frame				
Send command only	ID=0x4A Data=Command	0us	Same as Received Frame				
Read setpoint & command	ID=0x00 Data=Not used	2.6us	Same as Received Frame	ID=0x95 Data=Command	ID=0x8a Data= setpointback		
Read Configuration	ID=0x01 Data=Not used	2.6us	Same as Received Frame	ID=0x96 Data={version, 32'b0}	ID=0x8B Data={27'b0, fiber_good, SW1 status}}		
Reserved	ID=0x02 Data= Not Used	0us	Same as Received Frame				

On site testing: FOFB-PSC

- Testing results
  - The PSC module power on/off is controlled by the network, and the function of fiber optic control for power on/off has been removed.
  - The FOFB receives normal read back data, and there are no errors in data communication during short-term testing. the power supply current setpoint can correspond to the setpoint value.

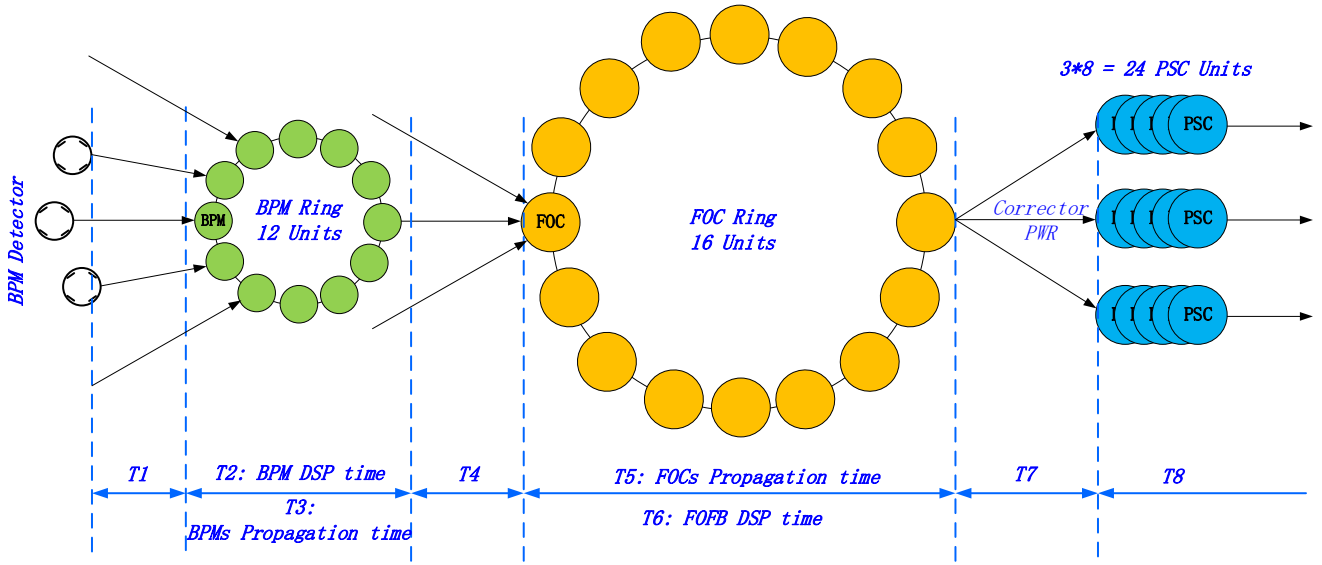




6，FOFB Latency and Bandwidth estimation

Time consumption and FOFB system bandwidth

- FOFB system time consumption testing, and FOFB feedback bandwidth estimation



T1, BPM detector and signal transmission time: 0.2μs

T2, BPM date processing time: 96μs

T3, BPM ring data transmission time: 0.4+12*0.2=2.8μs

T4, Data transmission time from BPM ring to FOFB ring: 1.41μs

T5, FOFB ring data transmission time: 9.75μs

T6, Data processing time of FOFB algorithm: 3.5μs

T7, Data transmission time from FOFB to PSC: 3.0μs

T8, Fast corrector system delay: less then 25μs

Time consumption and FOFB system bandwidth

- The delay of the FOFB system is divided into 8 parts, and the total delay of the system is estimated based on our laboratory test results.

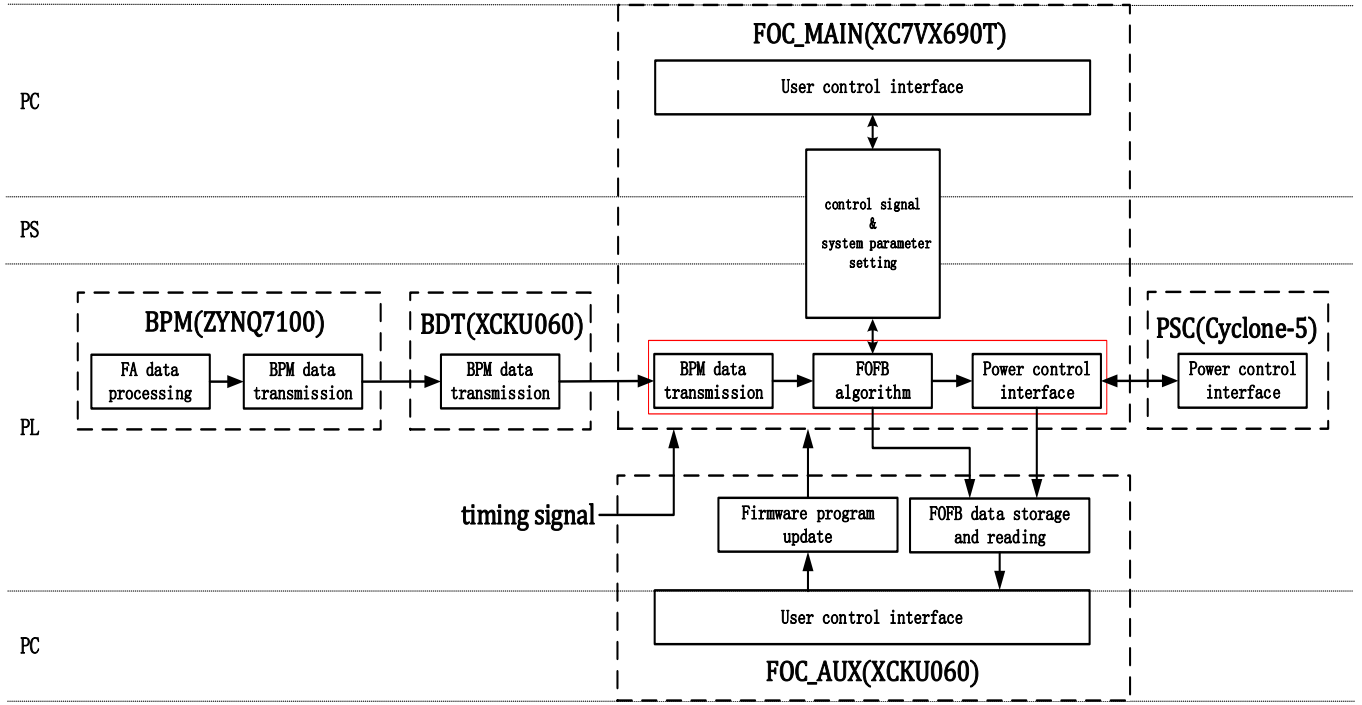
$$T_{totle} = \sum T_i = 141.66\,\mu s \qquad BW_{FOFB} = \frac{1}{10 * T_{totle}} = 705.9Hz$$

- Conclusion: a feedback bandwidth of more than 500 Hz can be achieved for the HEPS FOFB system.

6，FOFB software and algorithm design

➢System software architecture

- Three tier software architecture: PL(Verilog)、PS(C)、PC(Python)
- 8 core software function modules.
- PL: FOFB core signal link, FOFB algorithm, GTH transceiver, etc., directly determine FOFB system performance.
- PS: Developed based on Microblaze soft core, used for data transmission between PL terminal and PC.
- PC: User control interface, data processing and analysis.



Upper-Layer Control Software

- Develop the Upper-Layer Control Software for the FOFB System Using QT.
- The implemented functions include: FOC state control, FOFB parameter setting, FOFB data readout and processing.
- Over 15,000 32-bit FOFB system parameters should be set in the system running time.
- The read data is stored in binary file format, and after format conversion, the data can be saved in large quantities on the server.

Implementation of FOFB algorithm

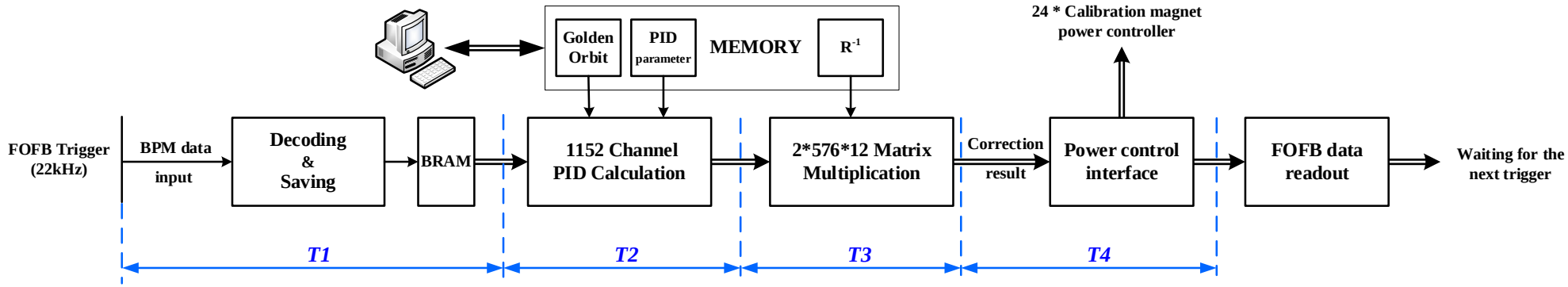
- The core algorithm of FOFB controller adopts periodic pipeline deployment in FPGA.

➢ FOC delay should be less than 35 μs, it needs to be completed within 3500 clock edges （~100M clk）.

➢T1: BPM data transmission time is set based on the actual measurement results of HEPS.

➢T2+T3: Correction calculation, based on Systolic Array, currently completed using 392 clock edges.

➢T4: Computation setpoint transmission time to PSC, adopting a custom transmission protocol ,about 2 μs.



7，Next plan

Next plan in 2025

- We have already completed testing and simulation of the signal links within the red box in the laboratory.
- Next, we will promptly conduct the following tests on HEPS:

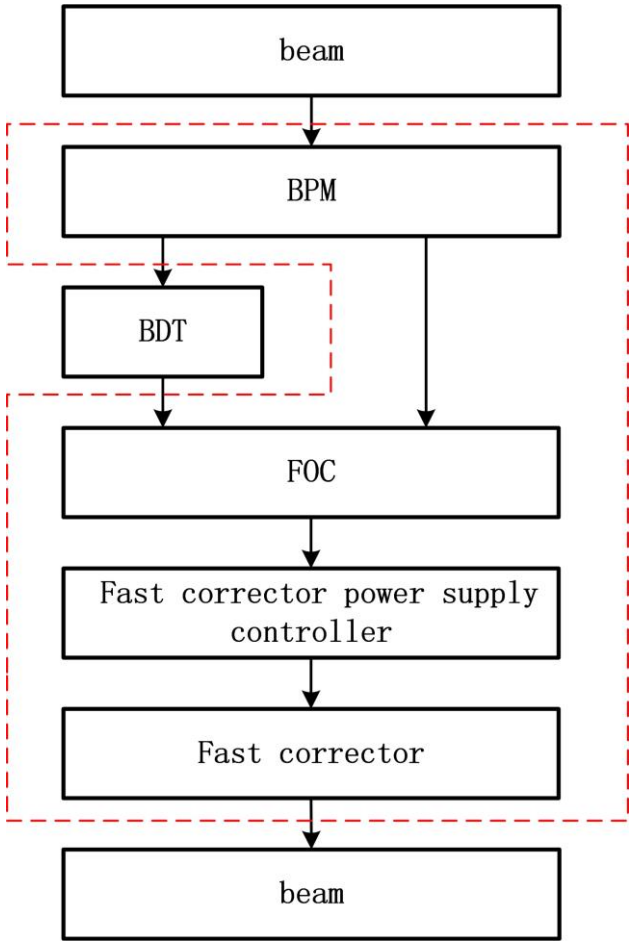
① Communication and latency testing of the 578 BPM data transmission network.

② Interface testing with the timing system and control system.

③ R&D based on actual beam signal in one FOC station.

④ Mass production.

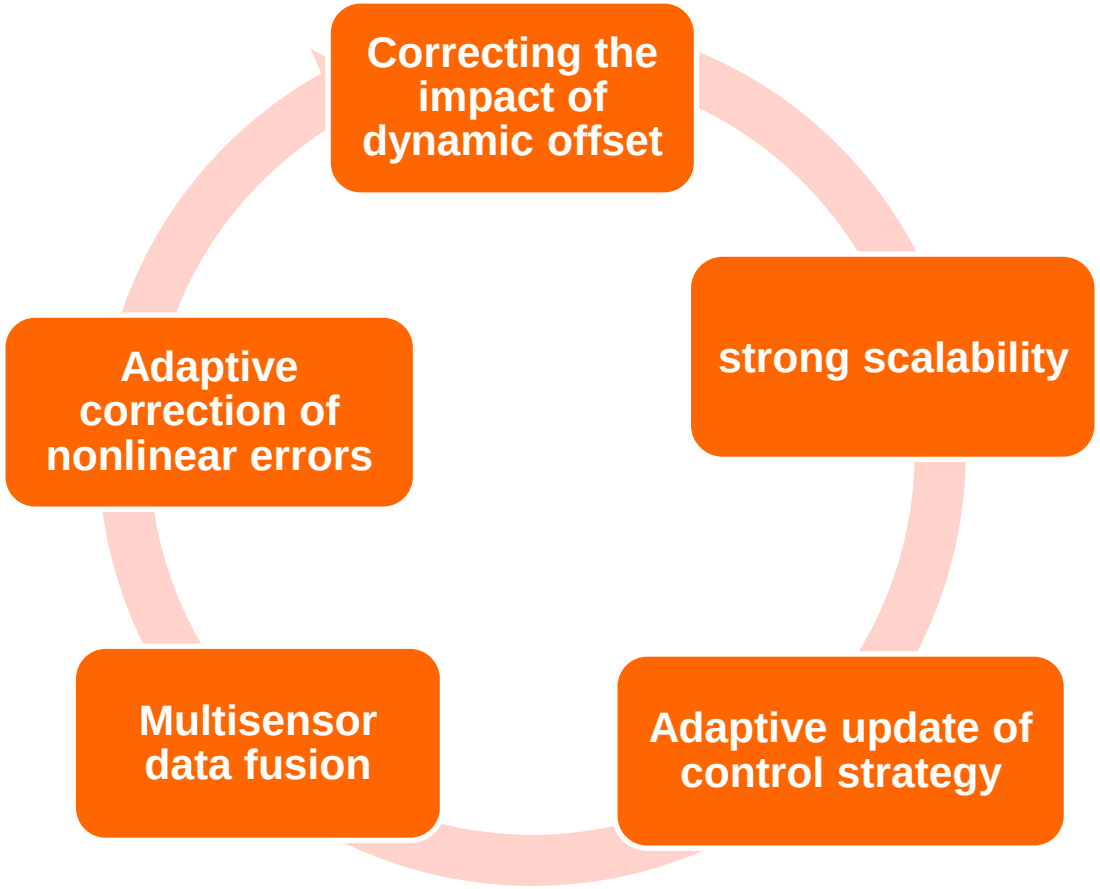
⑤ Start commissioning.



Long-term plans

Target:

- Realize intelligent monitoring and diagnosis of beam current online
- Realize compensation correction for the dynamic offset of the “Golden Orbit" and its impact on the accelerator FOFB system
- Accurate FOFB control of beam based on AI technology
- The developed control algorithm is based on FPGA and can be deployed in different FOFB systems. When the hardware resources meet the algorithm resource requirements, only software upgrades are needed

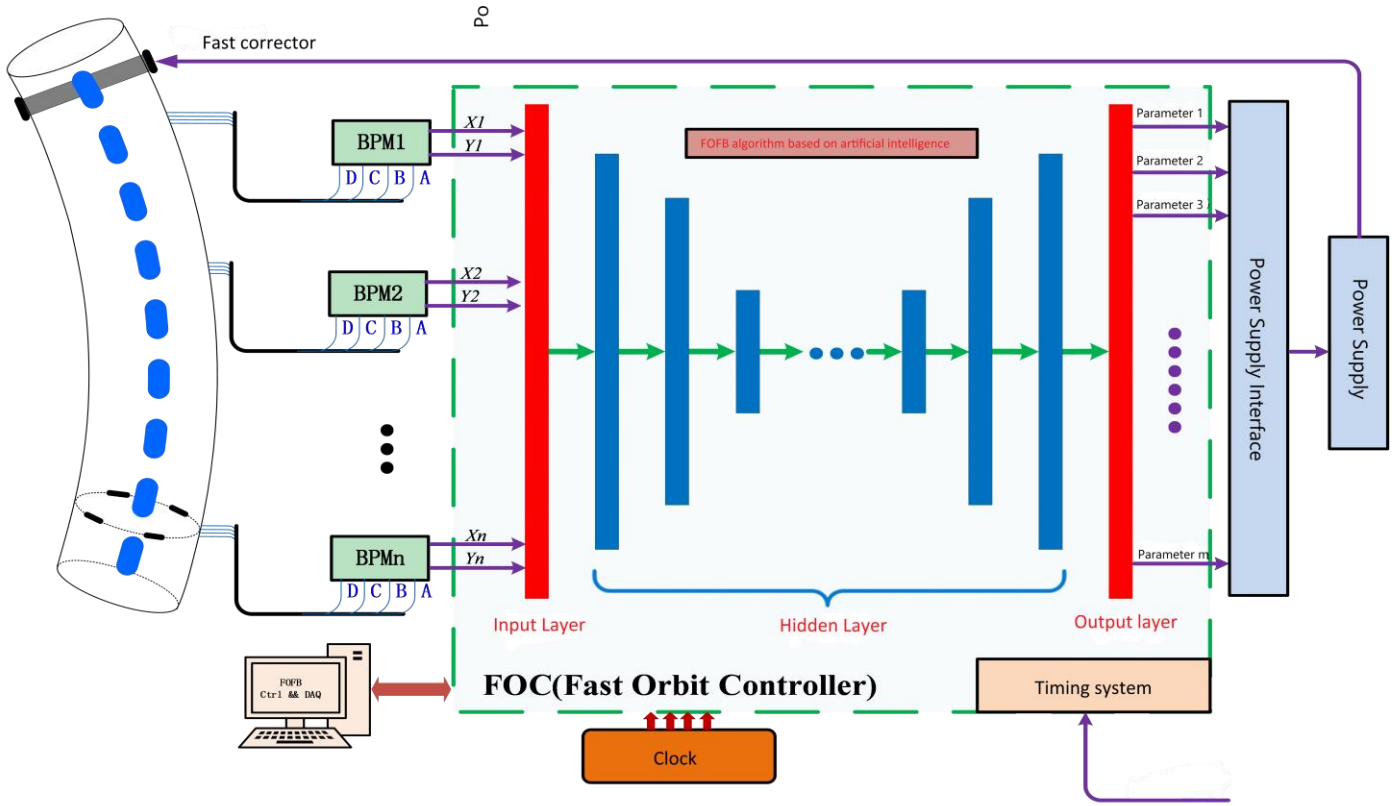


Long-term plans

Hardware implementation Strategy： ZYNQ +GPU

- ZYNQ: Complete high speed data receiving and caching via DDR4 among the BPMs and the Fast Correct Power sources, and the Parallel neural network reasoning acceleration.
  - Xilinx AI Processor IP Core & DPUCZDX8G
  - Supported devices : Zynq® UltraScale+™ MPSoC and ZYNQ 7000, which have been used in the FOFB systems
  - Vitis AI development kit : Verilog, AXI4, HLS
- GPU: Acceleration of neural network reasoning based on GPU.

- ✓ **Feedback control system based on neural network**
- ✓ **Instead of PID algorithm, improves feedback accuracy and reduces data calculation delay**



8, Summary

Summary

- The very small beam sizes of HEPS present significant challenges in achieving orbit stability.
- The FOFB system adopts star-ring data transmission network structure to reduce latency, and promote the system stability, furthermore, expand the input capability.
- We have completed all the hardware design, the overall hardware of the crate adopts a custom ATCA architecture.
- V7-FPGA manages BPM and FC data streams and perform correction computations.
- Based on the current latency test results of various systems, the system can achieve a closed-loop bandwidth of 500 Hz or even higher.
- We will soon complete the small system testing with beam and proceed to mass production. We hope to start commissioning by the end of the year.

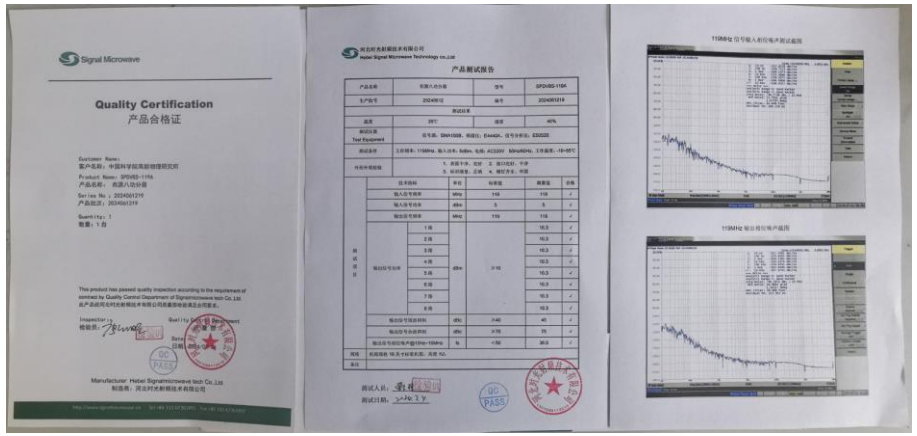
Acknowledgement

- Thanks to Tian Yuke(NSLS2), Yin Chongxian (SSRF), Jiang Bocheng (Chongqing University), Liu Lin (Sirius), Daniel Tavares (Sirius), Fernando de Sa (Sirius), and Holger Schlarb (DESY) for their insightful discussions.

Thank you for your attention!

RF clock fanout mdoule

- 1-8 power splitter for RF clock fanout.



BDT module function block

- FOFB BDT Function block
- Key features
  - Receive all 12 BPMs from one station;
  - Receive all XBPMs near the FOFB station;
  - Check, reassemble, and align all BPM data;
  - Finally, send the data to the FOC module using one fiber.