SiMPl devices - status and perspectives

- SiPMs basics
- SiPMs with Bulk Integrated Quench Resistors – SiPMl concept
- Results from the prototype production
- Future perspectives

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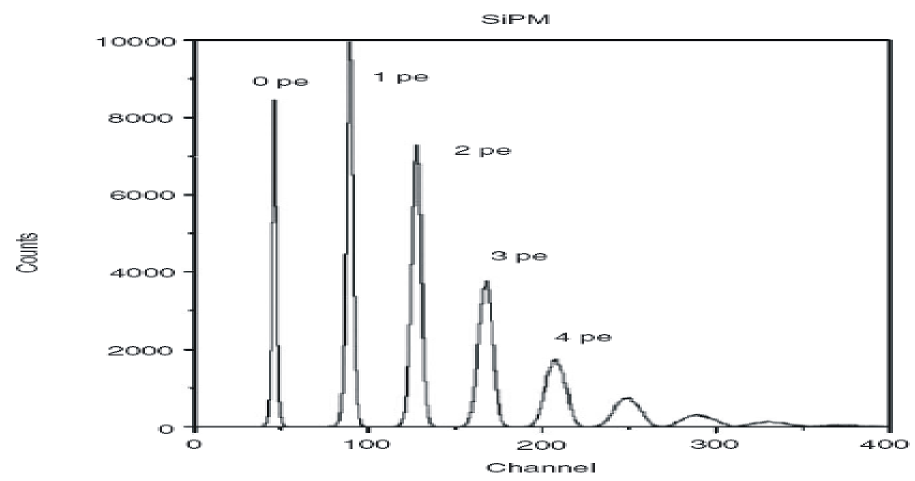
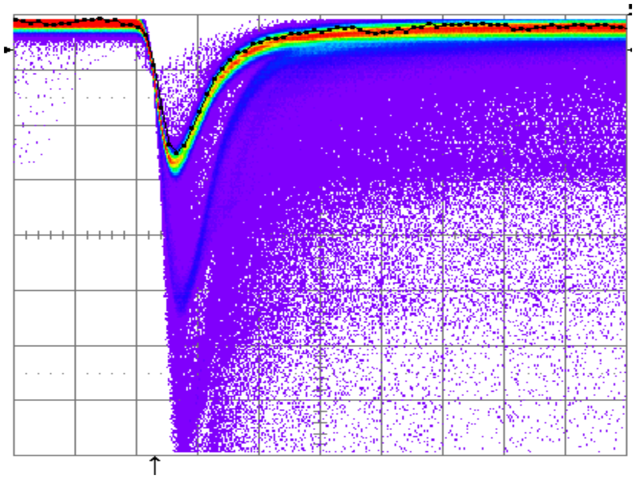
SiPM Basics



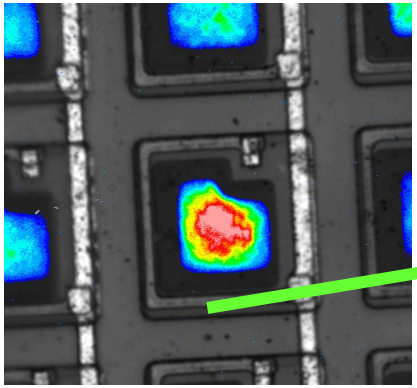
Array of avalanche photodiodes operated in Geiger mode and read out in parallel.

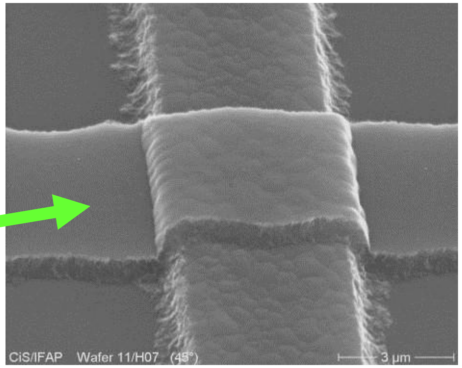
Require connection of quench resistor to stop the avalanche.



Operating voltage: «100 V
Gain: 10^5 up to 10^7
single pixel time resolution: ≈100 ps
single pixel recovery time: <1μs
dependence of Gain on Temp.: 0.5% dG/dT
peak photon detection efficiencies: ≈ 40% @ 500nm
dark count rate/mm²: 10^5-10^6 counts per second at room temp.
(strong dependence on temperature)

Polysilicon Quench Resistors



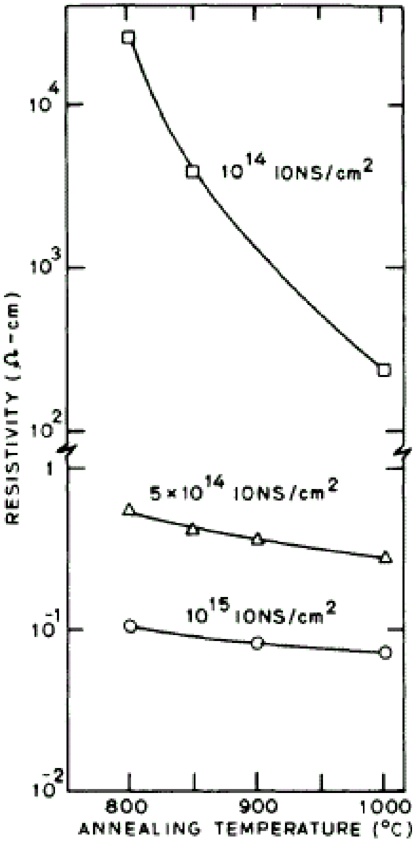


Complex production step

Critical resistance range

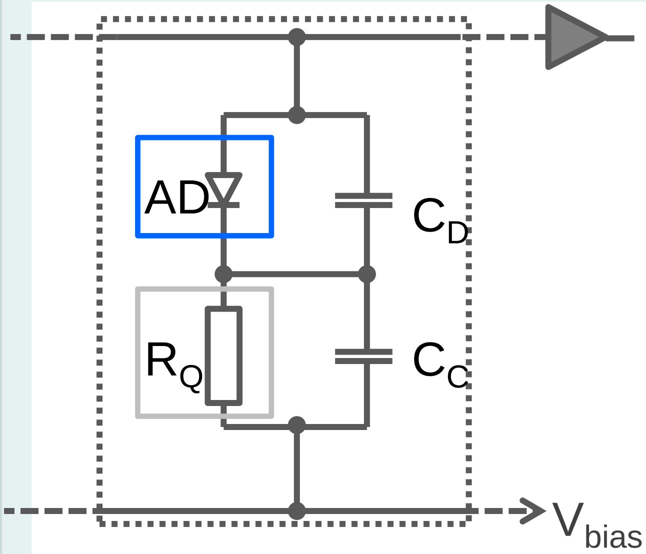
influenced by: grain size, dopant segregation in grain boundaries, carrier trapping, barrier height

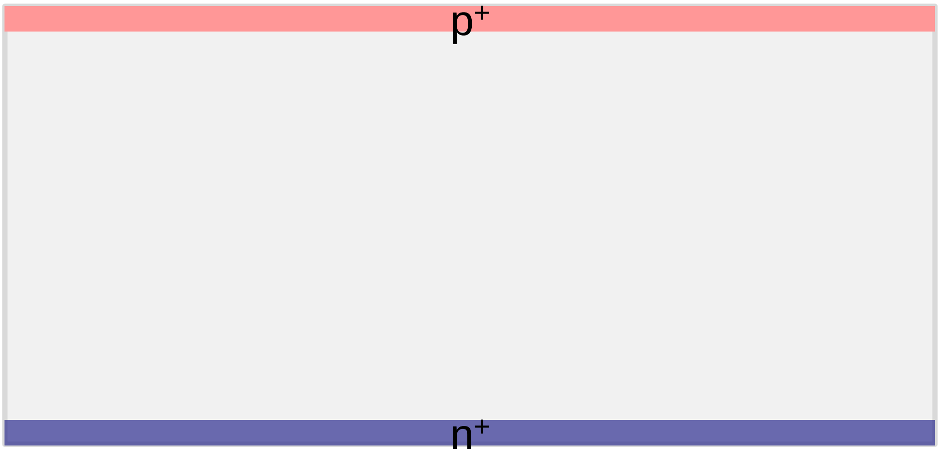
Rather unreliable process step and an obstacle for light



M. Mohammad et al.
'Dopant segragation in polycrystalline silicon',
J. Appl. Physics, Nov.,1980

SiPM cell components → SiMPI approach

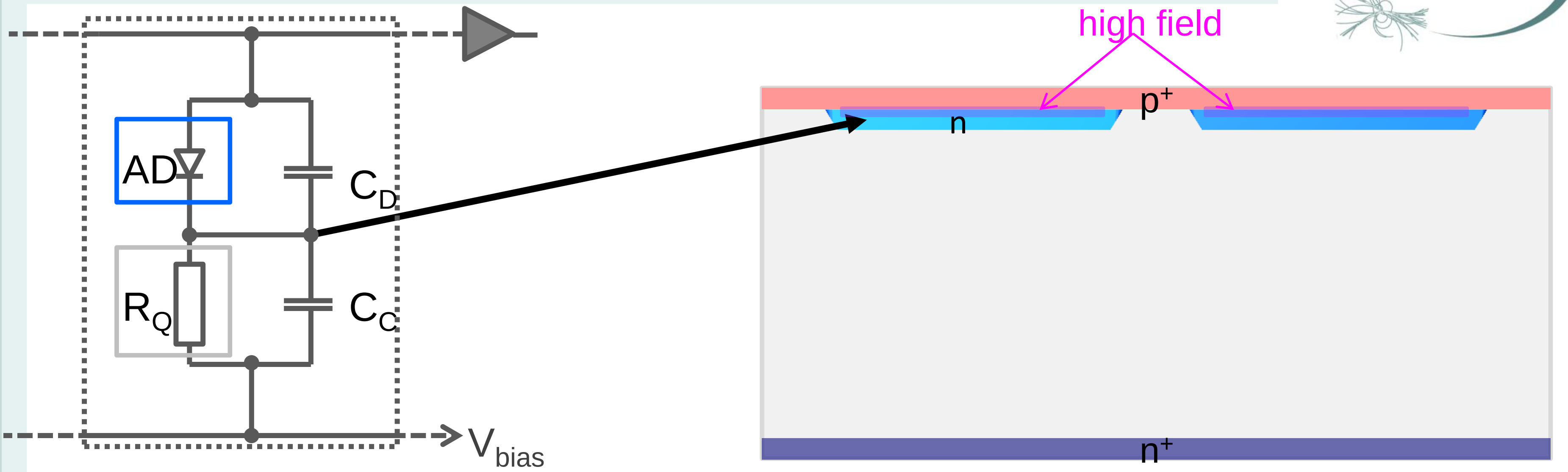




Idea brought by R. Richter

L. Andricek and G. Lutz

SiPM cell components → SiMPl approach



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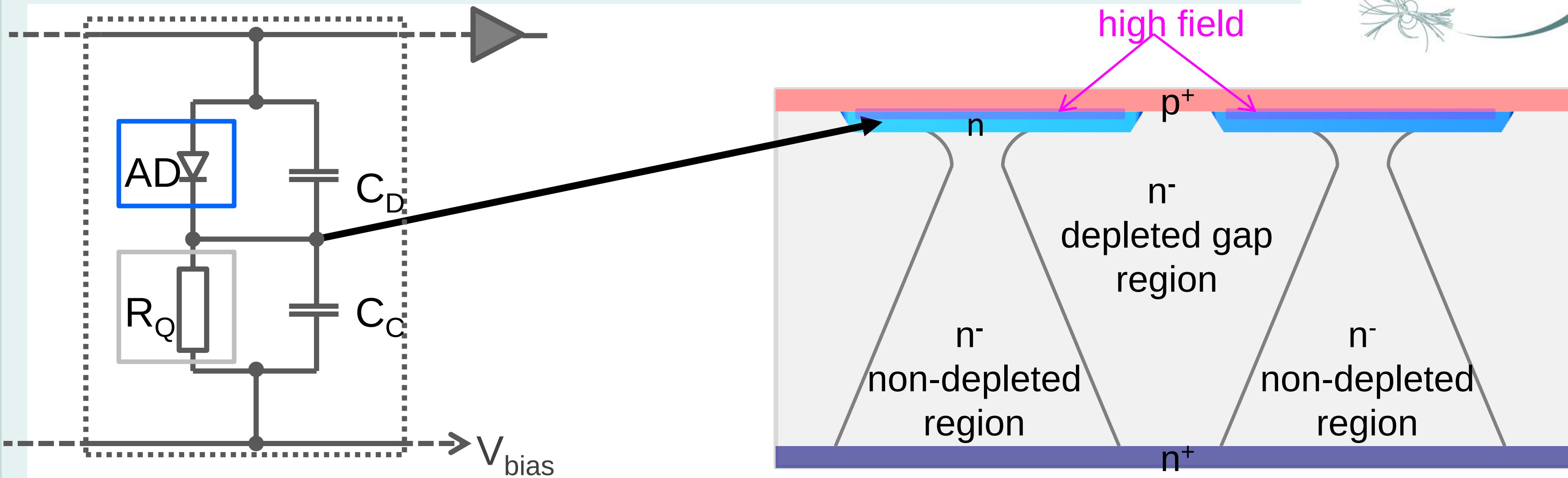

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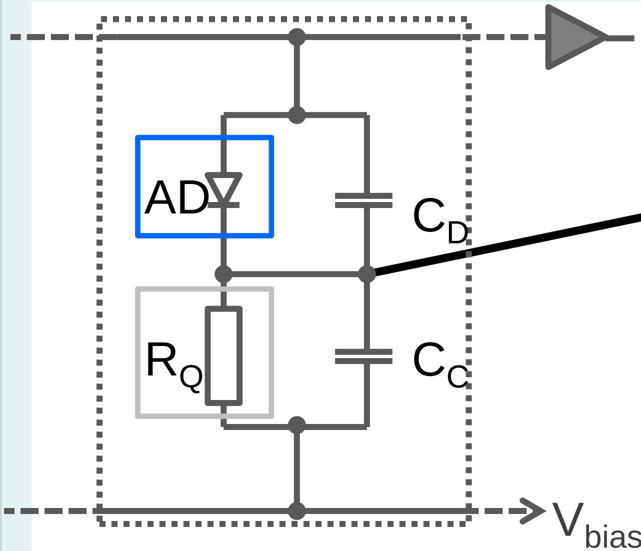
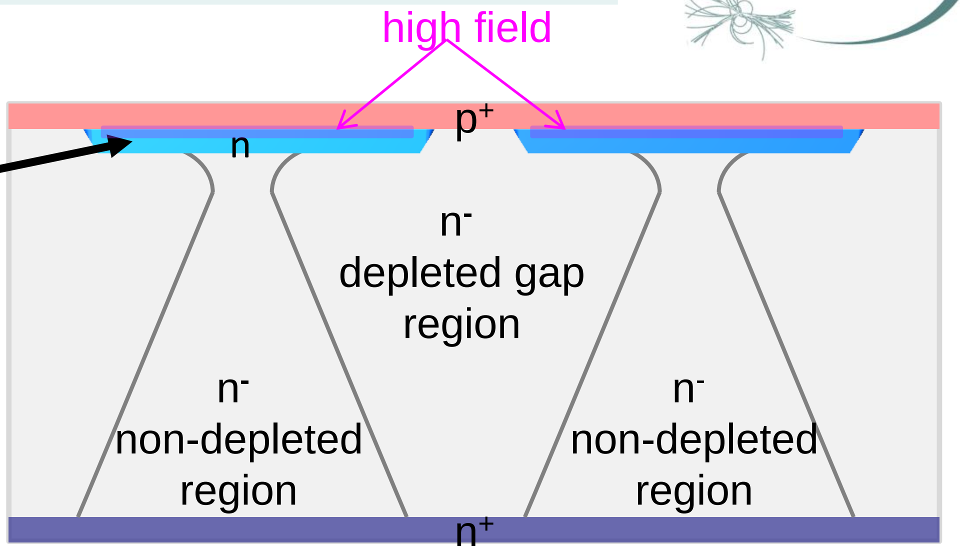
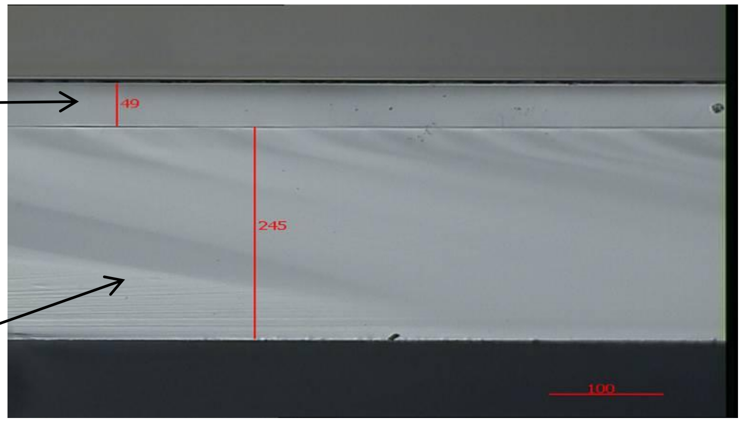




SOI wafers

Sensor wafer

Handle wafer



Advantages and Disadvantages

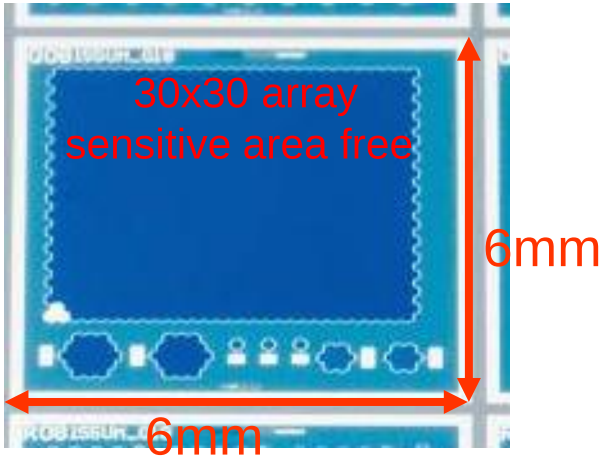
Advantages:

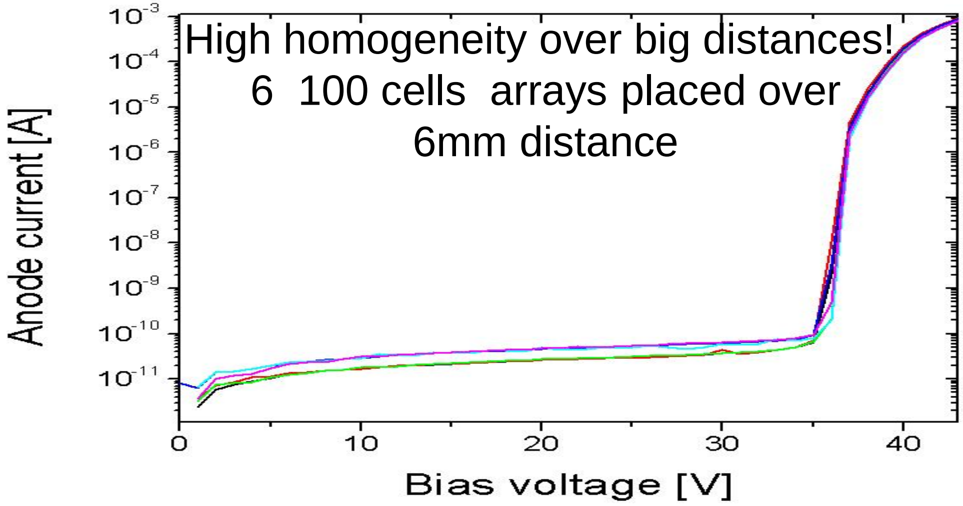
- no need of polysilicon
- free entrance window for light, no metal necessary within the array
- coarse lithographic level
- simple technology
- inherent diffusion barrier against minorities in the bulk -> less optical cross talk

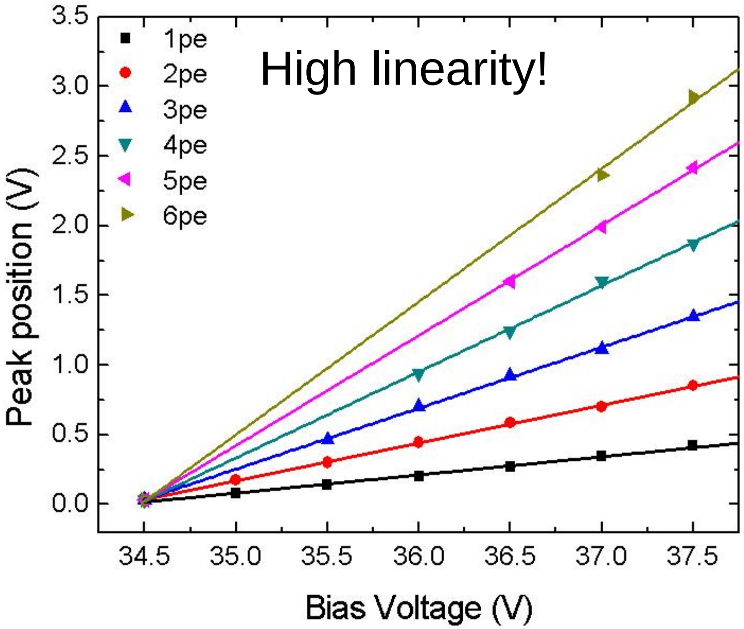
Drawbacks:

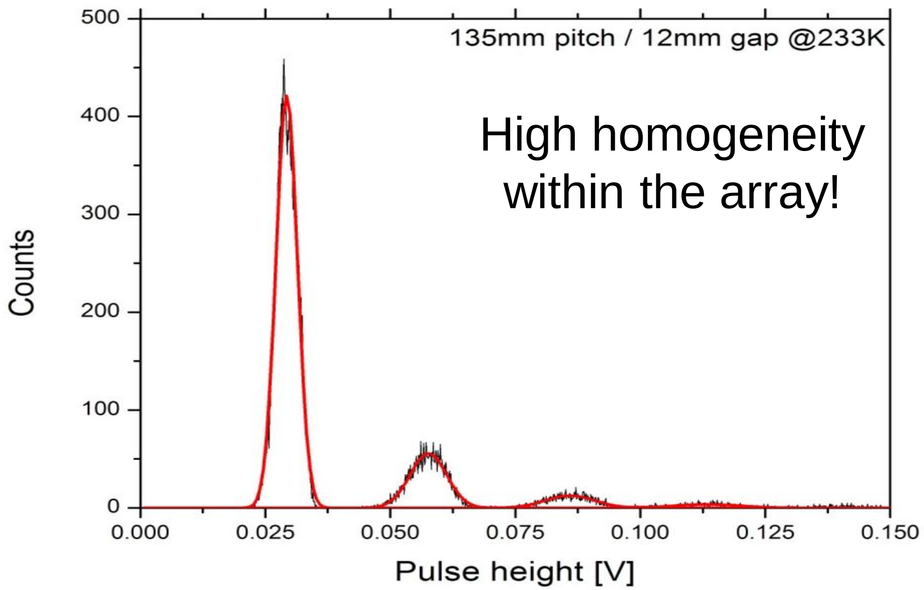
- required depth for vertical resistors does not match wafer thickness
- wafer bonding is necessary for big pixel sizes
- significant changes of cell size requires change of the material
- vertical ‘resistor‘ is a JFET -> parabolic IV -> longer recovery times

Prototype production





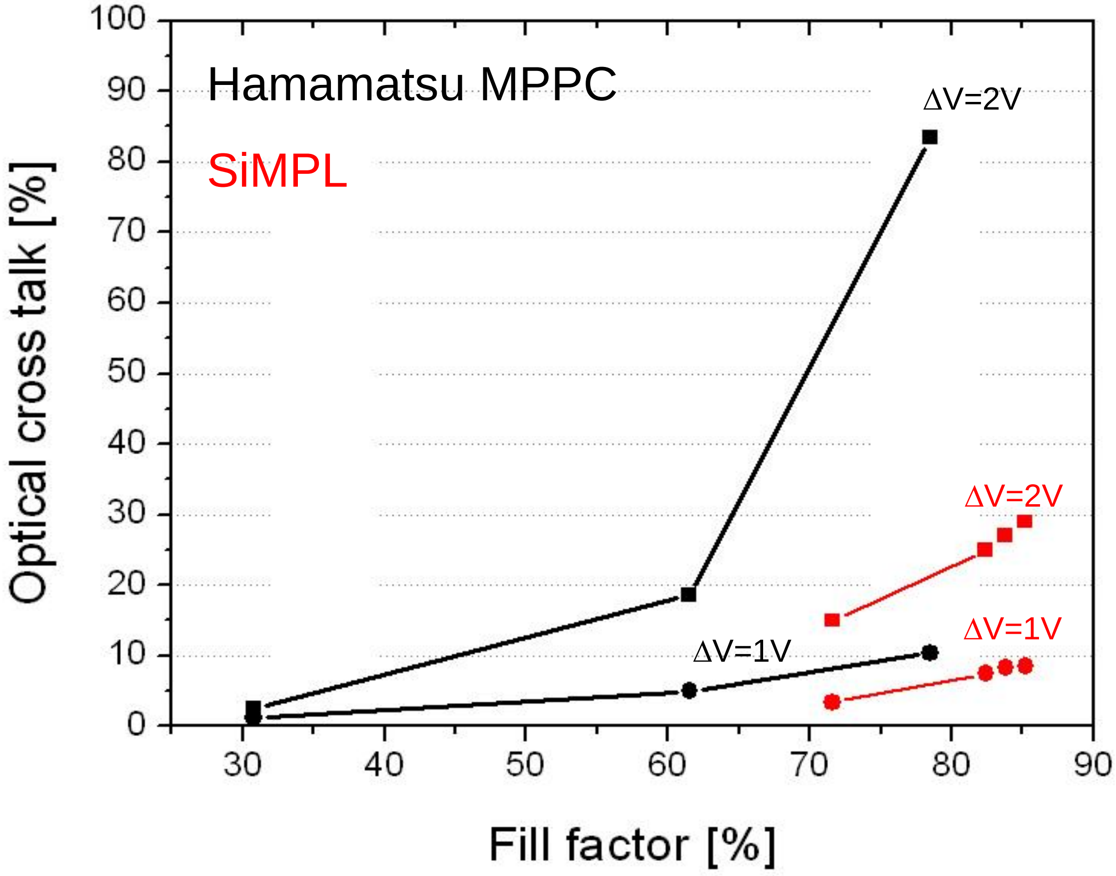




Fill factor & Cross Talk

Produced SiMPl devices have the extremely high fill factors and still lower cross talk!

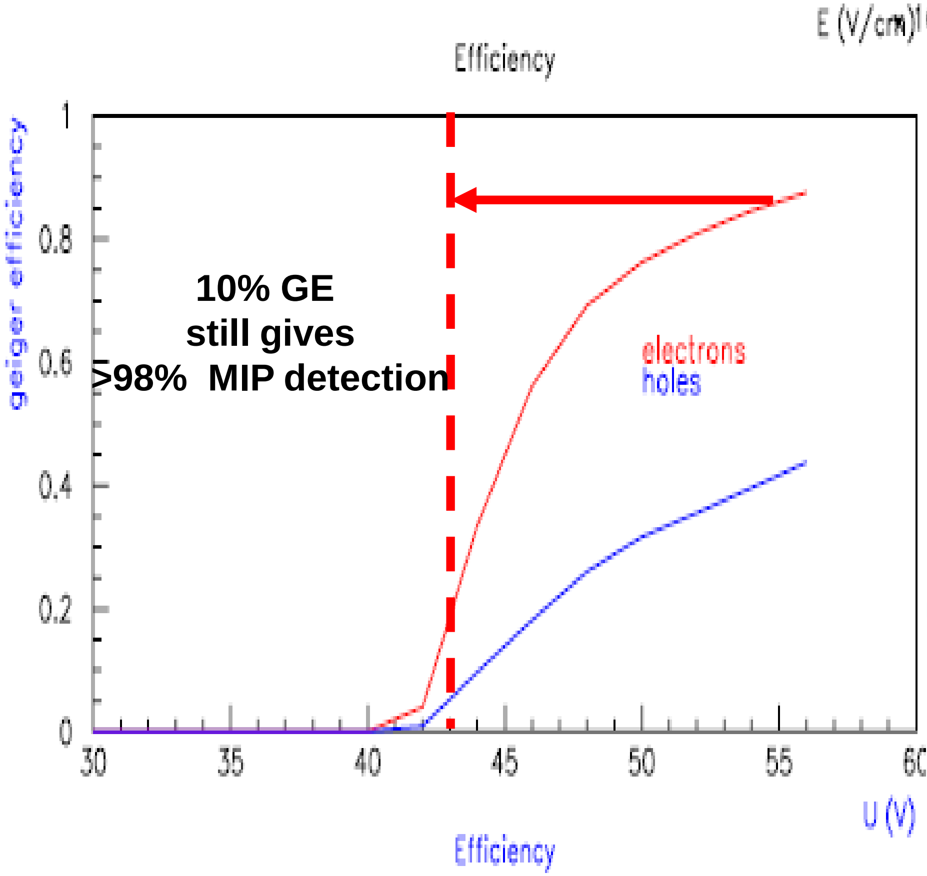
No special cross talk suppression technology applied
just intrinsic property of SiMPl devices

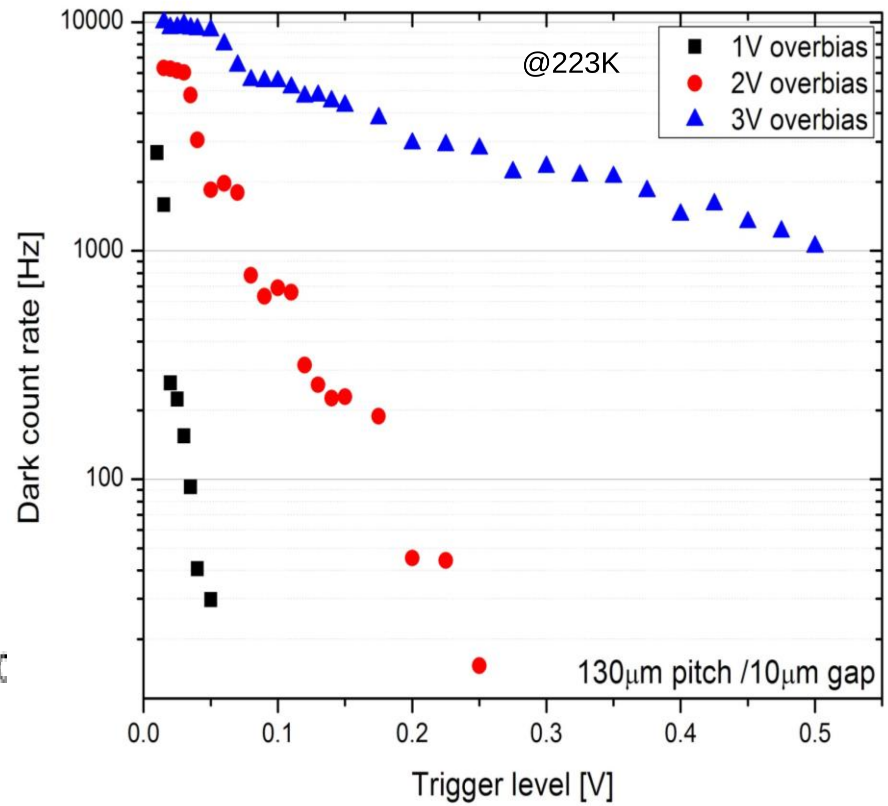


Detection of particles

Excellent time stamping due to the fast avalanche process (<1ns)

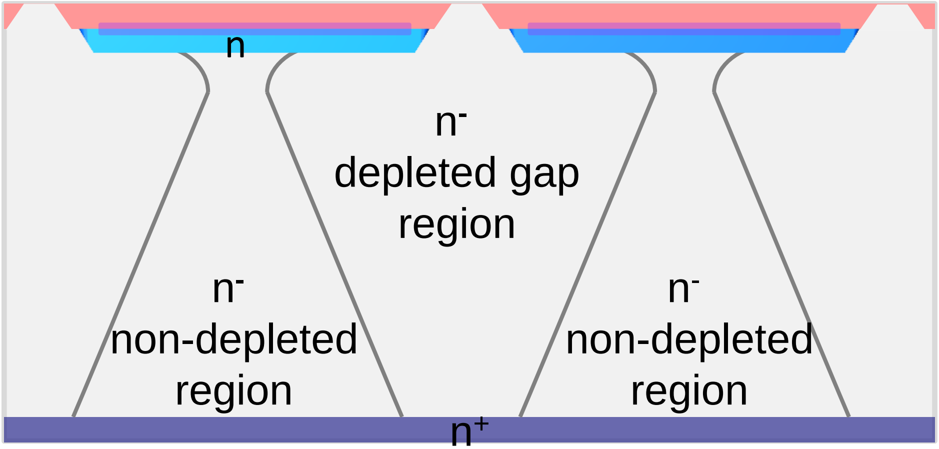
MIP gives about 80pairs/μm → huge signal in SiPM→ allows operation at small ΔV





Reduction of dark rate and cross talk by order of magnitude

Next generation SiMPI devices



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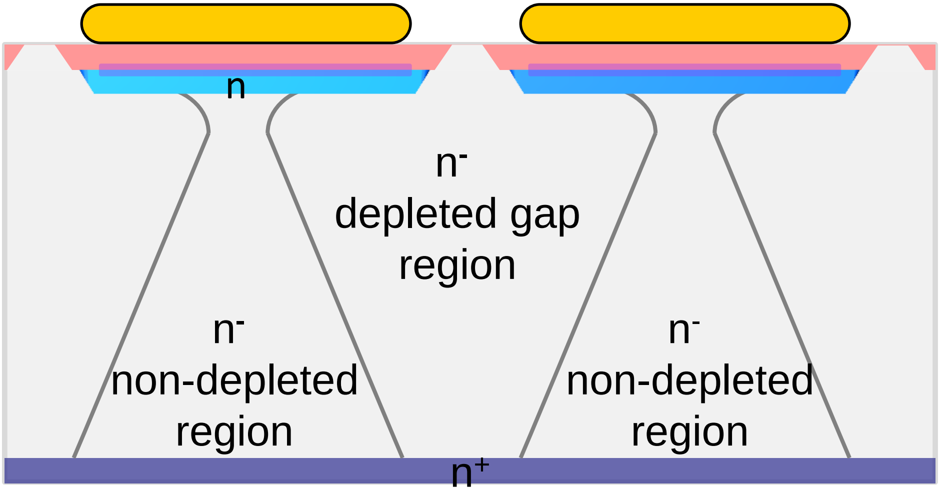

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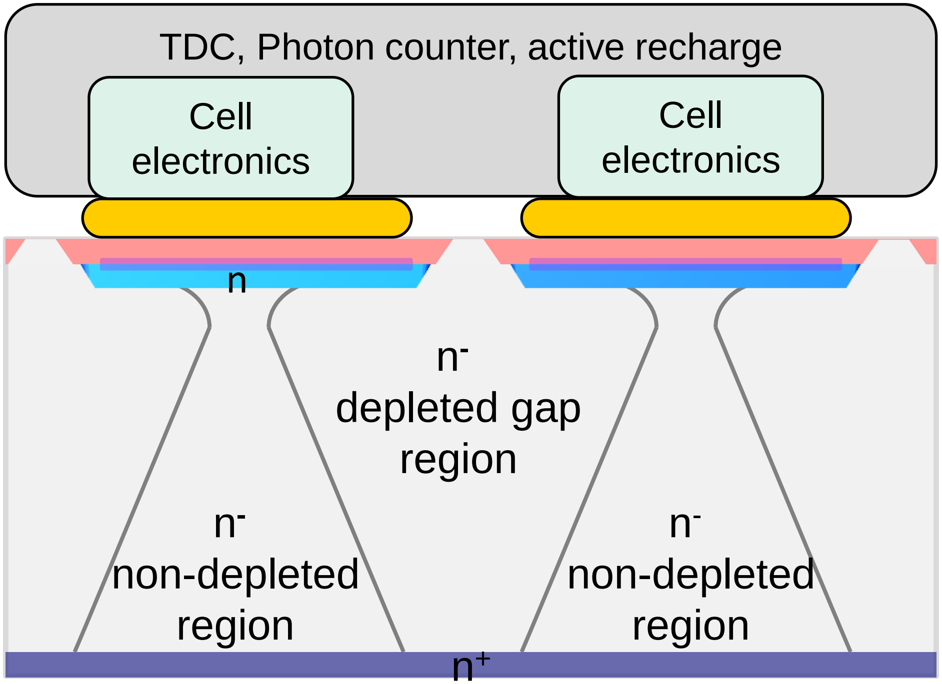


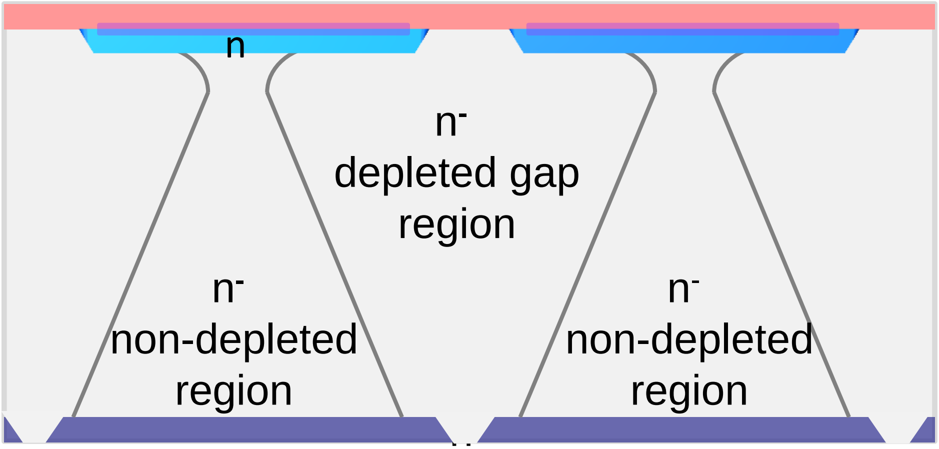
Topologically flat surface

High fill factor

Adjustable resistor value

Pitch limited by the bump bonding

Next generation SiMPl devices

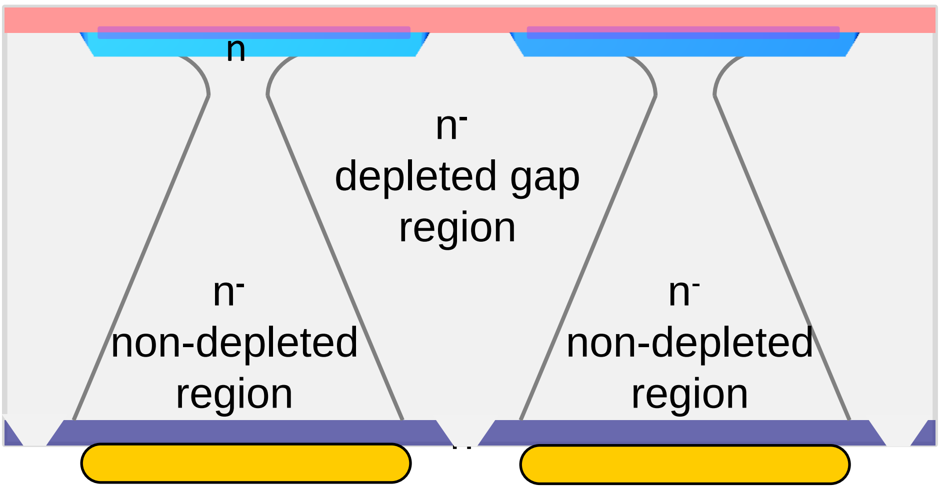


Topologically flat and free surface

High fill factor

Sensitive to light

Next generation SiMPl devices



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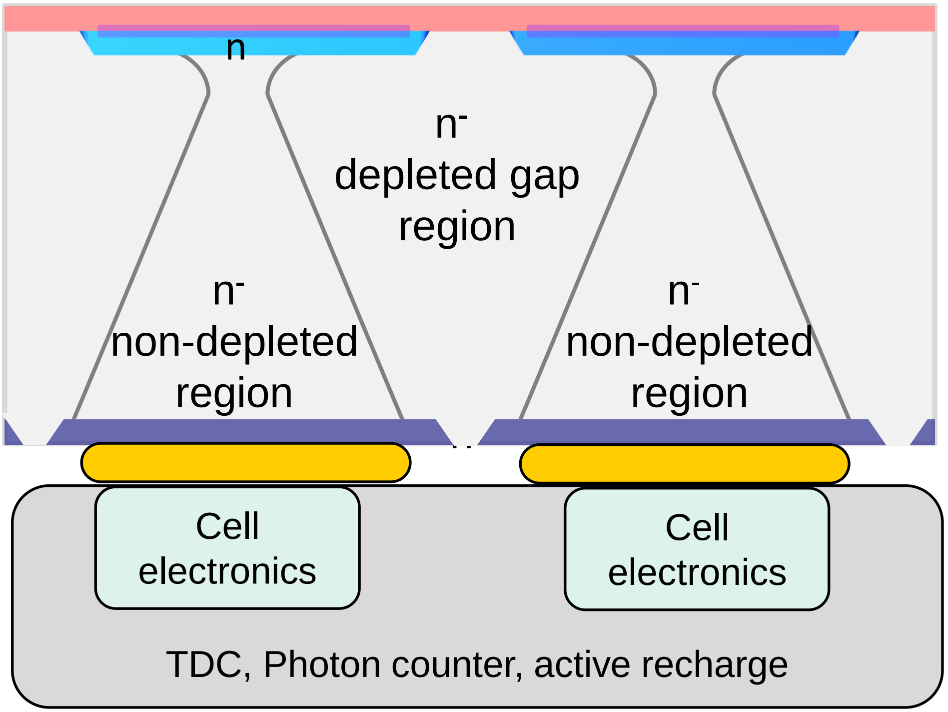

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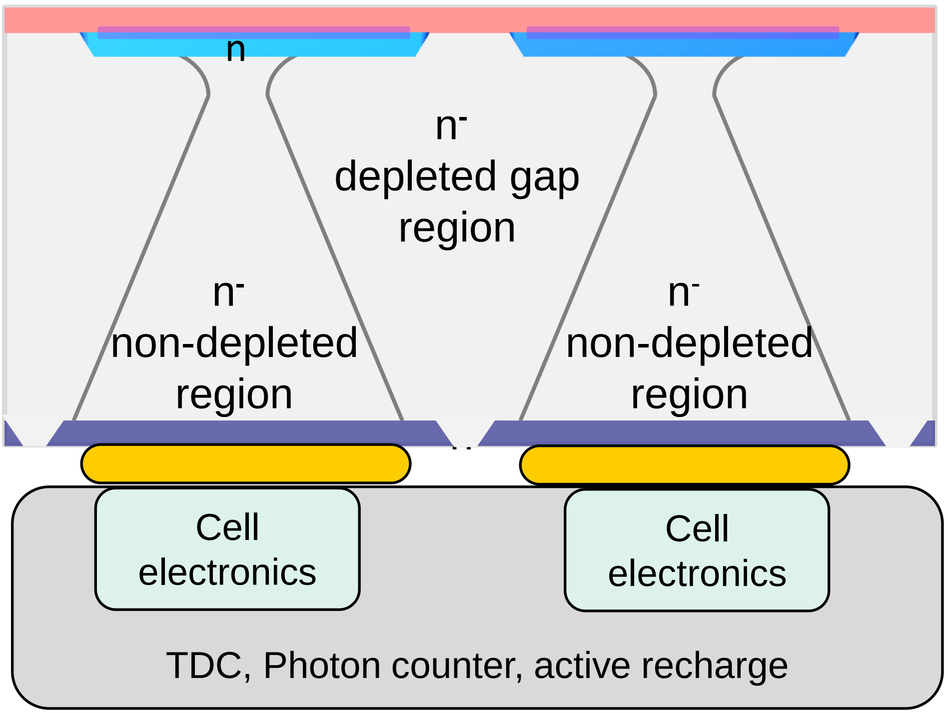


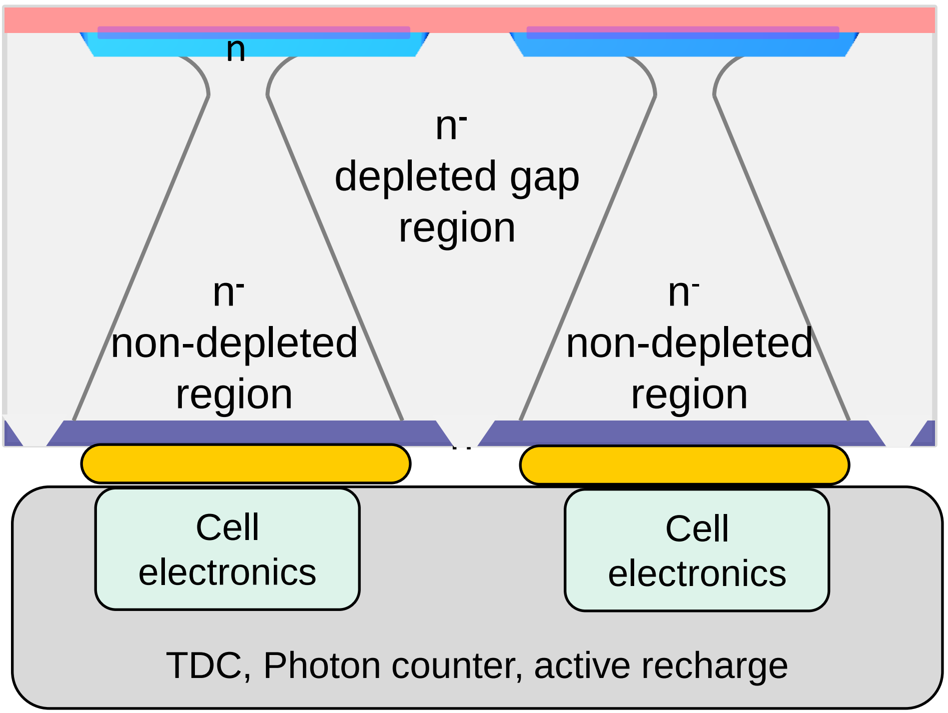
Topologically flat and free surface

High fill factor

Sensitive to light

1. Structured implant on backside on sensor wafer
2. bond sensor wafer to handle wafer
3. thin sensor side to desired thickness
4. process SiMPl arrays on top side

Next generation SiMPl devices



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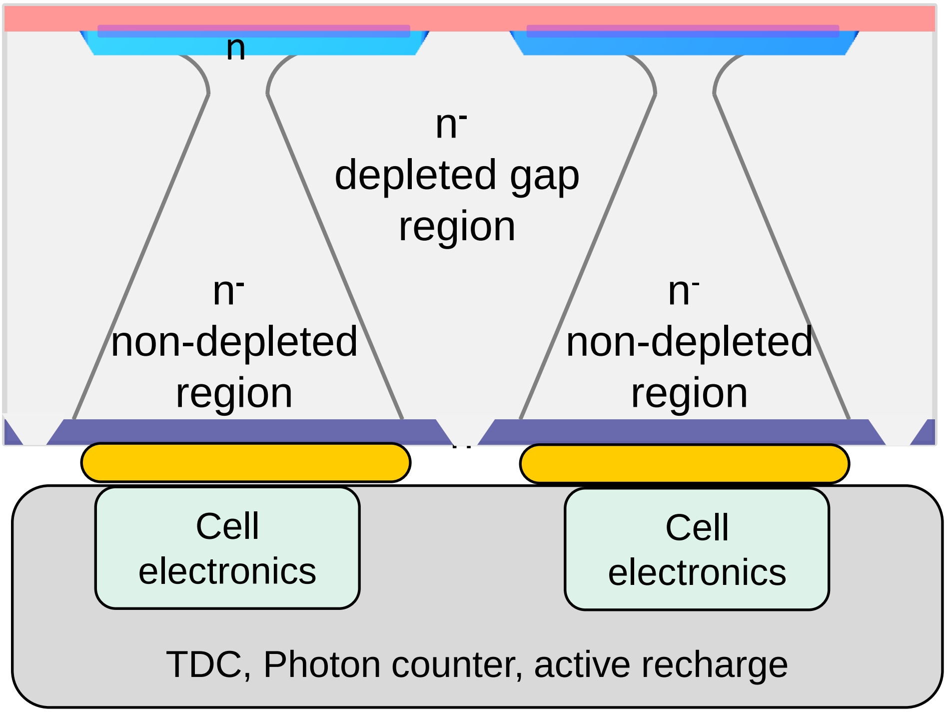

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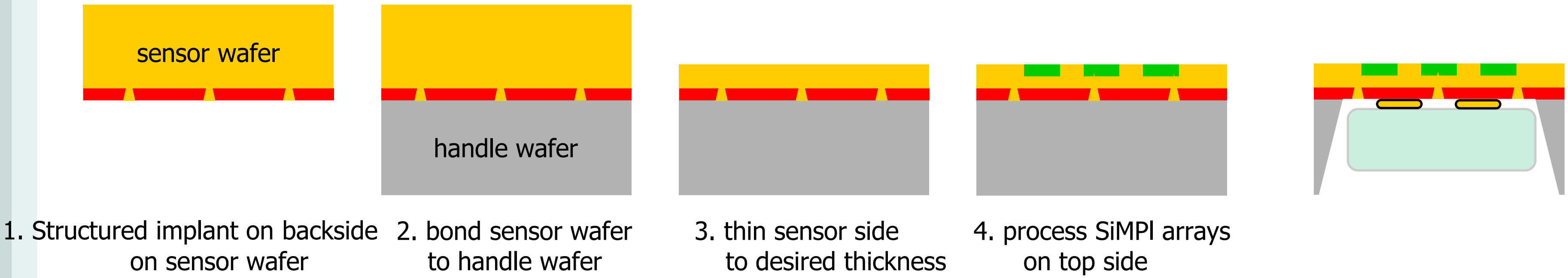

Thanks for your attention!!!

Questions?

Fill factor & Cross Talk & Photon Detection Efficiency

Produced SiMPI devices have extremely high fill factors!

Pitch / Gap	Fill factor	Cross talk meas. (ΔV=2V)	PDE calc. (ΔV=2V)	PDE calc. (ΔV=5V)
130μm / 10μm	85.2%	29%	41%	65%
130μm / 11μm	83.8%	27%	40%	64%
130μm / 12μm	82.4%	25%	39%	63%
130μm / 20μm	71.6%	15%	34%	54%

PDE estimate PDE= FF x QE x GE:

- Optical entrance window: 95% @400nm
- Geiger efficiency : 50% @ 2V overbias 80% @5V overbias